Filling of nano-via holes by laser-assisted direct imprint

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Available online 14 February 2006

Abstract

A new technique for filling narrow and high-aspect ratio nanoscale via holes by laser-assisted direct imprint has been proposed and developed. In the process, the filling material (e.g., metals or Si) is first deposited onto the nano-via holes by a deposition method that has a poor step coverage and hence fills the holes partially with voids. Then a mirror-flat transparent plate (mold) is pressed against the substrate, while an excimer laser pulse (XeCl, 308 nm wavelength, 20 ns pulse duration) shines through the mold. The laser pulse melts the filling material, and the flat mold presses the molten materials into the holes, filling them completely without voids. As examples, we successfully filled a hole array having 100 nm diameter, 500 nm depth (aspect ratio 5) and 200 nm inter-hole spacing (pitch) with e-beam evaporated silicon and copper. Besides superior step coverage and negligible thermal budget, this technique is fast and simple and doesn’t need a seed layer. Furthermore, it can planarize the wafer surface in addition to filling the holes. Clearly, this technique could be extended to other materials important for ICs metal interconnect, and may become an alternative to the dual damascene and CVD tungsten plug process used in the current ULSI fabrication.

Keywords: LADI; Nanoimprint; Pulsed excimer laser; Via filling; Step coverage; Nanofabrication

1. Introduction

Filling via holes or trenches with a deposited material is an important step in IC manufacturing. At present, the metal interconnect for ICs is typically fabricated by the dual damascene and, for the first wiring level, tungsten CVD plug process [1,2], where the via holes and trenches are etched in a dielectric material and subsequently filled up with a metal. Clearly, any voids left in the vias or trenches caused by poor step coverage will create a serious problem for the interconnects.

Though superior to PVD, the step coverage of tungsten CVD is still limited by the low volatility of the precursor gas WF6 that leads to a low vapor pressure. The result is a mass transport limited deposition rate, and the hole opening receives faster deposition and would be closed before the holes are completely filled. Another disadvantage of CVD is its relatively high thermal budget.

Atomic layer deposition (ALD) can achieve excellent step coverage in certain conditions [3]. It is a modified form of CVD with gas precursors introduced one at a time with pump/purge in between. So the film is deposited one atomic layer per cycle, with a typical deposition rate of order 0.5 nm/min. Not only the slow deposition rate is a manufacturing issue, but also in ALD, voids will be formed if the via holes or trenches have a sidewall with negative angle.

Another candidate for filling future high-aspect ratio vias is chemical fluid deposition (CFD) developed recently [4]. CFD uses supercritical fluids like CO2 as a carrier for organometallics. As the supercritical fluid CO2 retains its gas nature and can flow into deep holes, the material deposition rate is limited by chemical reaction rate, giving conformal step coverage. The drawbacks of CFD include high process pressure of order 100 bar and limited choice...
of precursors having high solubility in the supercritical fluid. Moreover, like ALD, voids will be formed when vias or trenches have a negative sidewall angle.

Therefore, there is still a great need for a new method capable of completely filling nano-via holes with high-aspect ratio, regardless of the sidewall angle, and with a high throughput. In this work, we will demonstrate that high-aspect ratio holes can be filled by pressing while melting momentarily the filling material using a pulsed laser, a process similar to laser-assisted direct imprint (LADI) [5] and laser-assisted nanoimprint lithography (LAN) [6].

2. Experiments and results

To demonstrate our method of filling nanoscale via holes by LADI, we fabricated in Si a hole array having 100 nm diameter, 500 nm depth (aspect ratio 5) and 200 nm inter-hole spacing (pitch). The hole array was patterned by nanoimprint lithography and etched by Cl₂/Ar RIE. As silicon is a good heat sink, a 15 nm thermal oxide layer was grown to reduce heat loss to the surrounding bulk Si, and to shrink the hole size at the same time. Finally, 200 nm Si or Cu was deposited on top of the hole array by e-beam evaporation. As expected and shown in Fig. 1, evaporation has very poor step coverage, so the holes were only partially filled, with the sidewall of the holes receiving little deposition before the hole opening was closed.

During the hole filling by LADI, we pressed a UV grade quartz plate with a mirror-flat surface against the substrate coated with the filling material, and vacuumed the sample assembly below 200 mTorr. Then a single excimer laser pulse (XeCl, 308 nm wavelength, 20 ns pulse duration, 2.5 × 2.5 mm² beam size) of fluence 1.1 J/cm² melted the filling material momentarily. When in molten state, Si and Cu have very low viscosity (see the following section), so they could flow into the hole and reach the hole bottom within some 100 ns. Fig. 2 shows via filling by Si, indicating a complete filling without voids. For via filling by Cu (Fig. 3), the Cu plugs were found broken after wafer cut, and it is possible that the built-in stress caused by fast cooling of the liquid Cu has contributed to the Cu plug fracture. Nonetheless, we believe that most holes were completely filled to the bottom, as indicated by the Cu plug sections found on the bottom of the holes.

For both Si and Cu filling, based on the laser fluence and thermal properties of the related materials, the 15 nm SiO₂ and a very thin layer of the surrounding Si at the upper part of the hole should have been melted. However, due to the 8–9 orders higher viscosity of SiO₂ compared to that of the filling material, the flow of the molten SiO₂/Si is negligible, leading to no apparent distortion of the holes, as evidenced by the regular and distinct shape of the Si and Cu plugs with diameter corresponding to the original hole diameter. On the other hand, the 15 nm thermal SiO₂ is much thinner than the characteristic heat diffusion length (see the following section) of 260 nm for SiO₂, leading to significant heat loss to the bulk Si. The via filling would be greatly facilitated in reality when the vias are surrounded by a thick thermal insulator.

During the via filling by LADI, the wafer surface could also get planarized due to the low viscosity of the molten material and the flat surface of the mold. The wafer planarization method, termed as wafer planarization by laser-assisted direct imprint (PLADI), will be discussed elsewhere [7].
3. Discussions

In the via filling process, the driving force is apparently the applied pressure. The counter forces include surface tension, the viscous force and the inertial force. For simplicity, we will discuss them separately.

The minimum applied pressure necessary for squeezing the molten material into the holes is determined by the surface tension and has order of \( \sigma / \phi \) with \( \sigma \) as surface tension and \( \phi \) as hole diameter. As seen in Table 1, liquid Si and Cu have surface tensions one order higher than that of water, necessitating order of 100 bar for filling holes with 100 nm diameter. In practice, this restriction could be relieved by coating the wall of the holes with a thin lining layer that wets the molten filling material.

The effect of viscous force can be estimated by assuming that a steady flow develops momentarily at a distance \( L \) from the top dielectric surface, or 400 \( \mu \)m for SiO\(_2\) that conducts heat better, then the maximum temperature experienced at the dielectric/semiconductor interface should be \( <1/5 \) that of the maximum temperature at the top dielectric surface, or 400 \( ^\circ \)C if assuming a maximum surface temperature of 2000 \( ^\circ \)C; and the heating lasts for only order of 10 \( t_p \) (=200 ns here). As a consequence, unlike tungsten CVD, the via-hole filling by LADI would have a negligible thermal budget.

Besides superior step coverage and negligible thermal budget, the current technique is fast and simple and doesn’t need a seed layer. Its disadvantage, as compared to tungsten CVD, lies in the challenge to scale up due to the likely high pressure required to overcome the surface tension, and the availability of high power pulsed laser having wafer-size power uniformity.

4. Summary

We have demonstrated a novel process capable of completely filling deep high-aspect ratio holes by laser-assisted direct imprint. The holes are 500 nm deep and 100 nm wide, with a spacing of 200 nm between neighboring holes. The filling materials are e-beam evaporated Si and Cu, and the filling time is on the order of 100 ns. Besides Si and Cu, this process could be extended to other materials important to ICs and other nano-devices. Together with trench filling and wafer planarization that can be accomplished simultaneously, the current process could fulfill the needs for ICs metal interconnect that is currently realized by the dual damascene and tungsten CVD process.

References

