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Selective tungsten filling of sub-0.25 μm trenches for the fabrication of scaled contacts and x-ray masks

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Trenches in a layer of SiO_2 on Si, with feature sizes down to 0.125 μm have been filled with tungsten (W) using selective chemical vapor deposition (CVD). The trenches were formed in a fashion similar to contact vias by reactive ion etching the SiO_2 to the underlying silicon. The tungsten was then deposited in a cold wall CVD reactor, by silane reduction of WF_6, to a thickness of 0.5 μm. The process results in good planarity and uniformity making it suitable for the fabrication of sub-0.5 μm contacts and interconnects, and for the formation of high aspect ratio absorbers in x-ray masks.

I. INTRODUCTION

Over the recent years, the selective deposition of tungsten has emerged as an attractive technique in many very large scale integrated (VLSI) applications, especially for planarization in multilevel metallization[1–3] and interconnect technologies.[4] In particular, contact and trench filling with tungsten deposition greatly improves the quality of metal step coverage, and tungsten exhibits lower resistance than polysilicon for interconnects. In addition, tungsten is widely used as an absorber in the fabrication of masks for x-ray lithography[5,6] because of its high absorption of x rays and the compatibility of its thermal expansion coefficient with that of the silicon membrane. Contact vias and trenches with dimensions down to 0.75 μm have been succcessfully filled with tungsten[3,7–9] using either selective chemical vapor deposition (CVD) deposition or a blanket deposition followed by etch back. However, as the integrated circuit technology continues to evolve and as device dimensions are scaled down, it will be soon necessary to scale contacts and interconnects to dimensions below 0.5 μm. Furthermore, the fabrication of masks for high resolution x-ray lithography demands high aspect ratio absorber with feature sizes below 0.25 μm.

The selective CVD of tungsten by either the hydrogen[1,10,11] (H_2) or silane[11–13] (SiH_4) reduction of WF_6 has been previously reported and studied. The H_2 reduction process results in good conformal coverage, but causes low deposition rates especially at temperatures lower than 325 °C and results in encroachment and "wormholes" effects.[1] The addition of SiH_4 as a reducing agent provides higher rates[11,12] of selective deposition even at temperatures as low as 300 °C, but often results in void formation.[14]

We report here the selective filling of trenches using CVD tungsten. By alternating the H_2 and SiH_4 reduction steps, the effects of the problems associated with each reducing agent are minimized. Using this process, feature sizes ranging from 1 μm down to 0.125 μm were filled. This process makes selective CVD tungsten an attractive technique for circuits with geometries in the range of 0.5 μm and below.

II. EXPERIMENTS AND RESULTS

The starting silicon wafers were *n*-type (100) with a resistivity of 5 Ω cm. A 550 nm thick layer of SiO_2 was thermally grown in steam at 950 °C, followed by the evaporation of a thin layer of Cr (typically 30 nm). Electron beam lithography, using a Perkin-Elmer MEBES-I with an accelerating voltage of 10 kV, was used to expose the patterns on 40 nm thick poly(methylmethacrylate) (PMMA). The PMMA layer needs to be thin in order to minimize the electron forward scattering in the resist, thus allowing the definition of 0.125 μm lines and spaces. The patterns in the PMMA were then transferred into the Cr by chemical etching in a Cyantek CR-14 solution for 40 s. After the removal of the PMMA, the SiO_2 was reactive ion etched, using the Cr layer as a mask, in a CHF_3/O_2 discharge using an Applied Materials AME 8100 etcher. The Cr layer provides a very good mask with a selectivity between SiO_2 and Cr of more than 50:1. The high selectivity seems to be improved due to the exposure of the Cr surface to oxygen during the reactive ion etching (RIE) of the SiO_2, possibly resulting in the formation of chromium oxides. The high etch selectivity eliminates the erosion of the Cr mask during the RIE, hence preventing the degradation of the sidewall angle of the trench. The Cr was stripped prior to the tungsten deposition in a CR-14 solution and the wafers were cleaned in HCl/H_2O_2 followed by a short etch in buffered HF (20:1) to remove the native oxide.

The tungsten was selectively deposited in a configured Genus-8402 cold wall reactor. A three-step process was used, starting with H_2 reduction followed by a step using a mixture of H_2 and SiH_4 and then finally a H_2 reduction step. The purpose of the first step is to provide a thin primary base layer free of voids often found when using SiH_4 reduction. The deposition time was limited to 60 s to minimize the encroachment and wormhole effects of H_2 reduction processes. The high deposition rate obtained in SiH_4 reduction is used in the second step to deposit thicker films in a relatively short time. The last step is used to eliminate any remaining unreacted SiH_4 and minimize void formation.[8] The deposition

TABLE I. Process conditions for the three-step process ($H_2/SiH_4/H_2$ reduction).

	H_2 reduction	SiH_4 reduction	H_2 reduction
Step (No.)	1	2	3
H_2 flow (sccm)	2000	2000	2000
SiH_4 flow (sccm)	···	20	···
WF_6 flow (sccm)	100	100	100
Pressure (mT)	200	200	200
Temperature (°C)	300	300	300

temperature was 300 °C in order to reduce the thermal stresses that arise due to the difference between the thermal expansion coefficients of tungsten and silicon. The pressure during the deposition process was kept at 200 mT. The gas flows and process conditions are summarized in Table I. The deposition rate in the second step was approximatley 30 nm/min.

The resistivity of the tungsten film was measured in large areas using a four-point microprobe and was found to be 20 $\mu\Omega$ cm for a 0.5 μm thick film.

Trenches of various widths and spacings were fabricated. Figures 1(a)–1(d) show trenches 1, 0.5, 0.25, and 0.125 μm wide, respectively. The trenches in the SiO_2 have been filled with tungsten to a thickness of 0.5 μm; a high deposition selectivity was observed even in the densely patterned 0.125 μm trenches. The grain size appears to be dependent on the trench width, shrinking with decreasing widths. However, the grain size difference between trenches of different widths did not affect the thickness uniformity across the wafer. The columnar growth is observed in all the trenches; for the 0.125 and 0.25 μm wide trenches, it is restricted to two pillars, which resulted in the formation of voids in the 0.125 μm wide trenches. These voids suggest that mass transport of reactants into the trenches becomes critical at sub-0.25 μm dimensions. This finding indicates that current deposition processes optimized for feature sizes larger than 0.75 μm may not be suitable for sub-0.25 μm features.

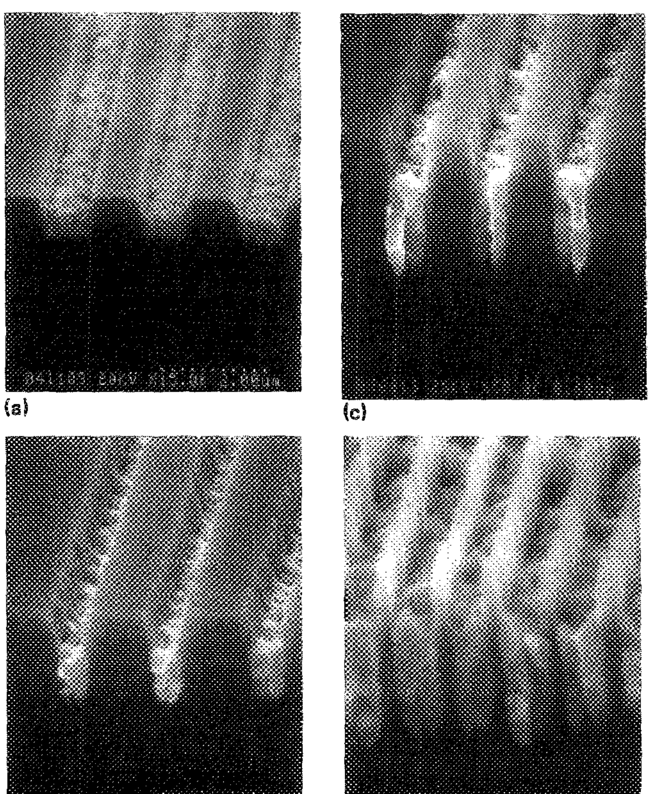

FIG. 1. Trenches of varying widths, (a) 1 μm, (b) 0.5 μm, (c) 0.25 μm, and (d) 0.125 μm, filled with tungsten. The patterns were defined in PMMA using electron beam lithography then transferred into a thin layer of Cr. The SiO_2 was reactive ion etched using the Cr as a mask. The tungsten was deposited selectively in a three-step process consisting of H_2 reduction of WF_6 followed by SiH_4 reduction then again H_2 reduction.

After the chemical etching of the Cr, a widening of the exposed lines on the order of 20 nm was observed because of the isotropic type of the etching solution. This effect is best observed in Fig. 1(d); the width of the trench and the spacing are approximately 150 and 90 nm, respectively. In addition, the etching process resulted in rough line-edges of the Cr layer. As a result of the high etch selectivity between the Cr mask and the SiO_2 during the RIE of the latter, these effects were replicated onto the trench profile as shown in Figs. 1(c) and 1(d).

III. SUMMARY

We reported the filling of trenches with feature sizes down to 0.125 μm, with selective CVD of tungsten. The grain size is a function of the trench width and the tungsten thickness is uniform across the wafer. The filled trenches indicate that CVD tungsten is useful for applications in scaled contacts and as absorber material in x-rays masks for the next generation of device groundrules of 0.5 μm and below. More work remains to be done to understand the effect of feature size on the deposition process and the properties of tungsten.

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