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Wafer-scale patterning of sub-40 nm diameter and high aspect ratio (>50:1) silicon pillar arrays by nanoimprint and etching

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Abstract

We demonstrate wide-area fabrication of sub-40 nm diameter, 1.5 μm tall, high aspect ratio silicon pillar arrays with straight sidewalls by combining nanoimprint lithography (NIL) and deep reactive ion etching (DRIE). Imprint molds were used to pre-pattern nanopillar positions precisely on a 200 nm square lattice with long range order. The conventional DRIE etching process was modified and optimized with reduced cycle times and gas flows to achieve vertical sidewalls; with such techniques the pillar sidewall roughness can be reduced below 8 nm (peak-to-peak). In some cases, sub-50 nm diameter pillars, 3 μm tall, were fabricated to achieve aspect ratios greater than 60:1.

(Some figures in this article are in colour only in the electronic version)

Nanopillars (i.e. vertical nanowires) perform key functions in many emerging technologies [1] with properties based on confinement effects [2] or large surface to volume ratios [3]. Arranging the nanowires vertically allows higher device densities and has been proposed for a broad range of applications in electronics [4, 5], optics [6], chemical synthesis and catalysis [7], and chemical and biological sensing [8]. Silicon nanowires are of particular interest because of their material and process compatibility with traditional integrated circuit devices (CMOS).

There are two principle routes to silicon nanowire fabrication: top-down lithography and etching, and bottom-up growth techniques. Top-down fabrication by standard reactive ion etching (RIE) can be used for high precision etching of submicron features, but high aspect ratios remain elusive, hampered by etch mask erosion during plasma bombardment. Submicron features have been etched by RIE to aspect ratios as high as 23:1 for 120 nm diameter pillars, but it was difficult to achieve non-tapered sidewalls in that process [9]. Pillar and grating structures have been etched using deep reactive ion etching (DRIE) to a ratio of 10:1, albeit with significant sidewall roughness and sidewall tapering [10]. Gratings with smoother sidewalls have been demonstrated using cryogenic etching [6] with liquid nitrogen cooled substrates. High aspect ratio gratings have been demonstrated by anisotropic wet chemical etching of silicon (111) planes [11], but pillar structures are not possible. Post-processing can further increase aspect ratios from the as-etched feature size by reducing the wire diameter with isotropic wet chemical etching [12] or with thermal oxidation of silicon followed by etch back with hydrofluoric acid [13].

Bottom-up fabrication of silicon pillars by vapor–liquid–solid growth has risen in popularity as a low-cost alternative to lithography and etching, and is capable of dense, high aspect nanowires with vertical sidewalls [14]. Several challenges remain to this approach. In particular, metal mediated nanowire growth is troublesome for silicon based electronics. For example gold, the most common and successful catalyst for silicon nanowire growth, introduces mid-bandgap trap states that seriously degrade device performance [15] and has led

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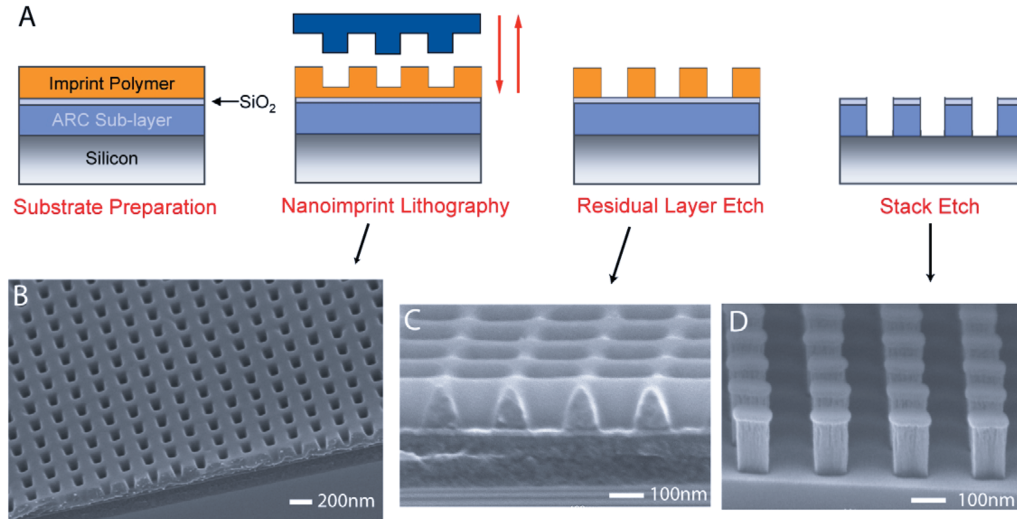

Figure 1. Schematics and scanning electron micrographs showing pre-patterning of a deep reactive ion etch (DRIE) mask by nanoimprint lithography (NIL). (a) The tri-layer imprint stack consists of spun-on imprint resist, evaporated SiO_2 as a thin supporting layer and a cross-linked ARC layer on a Si(100) substrate. (b) Imprint of 235 nm pitch pillar pattern by nanoimprint lithography in top imprint resist. (c) Residual layer etch by standard RIE and pattern inversion by metallization and lift-off using a thin (∼5 nm Cr). (d) RIE etched pillars on Si substrate that act as etch mask for etching of high aspect ratio nanopillars with optimized DRIE.

to the use of aluminum catalysts to grow silicon nanowires. However, these silicon nanowires grow preferentially as [111] and [110] wires and the growth of [100] nanowires remains difficult even when seeded on [100] oriented silicon substrates [16]. Recently, templated Si⟨100⟩ nanowire growth was demonstrated using gold catalysts in porous, anodized aluminum placeholders [17] or by direct etching of silicon using self-assembled diblock copolymer etch masking [18]. Unfortunately these templates, although they provide for very dense nanowire packing, lack long range order due to domain formation during self-assembly. The self-assembled templates also add fabrication complexity because they are not reusable. Other challenges for nanowire growth techniques include high temperature processing requirements in an ultra-high vacuum environment, wire placement, diameter uniformity and growth rate differences leading to inhomogenities in the final height of grown wires.

We present direct fabrication of vertical silicon nanowires by combining nanoimprint lithography (NIL) and DRIE to pattern wide-area (cm^2), high aspect ratio, [100] silicon pillar arrays directly in silicon (100) substrates. First a DRIE etching mask is pre-patterned by a nanoimprint process (mold fabrication and imprint and transfer into a tri-layer stack material) [19, 20] and second, by a DRIE plasma etch at room temperature to transfer the masked patterns into the bulk silicon substrate.

Nanoimprint lithography (NIL) is a next generation lithography solution for low-cost, wafer-scale nanopatterning [21] and has demonstrated sub-10 nm feature fidelity [22]. In NIL, an imprint mold is used to pattern a thin, curable polymer layer on a substrate. The polymer layer can be a functional material or act as an etch mask for transferring the pattern into the underlying substrate. Due to the high fidelity of the imprint process, features are replicated precisely and mold quality is critical to high-resolution nanoimprinting. Our imprint molds have 200 and 235 nm pitch pillar arrays covering 4 inch diameter silicon wafers. The pillar molds were fabricated using a daughter mold fabrication process where two cycles of nanoimprint lithography (including subsequent pattern transfer by standard RIE) are carried out with a one-dimensional (1D) grating mold. In the second cycle, the 1D grating mold was rotated 90° to create a two-dimensional (2D) array of pillars [23]. The original 1D grating mold was patterned on 4 inch diameter wafers by interference lithography [24]: UV interference lithography with a 351 nm Ar-ion laser source (SabreUV, Coherent) was used to make the initial 1D grating features in an i-line photoresist (AZ7905, AZ Electronic materials), part of a tri-layer resist stack which also included a thin, ∼15 nm layer of evaporated SiO_2 on top of a 180 nm thick UV absorbing ARC layer (xHiRC, Brewer Science). Following exposure and development, the 1D grating patterns were transferred through the resist stack and into the substrate and used to pattern the 2D pillar molds. After fabrication, the 2D pillar molds were surface treated using vapor phase deposition with NX-110 Mold Release Agent (Nanonex) to enhance separation after imprint.

These low aspect ratio (1:1), 2D pillar molds were used as masters to pre-pattern the silicon substrates for DRIE. High selectivity etching masks for DRIE are photolithography defined resist or silicon dioxide. Here NIL was used to pattern nanoscale features in thermal imprint resist, part of a multi-layer resist stack [25] shown in figure 1. The etch mask for the DRIE etching was a tri-layer resist stack which consists of a bottom layer of a 180 nm thick antireflection coating (ARC) (xHRic, Brewer Scientific) spun on a silicon wafer, a middle layer of evaporated SiO_2 (20 nm), and a top layer of 150 nm thick thermal imprint resist (NX-1020, Nanonex). The ARC layer is a cross-linked polymer layer typically used for planarization and fine feature control during

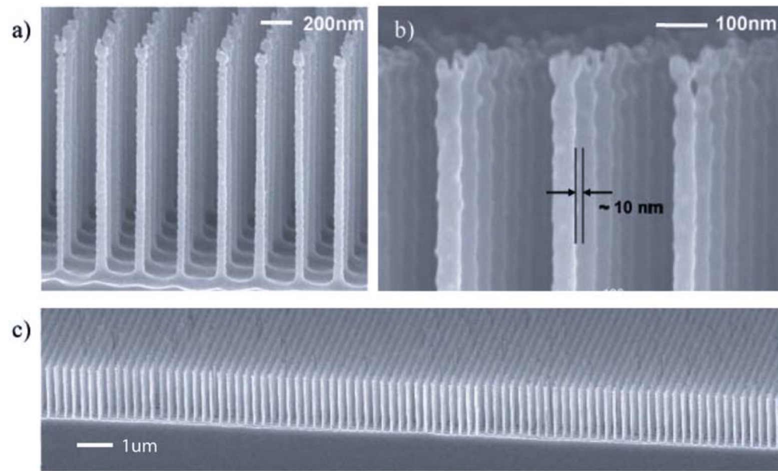

Figure 2. Direct etching results of arrays of vertical silicon (100) nanopillars using DRIE with an ARC etch mask. (a) Silicon nanopillars as narrow as 40 nm diameter and 1.5 μm tall with vertical sidewalls arrayed on an ordered 235 nm pitch grid. (b) Higher magnification view showing sidewall roughness less than 10 nm peak-to-peak. (c) Wide field view showing a large area array with long range order.

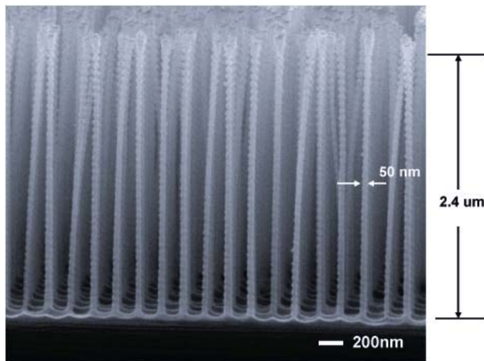

Figure 3. Direct etching of 50 nm diameter nanopillars precisely positioned on a 200 nm pitch grid and etched to a depth of 2.4 μm using 100 nm thick thermal SiO_2 in addition to the ARC etch mask layer. Sidewalls are vertical with ~15 nm sidewall scalloping.

photolithography. Here it was simply used as a cross-linked etch mask polymer with etch selectivity similar to photoresist. After imprint (Nanonex NX-2000), O_2 RIE was used to remove the residual imprint layer. Then the imprint resist was used as an image reversal mask using Cr evaporation and lift-off. A 5 nm thick Cr layer was deposited by electron beam evaporation followed by lift-off in acetone. The remaining Cr pads were used as a hard mask to pattern the evaporated SiO_2 layer by CFH_3/O_2 plasma RIE. The thin Cr layer was then removed using Cr-7 etchant. The ARC sub-layer was then etched by O_2 RIE down to the Si surface which acts as an etch stop. The nanopatterned ARC sub-layer, including the remaining SiO_2 cap, was used as the final etch mask for DRIE etching. As an additional option, the ARC layer was also used to further pattern a hard etch mask such as a thermal oxide layer grown on the silicon substrate. Finally, the sample wafers with nanopatterned DRIE etch masks were cleaved into smaller, ~1 cm^2 and greater pieces and mounted with thermal paste (AI Technologies, New Jersey) on 4 inch diameter silicon carrier wafers.

DRIE is a mainstay for micro electro mechanical systems (MEMS) and microfluidic device fabrication, enabling rapid etching of silicon with anisotropic etch profiles with high etch mask selectivity. Microstructures with vertical sidewalls are achieved using multiple cycles of the two-step Bosch process [26]. Short, approximately isotropic plasma etching of the silicon (SF_6/O_2) is followed by plasma deposition of fluoropolymer (C_4F_8) to passivate the sidewalls and suppress lateral etching of the silicon during the isotropic step. While overall etch results are anisotropic and vertical sidewalls the norm, the two stage etch results in the characteristic local *scalloping* of the sidewalls [26]. In standard high etch rate processes this scalloping is on the order of several hundred nanometers, enough to completely destroy nanoscale patterning. For microscale features, high aspect ratio trenches (5 μm wide $\times$ 200 μm deep) were demonstrated early on [26] and more recently nanoscale gratings [27] and pillar structures [10] have been etched successfully with aspect ratios approaching 5:1. We report aspect ratios as high as 60:1 for 50 nm diameter nanowires by using reduced cycle times and gas flows in a standard Bosch capable etcher (Multiplex ASE, Surface Technology Systems).

Etch results for 40 nm diameter and 1.5 μm high, silicon nanopillars are shown in figure 2 arranged on a wide-area, 235 nm square grid. The nanopillars were etched directly into the silicon (100) substrate and the wires were oriented along the $\langle 100 \rangle$ direction. The DRIE etching conditions using discrete switched parameters were as follows: *passivation*—85 sccm C_4F_8, 600 W coil, 5 s; *etching*—30 sccm SF_6, 6 sccm O_2, 2 sccm Ar, 600 W platen, 600 W coil, 7 s for 30 cycles. The respective cycle times were ramped, increased by 0.1 s per cycle as the etch continued. The pressure in the chamber was regulated by fixing the position of the gate valve (85% APC) to the turbo pump to achieve a nominal pressure of 20 mTorr. Backside helium cooling was also used to regulate substrate temperature drift, in order to limit Arrhenius effects in the temperature dependent chemical etching process.

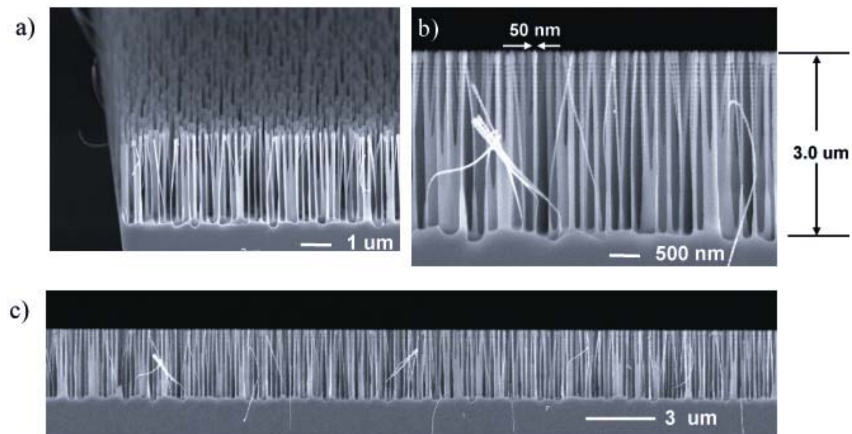

Figure 4. (a) Tilt SEM view of a forest of vertical silicon nanopillars etched to a nominal depth of 3 μm. Some nanowire branching and feature size etch rate dependence is evident, as is bowing of the high aspect ratio structures. (b) The labeled wire is $\sim$50 nm in diameter and 3 μm tall for an overall aspect ratio of $\sim$60:1.

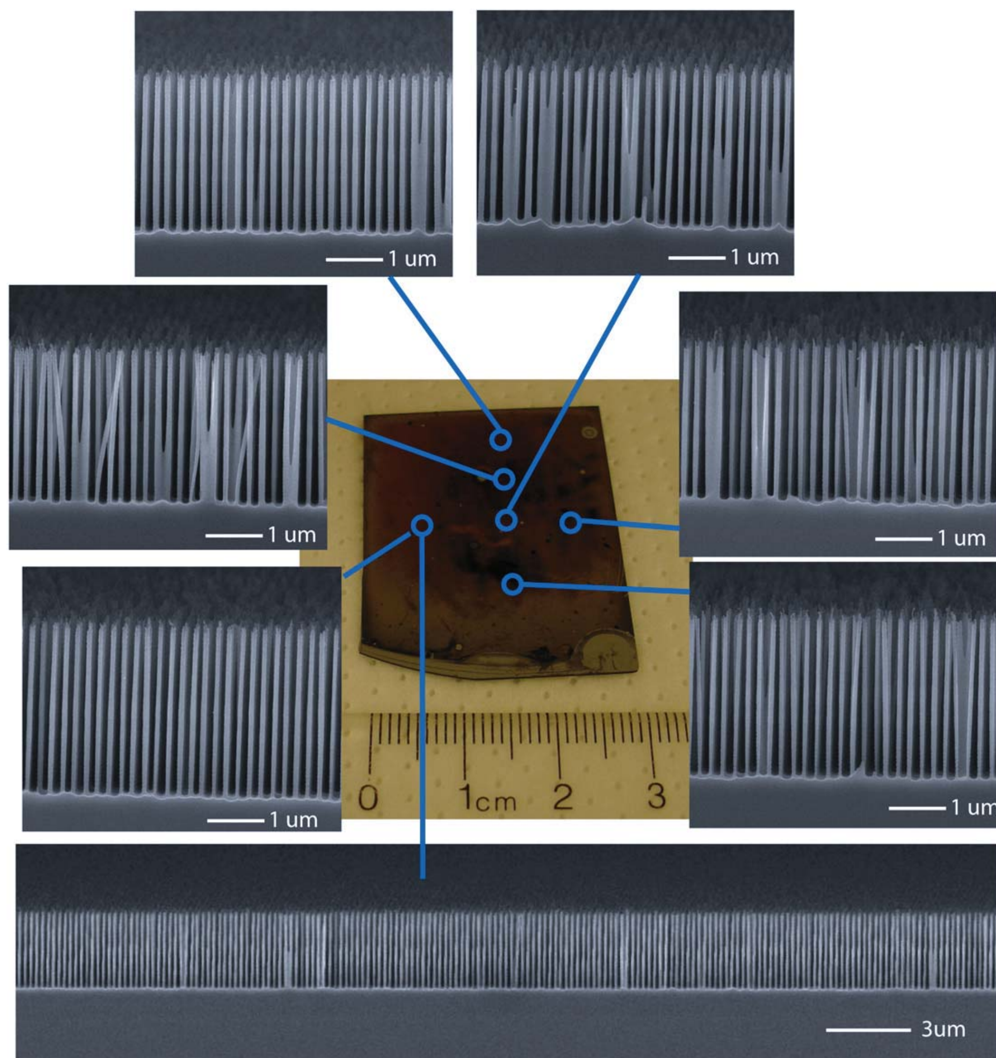

Figure 5. Comparison of the etch uniformity of $\sim$30:1 aspect ratio pillars across different regions of a 3 cm $\times$ 3 cm sample.

Note that with these parameters, sidewalls are vertical and all wires are etched to the same depth. Sidewall scalloping is just discernable using SEM (Zeiss/Leo 1550) and overall sidewall roughness (figure 2(b)) is on the order of 8 nm peak-to-peak. Some of the pillars are as narrow as 40 nm and wire to wire variation in diameter is from initial non-uniformities in the pre-patterned etch mask. Higher precision NIL master molds are possible using newly developed techniques to repair and perfect nanostructures by laser liquefaction [28].

High aspect etching of 50 nm diameter and 2.4 μm tall nanowires arrayed on a 200 nm square grid is shown in figure 3. The scalloping from the cyclic DRIE etch process is more pronounced and is approximately 15 nm peak-to-peak. The deeper etch (40 cycles) was possible by using a 100 nm thick thermal oxide as an etch mask, which can be made by transferring (RIE etching) the patterns in the ARC layer to the thermal oxide. The remaining ARC layer was left on the substrate for the DRIE etch. Slight bowing in the free standing silicon nanowires is also evident.

A large area (cm^2) forest of ultra-high aspect ratio silicon nanowires etched to a maximum depth of 3 μm is shown in figure 4. Further etching amplifies small differences in the original nanopatterned substrate because DRIE is prone to feature size dependent etch rates, leading to non-uniform etch depths and some branching. Some of the single, detached wires etched to the full 3 μm depth are as narrow as 40 nm for a total aspect ratio greater than 60:1. Lastly in figure 5, the wafer-scale uniformity of the etch process is examined. A 3 cm $\times$ 3 cm sample with pillars arrayed on a 200 nm pitch grid is shown after DRIE etching. Here the aspect ratios are greater than 30:1. Visually the sample appears slightly mottled with darker patches. The left-hand side being the most uniform and also having the most uniform pillars. The pillar diameters vary between 80 and 95 nm and etch depths vary between 2.7 and 2.9 μm from region to region. Again self-repair techniques to homogenize the etch mask pattern would improve the diameter uniformity.

In summary, we have demonstrated direct, high aspect ratio etching of silicon (100) nanowires with vertical sidewalls. We combined precision pre-patterning by nanoimprint lithography and optimized DRIE to achieve aspect ratios as high as 60:1 for 50 nm diameter wires. Direct etching of crystalline silicon provides a CMOS compatible route to vertical silicon nanowire transistors and other potential applications. Nanoimprint lithography allows low-cost patterning of dense, precisely positioned structures. In combination with deep reactive etching, the nanowires can be made in any Si substrate at low processing temperatures and with high aspect ratios, uniform wire widths and straight sidewalls. Additional etch process optimization and self-repair of the nanoimprint master molds should yield further improvements in diameter uniformity. Post-processing of the etched structures through self-limiting thermal oxidation or wet etching could also be used to fine tune the wire characteristics to further reduce the nanowire diameter.

References

[1] Cui Y and Lieber C M 2001 Functional nanoscale electronic devices assembled using silicon nanowire building blocks *Science* **291** 851–3

[2] Adu K W *et al* 2005 Confined phonons in Si nanowires *Nano Lett.* **5** 409–14

[3] Talin A A *et al* 2006 Large area, dense silicon nanowire array chemical sensors *Appl. Phys. Lett.* **89** 153102

[4] Schmidt V *et al* 2006 Realization of a silicon nanowire vertical surround-gate field-effect transistor *Small* **2** 85–8

[5] Goldberger J *et al* 2006 Silicon vertically integrated nanowire field effect transistors *Nano Lett.* **6** 973–7

[6] Hosomi K *et al* 2006 Ultrahigh-aspect-ratio, SiO_2 deeply etched periodic structures with smooth surfaces for photonics applications *J. Vac. Sci. Technol.* B **24** 1226–9

[7] Contreras A M *et al* 2005 Fabrication of platinum nanoparticles and nanowires by electron beam lithography (EBL) and nanoimprint lithography (NIL): comparison of ethylene hydrogenation kinetics *Catal. Lett.* **100** 115–24

[8] Cui Y *et al* 2001 Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species *Science* **293** 1289–92

[9] Chang Y F *et al* 2007 Fabrication of high-aspect-ratio silicon nanopillar arrays with the conventional reactive ion etching technique *Appl. Phys.* A **86** 193–6

[10] Choi C H and Kim C J 2006 Fabrication of a dense array of tall nanostructures over a large sample area with sidewall profile and tip sharpness control *Nanotechnology* **17** 5326–33

[11] Yu Z N *et al* 2003 Fabrication of nanoscale gratings with reduced line edge roughness using nanoimprint lithography *J. Vac. Sci. Technol.* B **21** 2089–92

[12] Fischer P B and Chou S Y 1993 Sub-50 nm high aspect-ratio silicon pillars, ridges, and trenches fabricated using ultrahigh resolution electron-beam lithography and reactive ion etching *Appl. Phys. Lett.* **62** 1414–6

[13] Liu H I *et al* 1994 Self-limiting oxidation for fabricating sub-5 nm silicon nanowires *Appl. Phys. Lett.* **64** 1383–5

[14] Hochbaum A I *et al* 2005 Controlled growth of Si nanowire arrays for device integration *Nano Lett.* **5** 457–60

[15] Wang Y W *et al* 2006 Epitaxial growth of silicon nanowires using an aluminium catalyst *Nat. Nanotechnol.* **1** 186–9

[16] Schmidt V, Senz S and Gosele U 2005 Diameter-dependent growth direction of epitaxial silicon nanowires *Nano Lett.* **5** 931–5

[17] Shimizu T *et al* 2007 Synthesis of vertical high-density epitaxial Si(100) nanowire arrays on a Si(100) substrate using an anodic aluminum oxide template *Adv. Mater.* **19** 917

[18] Zschech D *et al* 2007 Ordered arrays of ⟨100⟩-oriented silicon nanorods by CMOS-compatible block copolymer lithography *Nano Lett.* **7** 1516–20

[19] Chou S Y, Krauss P R and Renstrom P J 1995 Imprint of sub-25 nm vias and trenches in polymers *Appl. Phys. Lett.* **67** 3114–6

[20] Chou S Y, Krauss P R and Renstrom P J 1996 Imprint lithography with 25-nanometer resolution *Science* **272** 85–7

[21] Gao H 2006 Air cushion press for excellent uniformity, high yield, and fast nanoimprint across a 100 mm field *Nano Lett.* **6** 2438–41

[22] Austin M D *et al* 2004 Fabrication of 5 nm linewidth and 14 nm pitch features by nanoimprint lithography *Appl. Phys. Lett.* **84** 5299–301

[23] Kwon S *et al* 2005 Fabrication of metallic nanodots in large-area arrays by mold-to-mold cross imprinting (MTMCI) *Nano Lett.* **5** 2557–62

[24] Savas T A *et al* 1995 Achromatic interferometric lithography for 100 nm-period gratings and grids *J. Vac. Sci. Technol.* B **13** 2732–5

[25] Savas T A *et al* 1996 Large-area achromatic interferometric lithography for 100 nm period gratings and grids *J. Vac. Sci. Technol.* B **14** 4167–70

[26] Ayon A A *et al* 1999 Characterization of a time multiplexed inductively coupled plasma etcher *J. Electrochem. Soc.* **146** 339–49

[27] Wang X *et al* 2007 High aspect ratio Bosch etching of sub-0.25 μm trenches for hyperintegration applications *J. Vac. Sci. Technol.* B **25** 1376–81

[28] Xia Q and Chou S Y 2007 Perfecting Si and metal nanostructures using guided self-perfection by liquefaction (G-SPEL) *Proc. 51st Int. Conf. on Electron, Ion and Photobeam Technology and Nanofabrication*