Improved nanofabrication through guided transient liquefaction

STEPHEN Y. CHOU* AND QIANGFEI XIA

NanoStructure Laboratory, Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544, USA
*e-mail: chou@ee.princeton.edu

Published online: 4 May 2008; doi:10.1038/nnano.2008.95

A challenge in nanofabrication is to overcome the limitations of various fabrication methods, including defects, line-edge roughness and the minimum size for the feature linewidth. Here we demonstrate a new approach that can remove fabrication defects and improve nanostructures post-fabrication. This method, which we call self-perfection by liquefaction, can significantly reduce the line-edge roughness and, by using a flat plate to guide the process, increase the sidewall slope, flatten the top surface and narrow the width while increasing the height. The technique involves selectively melting nanostructures for a short period of time (hundreds of nanoseconds) while applying a set of boundary conditions to guide the flow of the molten material into the desired geometry before solidification. Using this method we reduced the 3σ line-edge roughness of 70-nm-wide chromium grating lines from 8.4 nm to less than 1.5 nm, which is well below the 'red-zone limit' of 3 nm discussed in the International Technology Roadmap for Semiconductors. We also reduced the width of a silicon line from 285 nm to 175 nm, while increasing its height from 50 nm to 90 nm. Self-perfection by liquefaction can also be extended to other metals and semiconductors, dielectrics and large-area wafers.

Traditionally, we improve the shape of a fabricated nanostructure by improving the fabrication method (various lithography, etching and deposition techniques) that was used to make the nanostructure[1]. However, this approach might no longer work when the feature size approaches the limitation of the fabrication method used[2]. Limitations include fabrication defects (such as deviations in shape from the intended design) as well as the minimum sizes for the various dimensions of the nanostructure. When feature sizes in a device are small enough, the fabrication defects in many nanofabrication methods can become a dominant factor that determines the actual shape of the nanostructure. Although extrinsic defects can be removed by improving the process, intrinsic defects caused by the fundamental statistical nature of a fabrication process (for example, noise in photon, electron or ion generation, scattering, and variations in chemical reaction) cannot be removed. The minimum linewidth and line height are often determined by the fundamental working principle of a fabrication, and are fixed once a fabrication method is selected. Fabrication defects can degrade or even destroy the operation of a wide variety of nanodevices in electronics[3,4], photonics[5], magnetic systems[6–8], biotechnology[9] and other applications. The minimum linewidth and line height can also limit device density and performance.

Rather than improving a nanostructure by improving its original fabrication method, here we demonstrate a new method, known as self-perfection by liquefaction (SPEL), which removes nanostructure fabrication defects and improves nanostructures after fabrication. This process is capable of removing both intrinsic and extrinsic defects, and also of forming new shapes that may not be achievable using conventional fabrication techniques. The method, which selectively melts nanostructures for a short period of time (hundreds of nanoseconds) while applying a set of boundary conditions to guide the flow of the molten materials into the desired geometry before solidification, has three basic forms (Fig. 1): open-SPEL, capped-SPEL and guided SPEL.

For open-SPEL, the nanostructures are located on a substrate without any additional boundary conditions. When melted into a liquid phase, the nanostructure flows under the influence of surface tension and interaction with the substrate, smoothing out the structure's rough edges. The flow can also cause a non-circular dot to become a near-perfect circular dot. Open-SPEL is similar to the well-known thermal flow of low-glass-transition-temperature ($\sim$100 °C) resist[10,11], except it uses a short pulse of surface heating to selectively melt hard semiconductors, metals or dielectrics of high melting temperatures ($\sim$1,000 °C or higher) to avoid damage to other parts of the devices or substrates. This means that open-SPEL suffers from the same drawbacks as ordinary thermal flow: widened line footprint and rounded sidewalls and top-surface. To overcome these problems, we propose the use of guiding during melting to reshape a structure, as discussed in the following.

In capped-SPEL, a single flat, transparent non-melting plate (such as quartz) is placed in contact with the top of all the structures to be improved, or one plate is placed on the top of each structure. During the melting, self-perfection is controlled by the surface tension of the molten material and the interaction of the molten material with the substrate and the top plate(s). The top plate(s) controls the top surface flatness, sidewall angle and triple phase line of the molten nanostructure. Capped-SPEL not only smoothes the sidewalls, it also makes the sidewalls vertical and the top flat.

In guided-SPEL, a flat plate is placed above the structures that are to be improved, with a gap between the plate and the nanostructure. The interaction between the structures and the top plate can make the molten structure rise up (against the liquid surface tension) to reach the top plate and, in the process,

© 2008 Nature Publishing Group

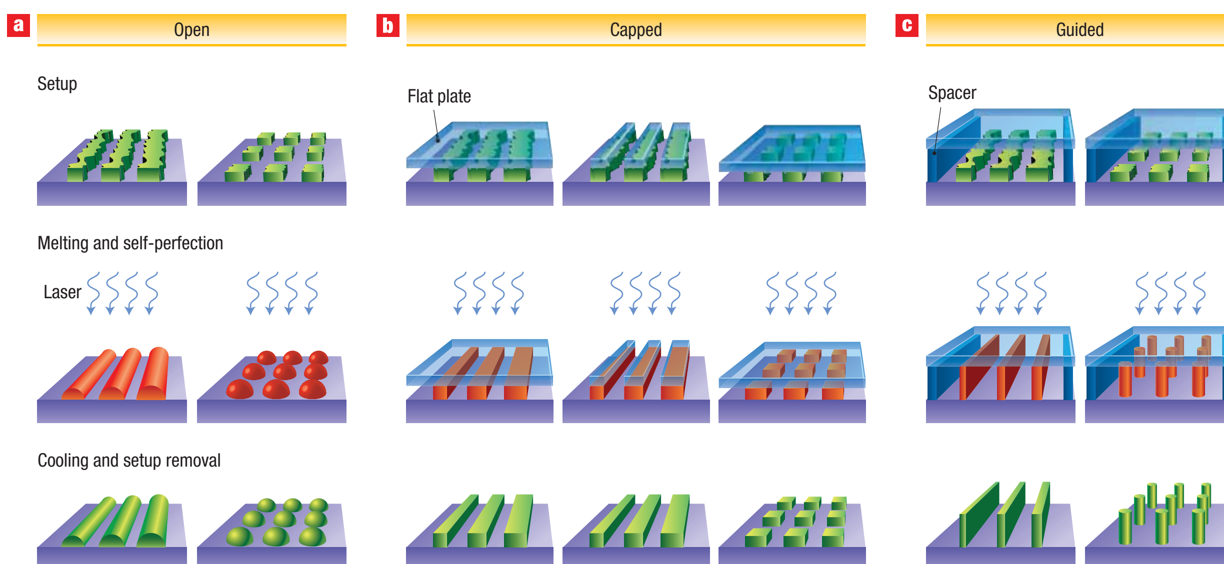

Figure 1 Working principle of three forms of self-perfection by liquefaction (SPEL). a–c, Open-SPEL (**a**), capped-SPEL (**b**) and guided-SPEL (**c**) for lines and squares (or dots). SPEL selectively melts nanostructures (for example, silicon or chromium) for a short period of time (hundreds of nanoseconds) while applying a set of boundary conditions (for example, one or more plates placed in contact or a gap above) to guide the flow of the molten material into a desired geometry before solidification. SPEL can significantly reduce the LER, can increase the sidewall slope and flatten the top surface (capped- and guided-SPEL), and, moreover, narrow the width while increasing the height (guided-SPEL).

form a new shape, leading to a greater height and a narrower linewidth (through conservation of volume), in addition to smooth edges, vertical sidewalls and a flat top.

In SPEL, heating can be provided by a pulsed laser of a certain wavelength with either a flood or masked beam, which selectively deposits a very small amount of energy to melt the desired material while keeping the materials under and near the structures at a low temperature and in the solid phase. Both pulsed and continuous-wave lasers have been used previously to melt materials for surface planarization[12,13], edge roughness smoothing of optical disks (100 μm diameter)[14], crystal growth[15] and direct imprinting[16].

APPLYING SPEL TO METALS AND SEMICONDUCTORS

We have demonstrated the three forms of SPEL in various materials, including metals, semiconductors and polymers. The main results for metals and semiconductors are summarized in Table 1. The figures of merit in line-edge roughness (LER) are the standard deviation σ and the correlation length ξ, both of which are determined by fractal analysis[17] of digitized scanning electron microscopy (SEM) images. All of our experiments used a 20-ns excimer ($\lambda = 308$ nm) laser pulse with a variable fluence. In open-SPEL with a fluence of 320 mJ cm^{-2} it was possible to reduce the 3σ-LER of 70-nm-wide, 40-nm-high chromium

Table 1 The measured 3σ-LER and correlation length ξ before and after SPEL. Analysis of SEM images of the chromium and silicon grating lines before and after open-, capped- and guided-SPEL show that SPEL can reduce 3σ-LER to well below the 3-nm 'red-zone limit'.

Samples		Image resolution (nm/pixel)	3σ (nm)	Improvement (%)	ξ (nm)	Laser fluence (mJ cm^{-2})
Open-SPEL						
70-nm-wide Cr lines on SiO_2 (Fig. 2a,b)	Original	0.43	8.4		281.7	
	After		1.5	560	387.6	320
70-nm-wide Si lines on SOI (Fig. 2c,d)	Original	1.7	19.5		30.0	
	After		3.6	542	60.0	545
70-nm-wide Si lines on Si (Fig. 2e,f)	Original	0.43	14.4		19.6	
	After		3.3	436	216.6	440
250-nm-wide Si lines on Si (Fig. 2g,h)	Original	1.7	9.6		23.0	
	After		4.2	228	38.9	880
Capped-SPEL						
280-nm-wide Si lines on SiO_2 (Fig. 4a,b)	Original	1.7	9.6		17.7	
	After		4.2	228	35.4	480
200-nm-wide Si lines on Si (Fig. 4c,d)	Original	1.7	11.1		37.2	
	After		5.4	205	125.6	390
280-nm-wide Cr lines on SiO_2 (Fig. 4e,f)	Original	3.4	17.7		27.6	
	After		7.5	236	117.3	406
Guided-SPEL						
280-nm-wide Cr lines on SiO_2 (Fig. 5a,b)	Original	3.4	17.4		24.1	
	After		5.4	322	79.3	406

© 2008 Nature Publishing Group

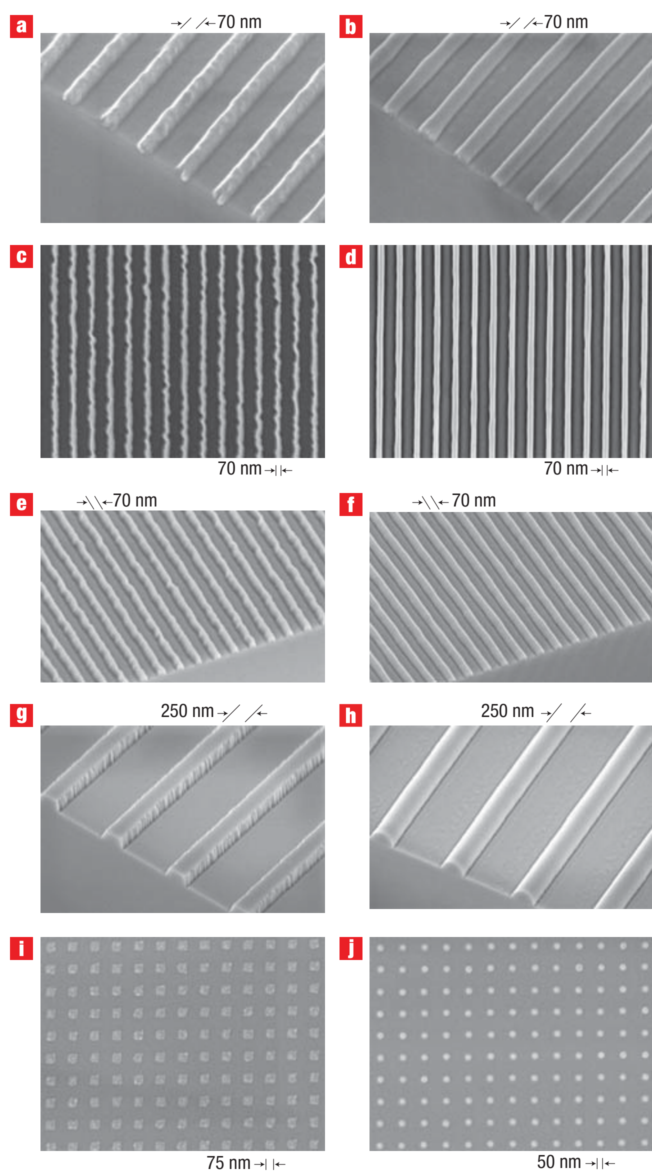

Figure 2 SEM images of various nanostructures before (left panels) and after (right panels) treatment with open-SPEL with a single excimer laser pulse. **a**,**b**, Chromium lines (70 nm wide and 40 nm high) SiO_2 substrate before (**a**) and after (**b**) open-SPEL. **c**,**d**, Silicon lines (70 nm wide) on SOI before (**c**) and after (**d**) open-SPEL. **e**,**f**, Silicon lines (70 nm wide) on silicon before (**e**) and after (**f**) open-SPEL. **g**,**h**, Silicon lines (250 nm wide and 150 nm high) on a silicon surface before (**g**) and after (**h**) open-SPEL. It can be clearly seen that open-SPEL reduces the LER of these structures. **i**,**j**, Open-SPEL can reduce 75 × 75 nm chromium squares on an SiO_2 surface (**i**) to dots with diameters of 50 nm (**j**).

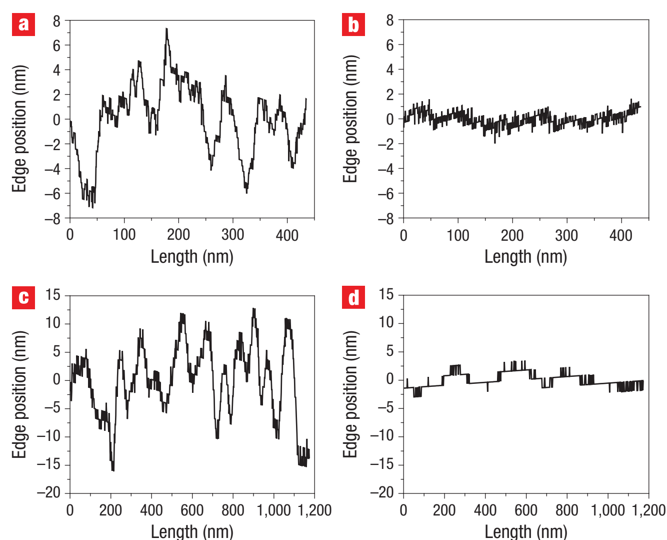

Figure 3 The edge profiles of some of the silicon and chromium lines from Fig. 2 before (left panels) and after (right panels) treatment with open-SPEL as measured in SEM images. **a**,**b**, The edge profiles for the 70-nm chromium lines before (**a**) and after (**b**) open-SPEL. **c**,**d**, The edge profiles for the 70-nm silicon lines (on SOI) before (**c**) and after (**d**) open-SPEL. Open-SPEL reduces the 3σ-LER of the 70-nm chromium line to below 1.5 nm, which is of the same order as the noise from the SEM imaging. (Note that the high-frequency noise in all the SEM images is the noise associated with the SEM imaging process itself, and not the actual LER).

grating lines on SiO_2 (Fig. 2a,b) from 8.4 nm to 1.5 nm, representing a reduction of 560% (defined as $\sigma_{\text{initial}}/\sigma_{\text{final}}$), and the value of ξ increased significantly (indicating the removal of high-spatial-frequency components of LERs). Considering the 0.43 nm/pixel resolution and other measurement noise in SEM images, the actual 3σ-LER of the chromium lines after open-SPEL should be much less than 1.5 nm, and hence well below the red-zone limit (3 nm) that was previously thought unachievable[2].

To further illustrate the LER improvements, the edge profiles before and after open-SPEL are compared in Fig. 3.

To test open-SPEL effectiveness in semiconductors, we created 70-nm-wide silicon grating lines with severe edge roughness, which had line heights of 100 nm on silicon-on-insulator (SOI) wafers and 70 nm on silicon wafers (Fig. 2c,e). After open-SPEL (a single pulse of 545 and 440 mJ cm^{-2} fluence, respectively), the zigzag edges were smoothed significantly (Fig. 2d,f). The 3σ-LERs were reduced from 19.5 nm to 3.6 nm and from 14.4 nm to 3.3 nm, respectively, corresponding to LER reductions of 542% and 436%. For 250-nm-wide silicon grating lines of silicon substrate, open-SPEL with one single pulse can reduce the 3σ-LER from 9.6 nm to 4.2 nm (Fig. 2g,h). The LERs could be further reduced by using a higher fluence or multiple laser pulses. For chromium squares that were 10 nm thick, with an area of 75 nm × 75 nm and rough edges, a single laser pulse (1.7 J cm^{-2}) turned the squares into nearly perfectly rounded dots with a diameter of 50 nm and height of 22 nm (Fig. 2i,j). The experiments also show that open-SPEL can round the sidewalls and top surface, and also widen the line footprint.

In capped-SPEL a plate is placed in contact with the top surface of the structure to be improved to keep the top surface flat and sidewalls vertical during the melting process. Capped-SPEL may also be able to keep the corners of a rectangular-shaped profile sharp if the triple phase lines of a molten material can be pinned on the plate. Figure 4 shows the SEM images before and after capped-SPEL (using a single laser pulse) of 280-nm-wide silicon lines on a silicon substrate guided by a single quartz plate (Fig. 4a,b), 200-nm-wide silicon lines on a silicon surface guided by individual caps (chromium/SiO_2, one on each line) (Fig. 4c,d), and 280-nm-wide chromium lines on an oxide surface guided by a single quartz plate (Fig. 4e,f). After

© 2008 Nature Publishing Group

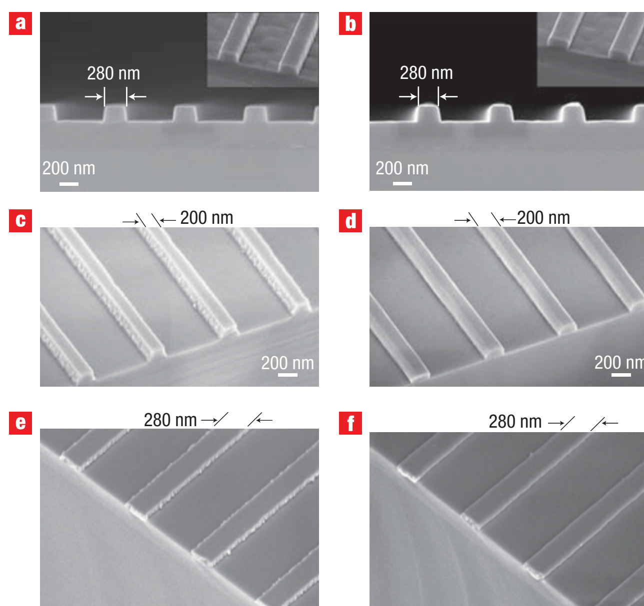

Figure 4 SEM images of silicon and chromium lines before (left panels) and after (right) treatment with capped-SPEL. **a**,**b**, Silicon lines (280 nm wide) before (**a**) and after (**b**) capped-SPEL with a single flat plate. **c**,**d**, Silicon lines (200 nm wide) before (**c**) and after (**d**) capped-SPEL with one chromium/SiO_2 cap on each silicon line. **e**,**f**, Chromium lines (280 nm wide) before (**e**) and after (**f**) capped-SPEL with a single flat plate. Capped-SPEL reduces the LER and also flattens the top and the side walls of the features.

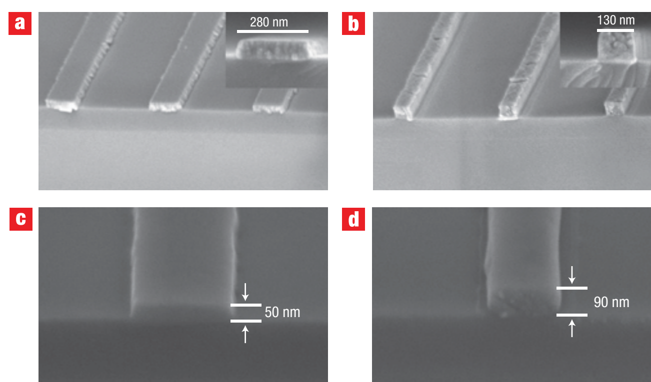

Figure 5 SEM images of chromium and silicon lines on SiO_2 substrates before (left panels) and after (right panels) treatment with SPEL with a single quartz plate guiding the process. **a**,**b**, In guided-SPEL with a 70-nm gap, the original chromium lines are 280 nm wide and 62 nm high **(a)**; after processing they are 130 nm wide and 130 nm tall **(b)**, which means that the aspect ratio has been increased by a factor of 4.5. **c**,**d**. In guided-SPEL with a 40 nm gap, the original silicon lines are 285 nm wide and 50 nm high (**c**); after processing they are 175 nm wide and 90 nm high (**d**).

capped-SPEL, the tops of these structures were flat and their sidewalls vertical. A fractal analysis of the SEM images shows that the 3σ-LER was reduced from 9.6, 11.1 and 17.7 nm to 4.2, 5.4, and 7.5 nm, respectively, achieving improvements of 228%, 205% and 236%.

In guided-SPEL, local spacers are used to keep a plate fixed above the nanostructures (Fig. 1), and surface tension causes the molten nanostructures to rise until they reach the plate. This leads to smooth edges, vertical sidewalls and flat tops, and also to narrower linewidths and greater line heights (and hence higher aspect ratios) than the original structures. The entire melting, rising-up and reshaping took less than 200 ns for silicon and chromium materials. Figure 5 shows chromium and silicon lines before and after guided-SPEL with a single quartz plate guide and a single laser pulse. Chromium lines on an SiO_2 surface were originally 280 nm wide and 62 nm tall, but after guided-SPEL (with a 70-nm gap between the original pattern and the plate, and a single 406 mJ cm^{-2} pulse) they were 130 nm wide (215% width reduction, defined as $W_{\text{initial}}/W_{\text{final}}$) and 130 nm tall (equal to the original height plus the gap, 210% of the original height, defined as $H_{\text{final}}/H_{\text{initial}}$), and hence had a 452% increase in aspect ratio. The width and height of a line should be reduced and increased respectively by the same factor, due to conservation of the material volume. The 3σ-LER was reduced from 17.4 nm to 5.4 nm (322% reduction). The silicon lines on an SiO_2 substrate were originally 285 nm wide and 50 nm tall, but after guided-SPEL (using a 40 nm gap and a 595 mJ cm^{-2} pulse) they were 175 nm wide and 90 nm tall (170% improvement).

We find that the sidewall angle is almost 90° for both silicon and chromium, which is in line with theoretical predictions for silicon but much less than the value of $\sim$130° predicted for molten chromium on SiO_2. One possible reason for this is that the charges generated in SPEL can modify the contact angle in a similar fashion to electrical wetting, which reduces the contact angle (Lippmann's equation). The local spacers for precisely controlling the gap were microfabricated on the top plate.

Furthermore, when applying open- or guided-SPEL to small chromium or silicon squares, they changed to having a nearly perfect round shape (semispheres or cylinders). Chromium squares that were originally 140 nm $\times$ 110 nm in size and 20 nm in height (Fig. 6a) became semispheres with a diameter of 80 nm and a height of 48 nm after open-SPEL with a 400 mJ cm^{-2} pulse (Fig. 6b), and became cylinders with a diameter of 70 nm and a height of 62 nm (310% of the original height), complete with vertical sidewalls and a flat top, after guided-SPEL with a 40-nm gap and the same laser fluence as the open-SPEL (Fig. 6c). Similarly, for the silicon squares (90 nm $\times$ 100 nm and a height of 50 nm; Fig. 6d), open-SPEL caused them to become semispheres with a diameter of 85 nm and a height of 62 nm (Fig. 6e), and guided-SPEL (with a 23-nm gap) made them into cylinders with a diameter of 78 nm and a height of 73 nm (150% of the original height), again with vertical sidewalls and a flat top (Fig. 6f).

SMOOTHING, THE ORIGIN OF GUIDED-SPEL AND SCALING

The fact that the edge-roughness smoothing-out time in molten silicon and chromium is approximately in the hundreds of nanoseconds rather than seconds or minutes can be explained by their high surface tension and low viscosity. Using Stokes–Navier equations and the continuity equation, the time T for smoothing a structure's topological variation of a spatial period λ and a height h on a two-dimensional liquid surface is proportional to the molten material viscosity and is inversely proportional to the surface tension[18]:

$$T = \frac{3\eta\lambda^4}{16\pi^4\gamma h^3}$$

Compared with a molten polymer, the molten chromium and silicon have viscosities η that are $\sim$100–1,000,000 times lower

© 2008 Nature Publishing Group

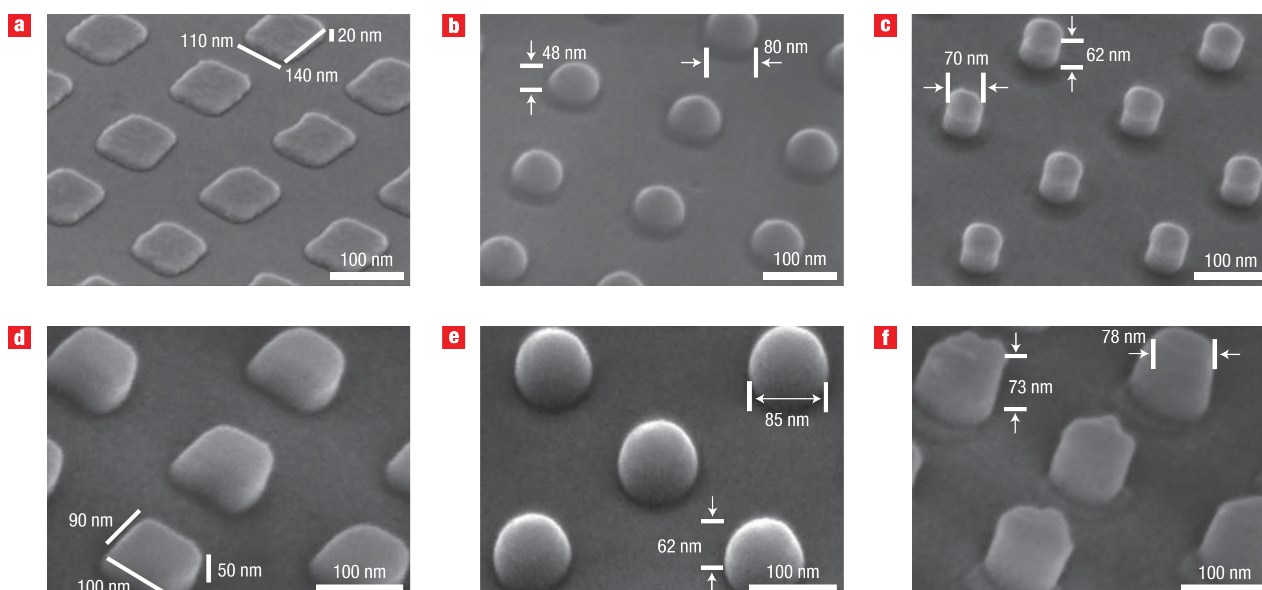

Figure 6 SEM images of various nanostructures before and after open- and guided-SPEL. a–c, As-fabricated chromium squares (**a**) become semispheres after open-SPEL (**b**) or cylinders after guided-SPEL (**c**) with a 40-nm gap. **d–f**, As-fabricated silicon squares (**d**) become semispheres after open-SPEL (**e**) or cylinders after guided-SPEL (**f**) with a 22 nm gap. The dimensions of all the nanostructures are given in the images.

and surface tensions γ that are 20–100 times higher, leading to a smoothing time that is 3–8 orders of magnitude shorter. For example, for smoothing $\lambda = 1\ \mu$m in a 50-nm-thick film, it would take 52 ns, 16 ns and 51 s for molten chromium, silicon and PMMA, respectively (assuming η is 100,000 mPa·s for softened PMMA). The short processing time of SPEL reduces or eliminates degradation of other structures adjacent and under the structures that are being perfected.

The mechanism of guided-SPEL is not entirely clear. Previously, a self-rise-up of a material located under a plate with a gap was observed only in a featureless molten-polymer thin film ($\sim$100 °C glass-transition temperature)[19,20] and was attributed to an electrostatic interaction between the plate and the molten material and electrohydrodynamic instability in liquid[19–21]. However, a self-rise-up in molten silicon and chromium was unexpected and had not been observed previously, because silicon and chromium have surface tensions much higher (over 20 times) than molten polymers (1,642, 720 and 30 mN·m^{-1} for molten chromium[22], silicon[23] and polymer, respectively). The high surface tension would require much stronger pulling force. Using the Stokes–Navier equations and the continuity equation, the analytical equation of the time t for a polymer to rise up under a potential difference between the molten material and the plate, $\Delta\phi$, is given by[21]

$$t = \frac{\eta\gamma d^3}{\varepsilon_0^2(\Delta\phi)^4}$$

where d is the initial gap between the material and the top plate (hence an electric field of $\sim\Delta\phi/d$) and $\varepsilon_0 = 8.85\times10^{-12}\ \mathrm{C^2\,N^{-1}\,m^{-2}}$ is vacuum permittivity. For $t \approx 200$ ns (observed in guided-SPEL), viscosity $\eta \approx 5.7$ mPa·s for molten chromium[24] and 0.58 mPa·s for molten silicon[25] (slightly lower than water, at 1 mPa·s), and $d \approx 70$ nm (chromium) and 40 nm (silicon), this requires values of $\Delta\phi$ of 22 and 7 V for guided-SPEL in chromium and silicon, respectively. The $\Delta\phi$ from theory is clearly much larger than our experiments where the $\Delta\phi$ is <3 eV. This implies that the analytical model for polymers is insufficient to describe the guided-SPEL of molten silicon and chromium, and new boundary conditions or numerical simulations may be needed.

SPEL can be scaled to large-area wafers (more than 8 in. diameter) by precisely controlling the gap between a wafer and the plate. This can be achieved over a large area by using local spacers to regulate the local gap between the SPEL plate and the substrate, a relatively flexible plate to allow it to conform to the contours of the wafer surface, and an air cushion press[26] to supply a uniform constant pressure over the entire plate.

It should be pointed out that the boundary conditions and processing parameters used in our current SPEL experiments serve only as examples, and many variations can be used. For example, different surface properties (such as the substrate, top plate or the structure) can be modified to control the final SPEL structure geometries. We found that SPEL also works for polymeric materials, but that much longer processing times (of the order of seconds and minutes) are needed, and we also expect it to work for other insulators (providing they can be melted).

Finally, we should point out that SPEL does have limitations. For example, it cannot be applied when the dimensions of the defect are comparable with the dimensions of the nanostructure, and it cannot fix defects where the total materials are insufficient. Moreover, the ends of lines can become rounded in SPEL unless the triple phase line of a molten material can be pinned. (Fortunately, the operation of most electrical, optical, magnetic and biological devices does not depend upon the exact shape of a corner.) The effects of SPEL on complex structure shapes are yet to be studied. Under certain conditions, the instability in the liquid may play some adverse role and should be controlled. Despite these limitations, SPEL is expected to have wide applications in nanofabrication and nanomaterial processing.

© 2008 Nature Publishing Group

METHODS

SAMPLE PREPARATION

The samples were fabricated using nanoimprint lithography and etching or lift-off (described elsewhere[27]). The LER of the nanostructures in the original samples therefore arose primarily from the imprint mould (as imprinting duplicates the mould patterns into resist with nanometre fidelity), etching or lift-off. The edge roughness in our imprint mould was caused by interference lithography, metal deposition, lift-off, etching and other steps used in mould fabrication. The LERs in the samples used for Fig. 2c,e are far worse than normal, primarily because of a 'bad' imprint mould.

LASER MELTING

In our experiments, the melting was provided by a XeCl excimer laser with a wavelength of 308 nm, a fixed pulse duration of 20 ns, a 3 mm $\times$ 3 mm uniform beam size and an adjustable fluence. The laser beam was directly absorbed only by the materials having an energy bandgap smaller than the photon energy, and passed unabsorbed through materials with a larger bandgap. The XeCl excimer laser pulse could therefore selectively melt metals and semiconductors, but not SiO_2 (including quartz). Selective melting of certain areas of a wafer can be achieved using a mask (reflecting or absorbing) that is placed either directly on the wafer or a distance away. The melting time was measured by measuring the reflectivity change of a HeNe laser ($\lambda = 633$ nm) from the molten surface, using the fact that the reflectivity of a molten material is different from that of its solid phase[16,28,29]. Depending upon laser fluence, a single laser pulse can melt a semiconductor or metal surface with a depth of 50–300 nm within 1 ns and keep it molten for $\sim$200 ns (ref. 16).

LER MEASUREMENTS AND ANALYSIS

We used digitized SEM images and fractal analysis[17] to calculate the 3σ-LER and the parameter ξ (a measure of the spatial frequencies of the LER, where a higher ξ indicates less-high-frequency roughness). The typical line length over which the LER is averaged was 4–7 μm. The SEM images had a 0.43 nm/pixel resolution and contained other measurement noise.

Received 18 February 2008; accepted 1 April 2008; published 4 May 2008.

References

1. Marrian, C. R. K. & Tennant, D. M. Nanofabrication. *J. Vac. Sci. Technol. A* **21,** S207–S215 (2003).
2. International Technology Roadmap for Semiconductors, 2006 <www.itrs.net/reports.html>, Table 77b (2006).
3. Diaz, C. H. *et al*. An experimentally validated analytical model for gate line-edge roughness (LER) effects on technology scaling. *IEEE Electron. Dev. Lett.* **22,** 287–289 (2001).
4. Asenov, A., Kaya, S. & Brown, A. R. Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness. *IEEE Trans. Electron. Dev.* **50,** 1254–1260 (2003).
5. Lee, K. K., Lim, D. R., Kimerling, L. C., Shin, J. & Cerrina, F. Fabrication of ultralow-loss Si/SiO_2 waveguides by roughness reduction. *Opt. Lett.* **26,** 1888–1890 (2001).
6. Chou, S. Y. Patterned magnetic nanostructures and quantized magnetic disks. *Proc. IEEE* **85,** 652–671 (1997).
7. Wasilewski, Z. R., Fafard, S. & McCaffrey, J. P. Size and shape engineering of vertically stacked self-assembled quantum dots. *J. Cryst. Growth* **201/202,** 1131–1135 (1999).
8. Fang, W., Cao, H. & Solomon, G. S. Control of lasing in fully chaotic open microcavities by tailoring the shape factor. *Appl. Phys. Lett.* **90,** 081108 (2007).
9. Cao, H. *et al*. Fabrication of 10 nm enclosed nanofluidic channels. *Appl. Phys. Lett.* **81,** 174–176 (2002).
10. Mori, S. *et al*. Reduction of line edge roughness in the top surface imaging process. *J. Vac. Sci. Technol. B* **16,** 3739–3743 (1998).
11. Yu, Z. N. *et al*. Fabrication of nanoscale gratings with reduced line edge roughness using nanoimprint lithography. *J. Vac. Sci. Technol. B* **21,** 2089–2092 (2003).
12. Tuckerman, D. B. & Weisberg, A. H. Planarization of gold and aluminum thin-films using a pulsed laser. *IEEE Electron. Dev. Lett.* **7,** 1–4 (1986).
13. Delfino, M. & Reifsteck, T. A. Laser activated flow of phosphosilicate glass in integrated circuit devices. *IEEE Electron. Dev. Lett.* **3,** 116–118 (1982).
14. Armani, D. K., Kippenberg, T. J., Spillane, S. M. & Vahala, K. J. Ultra-high-Q toroid microcavity on a chip. *Nature* **421,** 925–928 (2003).
15. Sameshima, T. Self organized grain growth larger than 1 μm through pulsed-laser-induced melting of silicon films. *Jpn J. Appl. Phys.* **32,** L1485–L1488 (1993).
16. Chou, S. Y., Keimel, C. & Gu, J. Ultrafast and direct imprint of nanostructures in silicon. *Nature* **417,** 835–837 (2002).
17. Constantoudis, V., Patsis, G. P., Tserepi, A. & Gogolides, E. Quantification of line-edge roughness of photoresists. II. Scaling and fractal analysis and the best roughness descriptors. *J. Vac. Sci. Technol. B* **21,** 1019–1026 (2003).
18. Orchard, S. E. On surface leveling in viscous liquids and gels. *Appl. Sci. Res.* **A11,** 451–464 (1962).
19. Chou, S. Y. & Zhuang, L. Lithographically induced self-assembly of periodic polymer micropillar arrays. *J. Vac. Sci. Technol. B* **17,** 3197–3202 (1999).
20. Chou, S. Y., Zhuang, L. & Guo, L. J. Lithographically induced self-construction of polymer microstructures for resistless patterning. *Appl. Phys. Lett.* **75,** 1004–1006 (1999).
21. Wu, L. & Chou, S. Y. Electrohydrodynamic instability of a thin film of viscoelastic polymer underneath a lithographically manufactured mask. *J. Non-Newtonian Fluid. Mech.* **125,** 91–99 (2005).
22. Keene, B. J. Review of data for the surface tension of pure metals. *Int. Mat. Rev.* **38,** 157–192 (1993).
23. Keck, P. H. & Vanhorn, W. The surface tension of liquid silicon and germanium. *Phys. Rev.* **91,** 512–513 (1953).
24. Brooks, R. F., Dinsdale, A. T. & Quested, P. N. The measurement of viscosity of alloys: A review of methods, data and models. *Meas. Sci. Technol.* **16,** 354–362 (2005).
25. Sato, Y. *et al*. Viscosity of molten silicon and the factors affecting measurement. *J. Cryst. Growth* **249,** 404–415 (2003).
26. Gao, H. *et al*. Air cushion press for excellent uniformity, high yield, and fast nanoimprint across a 100 mm field. *Nano Lett.* **6,** 2438–2441 (2006).
27. Chou, S. Y., Krauss, P. R. & Renstrom, P. J. Imprint lithography with 25-nanometer resolution. *Science* **272,** 85–87 (1996).
28. Liu, J. M., Kurz, H. & Bloembergen, N. Picosecond time-resolved plasma and temperature-induced changes of reflectivity and transmission in silicon. *Appl. Phys. Lett.* **41,** 643–645 (1982).
29. Carey, P. G., Woratschek, B. J. & Bachmann, F. Progress toward excimer-laser metal planarization and via hole filling using in situ monitoring. *Microelectron. Eng.* **20,** 89–106 (1993).

Acknowledgements

The authors thank K. Morton and Zhaoning Yu for master imprint moulds, Xiaogan Liang for providing the LER fitting programs and assistance, and P. Murphy for proofreading the manuscript. S.Y.C. thanks L. Cooper, formerly of the U.S. Office of Naval Research (ONR), for his understanding and encouragement, and for providing the earliest financial support to the work. We acknowledge the financial support from ONR and the Defense Advanced Research Projects Agency (DARPA).

Author contributions

S.Y.C. conceived the SPEL method. Both authors contributed to the experiments and data analysis and to writing the manuscript.

Author information

The authors declare competing financial interests: details accompany the full-text HTML version of the paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to S.Y.C.

© 2008 Nature Publishing Group

CORRIGENDUM

Bit storage and bit flip operations in an electromechanical oscillator

I. MAHBOOB AND H. YAMAGUCHI

Nature Nanotechnology **3,** 275–279 (2008)

There were two errors in thirteenth paragraph of this letter. The relation from which the power consumption can be extracted should read CV^2f_s, and the actual expression for the power consumed should read $m\omega^3x^2/2\pi Q$. These errors have also been corrected in the supplementary information.

ERRATUM

Improved nanofabrication through guided transient liquefaction

STEPHEN Y. CHOU AND QIANGFEI XIA

Nature Nanotechnology **3,** 295–300 (2008)

There was an error in the fourth paragraph of the section "Applying SPEL to metals and semiconductors". The first sentence should read: "In guided-SPEL, local spacers are used to keep a plate fixed above the nanostructures (Fig. 1), and the molten nanostructures rise up against surface tension until they reach the plate."

© 2008 Nature Publishing Group