

A novel method for fabricating sub-16 nm footprint T-gate nanoimprint molds

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Abstract

A novel method for fabricating nanoimprint lithography (NIL) molds for T-shaped gates (T-gates) for high speed transistors is proposed and demonstrated. This method uses NIL, low pressure chemical vapor deposition and reactive ion etching processes, and avoids costly electron beam lithography and high accuracy alignment technology. Using the T-gate nanoimprint molds fabricated by this novel method, T-gates with a footprint as small as sub-16 nm were achieved. This method can be extended to fabricate a broad range of 3D nanostructures.

To improve high frequency performance of microwave field-effect transistors, a T-shaped gate (T-gate) with short footprint is needed [1–4]. Since T-gates are 3D structures, it is a big challenge to fabricate them using conventional lithography methods, especially when sub-100 nm foot-width is required. However over the years, several new methods to fabricate T-gates with narrower foot-width have been developed. In most previous work, for T-gates with sub-100 nm foot-width, e-beam writing in multilayer hybrid resist was applied to achieve self-alignment [5, 6]. In some methods, double electron beam lithography was used (one for the footprint and another for the top T-shape). However, the e-beam lithography for ultra-short footprint are not only technically challenge, but also high cost and very low throughput. As a cost-efficient and high throughput method, nanoimprint lithography (NIL) was applied to fabricate T-gates [7]. The nanoimprint molds for T-gates are multilevel structures with a broader base mesa and a narrow top protrusion. To take the advantages of NIL, new fabrication method for multilevel structures has to be developed. In [7], e-beam writing was still used to inscribe a T-shaped opening in double-layered hybrid resist, after that complex tri-layered metal mask fabrication and sacrificial layer remove process followed to form a T-gate NIL mold. The complexity makes this method subtle and relatively high cost. By this method, the minimum foot-width that can be achieved is 40 nm. Further scaling down of the feature size requires some new technology.

In this paper, we present a novel fabrication process for T-gate molds, which achieves self-alignment without involving e-beam writing in multilayer resist or T-gates using NIL and a NIL mold fabricated by our novel method.

The multilevel NIL mold is the key to NIL fabrication of T-gates. Our novel fabrication of the T-gate mold involves core structure fabrication with NIL, conformal deposition with LPCVD and multilevel forming by anisotropic selective reactive ion etching, as illustrated in figure 1. The original Si substrate has a 140 nm SiO₂ layer on the top grown by dry oxidation at temperature of 1000 °C. On this substrate, a small duty-cycle (1/10) 1 μm pitch SiO₂ grating is fabricated using conventional NIL process with a 1 μm pitch grating mold made by interference lithography [8], as shown in figure 1(a). After the NIL patterning and pattern transfer, the line-width of the duplicated SiO₂ grating is around 100 nm. After that, the SiO₂ lines are shrunk to 20 nm wide in diluted buffered oxide etchant (DI:BOE = 10:1, etching time is ~4 min) to form the central protrusions in final T-gate molds. To achieve multilevel upside-down T-shaped mold with self-alignment, a uniform layer of silicon nitride (SiN_x) is conformally deposited to cover the SiO₂ lines on the Si substrate by low pressure chemical vapor deposition (LPCVD), as shown in figure 1(b). The final step is to anisotropically etch the SiN_x-coated structure by reactive ion etching (RIE) with O₂ at 1.5 sccm and CHF₃ at 10 sccm, and with RF power at 150 W. Due to the etching selectivity between SiN_x and SiO₂ (SiN_x is etched about twice as fast as SiO₂), multi levels in the structure (central higher protrusion of SiO₂ with lower shoulders of SiN_x on both sides) are formed and upside-down T-shapes are obtained, as shown in figure 1(c). At this point, the structure that can be used as a T-gate NIL mold is obtained. This structure has lower SiN_x shoulders on both sides and a narrow SiO₂ central protrusion at the center, which can form T-shaped grooves after imprint into resist.

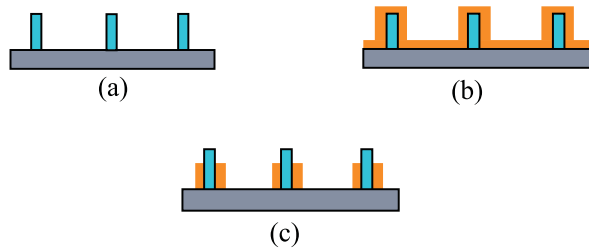


Figure 1. (a) Duplicate high aspect ratio SiO_2 grating on Si substrate by NIL. (b) Conformally deposit SiN_x by LPCVD. (c) Anisotropically etch down the SiN_x layer can T-shaped molds are obtained.

(This figure is in colour only in the electronic version)

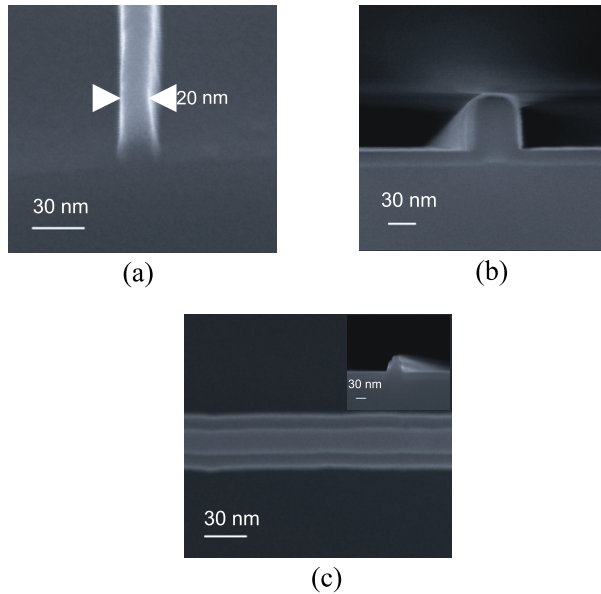


Figure 2. (a) SiO_2 nanowire on Si made by nanoimprint. (b) Conformal deposition of SiN_x on the SiO_2 nanowires. (c) T-gate imprint mold formed after RIE etching.

The fabrication results of the imprint mold are shown in figure 2. Figure 2(a) shows the 20 nm wide SiO_2 line on Si substrate made by nanoimprint lithography and shrunk from 100 nm by wet etching. Figure 2(b) shows the covered SiO_2 line with 30 nm thick SiN_x layer deposited by LPCVD. The multilevel T-gate mold, which is achieved by RIE etching of the covering layer of SiN_x , is shown in figure 2(c).

After the mold is treated by anti-sticking chemical, it can be used in typical thermal NIL process. In the thermal imprint process, several concerns need to be addressed here. First the thickness of spun thermal resist should be controlled carefully, to make sure the resist thickness is close to the height of the protrusion of imprint mold to reduce thickness of the residual resist layer. Large residual layer makes the nano-scale multilevel pattern transfer difficult, since thick residual layer takes a longer time to be etched away and a long etching time will degrade the profile of resist. In our process, the thermal resist (Nanonex NP69) was spun (at 6000 rpm) to be around 120 nm, close to the height of the mold. After imprint, there

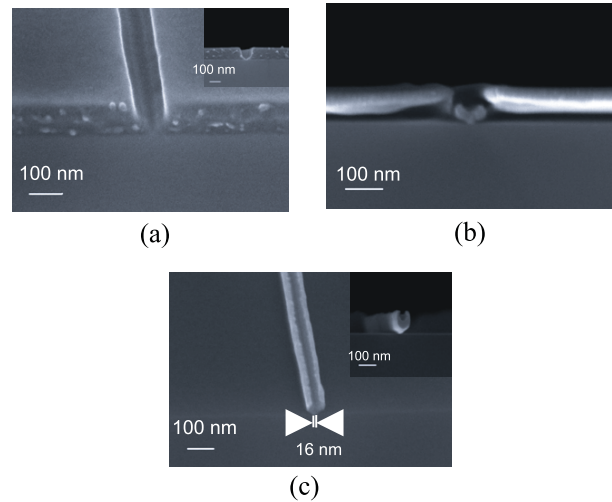


Figure 3. (a) Imprinted resist with T-shaped profile. (b) Cross section of metal T-gate after evaporation of metal. (c) Free standing T-gate.

is still a residual layer of around 6 nm as shown in figure 3(a). This residual layer was etched by RIE with a short time (~ 20 s by O_2 plasma with pressure of 10 mTorr and RF power at 50 W), and the T-shaped pattern in resist was not affected very much by RIE. Then 30 nm Cr was evaporated, as shown figure 3(b). The thickness of evaporated metal should be larger than the height difference between the central protrusion and shoulders of the mold to form big top-parts connected to the narrow feet. But the thickness of metal should not be too large; otherwise the lift-off process would be difficult. In our situation, the thickness of resist was around 110 nm, so the lift-off process with acetone rinse and gentle ultrasonic (200 W, ~ 5 min) could be carried out without serious difficulty. After lift-off, free standing metallic T-gates were left as shown in figure 3(c). From the SEM pictures (taken by using LEO SEM at 5 keV accelerating voltage and ~ 4 mm working distance) it can be observed that the foot-width of the T-gates is around 16 nm (figure 3(c) was taken at MAG 300 KX, corresponding resolution < 3 nm according to our calibration data), which is the smallest foot-width to date to authors' knowledge, and on both sides, upside-pointing wings are formed due to lift-off process.

Using the method proposed above, we have achieved T-gates with smallest sub-16 nm foot-width which is less than half of that achieved in previous work. At the same time this method comes up with a high yield (50 structures from three 2 inch \times 2 inch samples were randomly inspected and three failures were found). In our method, the forming of the foot (the central protrusion in the mold) is decoupled from self-alignment process. We can apply any lithography technologies and line-width shrink technologies to make the foot protrusion, and then conformally deposition and selective etching can be used to achieve self-alignment. Hence the foot-width of T-gate molds can be further scaled down without formidable difficulties. It is also worth pointing out that the proposed method could be applied to other complex structures with small feature sizes and multiple levels, and whose fabrication requires accurate alignment. Possible future applications of

this method could be extreme-fine pitch zone plates for short wavelength and some special metallic plasmonic structures.

In summary, this work demonstrated a novel fabrication method for the smallest T-gates with 16 nm foot-width. In this method, multilevel protrusion molds are fabricated without using high cost and time-consuming e-beam writing, instead NIL, LPCVD and RIE processes are applied. Generally, the method proposed in this work could be extended to fabricate broad range of multilevel structures with self-alignment. If multi layers of materials with different resistance to RIE etching can be conformally deposited on some 'core structures', broad range of multilevel structures can be formed, such as zone plates and multilevel grating.

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