Self-aligned fabrication of 10 nm wide asymmetric trenches for Si/SiGe heterojunction tunneling field effect transistors using nanoimprint lithography, shadow evaporation, and etching

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Fabrication of an asymmetric source/drain structure is important to heterojunction tunneling transistors but is extremely difficult to achieve reliably due to the stringent requirement of nanometer overlay alignment. Here the authors propose and demonstrate a simple self-aligned asymmetric nanotrench fabrication method, which has achieved a 10 nm wide (35 nm deep) trench in source region with an alignment accuracy better than 3 nm. The method is based on asymmetric shadow evaporation of the metal with the gate as a mask, creating an area uncovered by the metal only in the source but not in the drain, and a subsequent reactive ion etching with the evaporated metal as the etching mask. The accuracy of this method was found experimentally and theoretically to be within 5 nm. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3237138]

I. INTRODUCTION

Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) have a minimum subthreshold slope of $2.3(KT/q)$ (60 mV/decade at room temperature) due to the thermionic emission of carriers over a potential barrier, as shown in Fig. 1(a). To reduce the subthreshold slope beyond the classical thermionic-emission limit, which is very desirable for low power operation, it requires a new MOSFET structure and different operation principles where the subthreshold current is dominated by other transport mechanisms, such as impact ionization[1–3] or tunneling.[4–6] For a better subthreshold behavior, it is desirable to make asymmetric Si/SiGe heterojunction tunneling transistors (HETT),[7] as shown in Fig. 1(b).

To fabricate such asymmetric HETTs, one needs to make a SiGe heterojunction trench in the source region with a Si/SiGe interface next to the gate edge within a few nanometers [Fig. 1(b)]. However, such a stringent alignment accuracy cannot be met by current photolithography tools, nor can be achieved by conventional symmetrical self-alignment of the source and drain with the gate.[8–10]

To overcome this alignment challenge, it is preferable to have a reliable self-aligned method to fabricate an asymmetric trench in the source. Previously, self-aligned asymmetric source/drain doping was achieved in different FET structures by combining a vertical and a tilted implant[11] or using a sidewall-spacer gate;[2,6] but in these methods, the source/drain substrate materials still remained the same and no asymmetric trenches were created. Significantly different from these approaches, our method directly creates an asymmetric nanotrench right next to the gate and allows using different source/drain materials.

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II. FABRICATION PROCESS

The key steps in our approach are (a) using the gate as a shadow mask during an evaporation of Cr from an oblique angle to create a gap uncovered with Cr next to the gate and (b) etching Si substrate using the evaporated Cr as the etching mask to achieve an asymmetric nanotrench in the Si substrate next to the gate (Fig. 2). The gap size G, i.e., the trench width, is determined by the shadow evaporation angle θ (relative to the normal of the wafer) and the gate height H by

$$G = H \tan \theta. \quad (1)$$

To test our approach, we used a 200 nm period grating as the gate structure. Particularly, we first fabricated the grating in Si using nanoimprint lithography (NIL),[12–14] e-beam evaporation, metal lift-off, and reactive ion etching (RIE). Then a Cr mask with gaps self-aligned to the grating was formed by a shadow evaporation. This Cr layer defined asymmetric trenches during RIE and was removed after the etching. For completing a HETT structure, SiGe with desired doping level needs to be grown selectively[15–18] in the trench, which is not a part of this work. The details of the above fabrications are described below.

III. FABRICATION OF SUB-20-NM WIDE GRATING FOR NIL MOLDS AND SILICON GATE

The first step in the entire fabrication is to make a nanoimprint mold with sub-20-nm linewidth for the Si gate. We fabricated such molds by shrinking the grating linewidth of an existing mold to sub-20-nm in two steps: (1) use of an O_2 trimming of a trilayer resist structure[19] to narrow the linewidth and (2) further reduction in the resist grating linewidth (imprinted by the new mold) using a bidirectional shadow evaporation.

As shown in Fig. 3, the trilayer structure consists of a layer of 200 nm thick antireflection coating (ARC) (XHRiC-16, Brewer Science, Inc.), a layer 20 nm thick evaporated

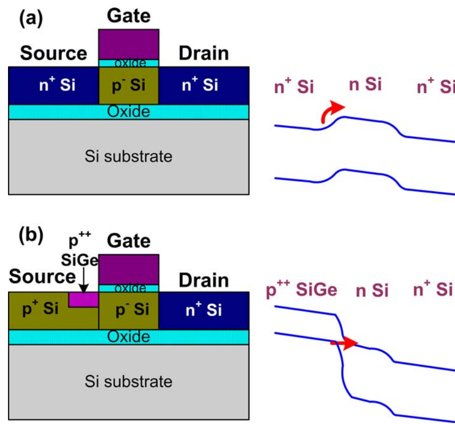

FIG. 1. (Color online) Comparison of a conventional Si MOSFET and a Si/SiGe heterojunction tunneling FET. (a) The device structure and the band diagram of a *n*-type Si MOSFET. (b) The device structure and the band diagram of an *n*-type Si/SiGe HETT transistor.

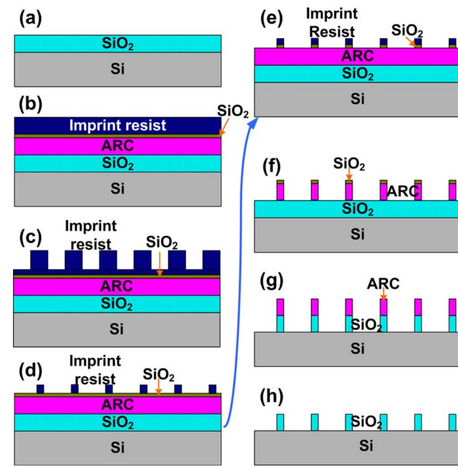

FIG. 3. (Color online) Fabrication of a narrow grating mold using a trilayer structure. (a) A layer of SiO_2 is thermally grown on Si substrate. (b) An imprint resist/SiO_2/ARC trilayer structure is deposited on SiO_2/Si substrate. (c) NIL is used to pattern imprint resist into gratings. (d) High-pressure O_2 RIE is implemented to trim the linewidth of resist gratings and also remove the residual layer. (e) CHF_3 RIE is used to etch through the thin evaporated SiO_2 layer. (f) High aspect ratio ARC lines are patterned by O_2 RIE with SiO_2 as the mask. (g) Narrow gratings are obtained in SiO_2 by CF_4/H_2 RIE using ARC as the mask. (h) ARC is stripped to get final grating mold.

SiO_2, and a layer of imprint resist (Nanonex Corp.) on a Si substrate with 130 nm thick thermal SiO_2. Nanoimprint lithography created a grating of 85 nm linewidth and 200 nm period in the top resist. Then an O_2 RIE process (SLR 720 RIE system, Plasma-therm, Inc.) at a relatively high pressure (~50 mTorr) was used to trim the resist linewidth from 85 to about 40 nm, in addition to removing the residual layer of the resist. A CHF_3 RIE at 2 mTorr base pressure was then used to transfer the narrow resist lines into the underlying thin SiO_2. Using the patterned SiO_2 as the etching mask, a further O_2 RIE transferred the narrow lines into ARC with a high aspect ratio since SiO_2 has a good resistance to O_2 RIE. Finally, using ARC as an etching mask, the narrow grating was transferred to the thermal SiO_2 of the mold by CF_4/H_2 RIE. ARC can be readily stripped by using standard RCA-1 cleaning (NH_4OH: H_2O_2: DI H_2O=1:1:5, 80 °C).

Figures 4(a) and 4(b) show the cross-sectional scanning electron microscopy (SEM) pictures of the patterns imprinted into resist using an original grating mold and the fabricated narrow grating mold, respectively. The grating linewidth shrunk from 115 to 40 nm. Such a mold was fabricated on a 4 in. wafer with a good uniformity [Fig. 4(c)], depending on uniform RIE etching. Another advantage of having a narrow width in a grating mold is that a thin residual resist layer, less than 5 nm [Fig. 4(b)], can be achieved more easily due to less resist flow.

To further shrink the linewidth, we used a bidirectional Cr shadow evaporation[20,21] to narrow the opening of the resist trenches which were imprinted using the new grating mold. About 9 nm thick Cr was evaporated from the two directions which are at 60° from the sample surface normal and perpendicular to the grating lines and capped the top part of the trench. The gap size could be shrunk from 40 down to 20 nm, as seen from Figs. 5(a) and 5(b). The narrow opening was then used as a mask for deposition of another layer of 15 nm thick Cr at the bottom of the trench. A lift-off process was then carried out to pattern Cr lines onto Si substrate [Figs. 5(c) and 5(d)], which consists of soaking the sample in acetone for ~15 min, spraying acetone using Airbrush spray

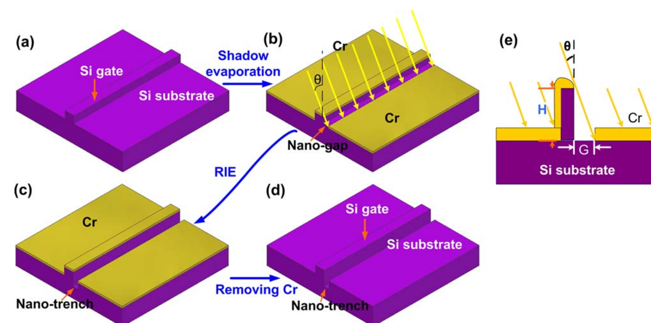

FIG. 2. (Color online) Fabrication of self-aligned asymmetric nanotrenches. (a) Si gate testing structure is patterned. (b) Nanogap is created and aligned to the gate by a Cr shadow evaporation. (c) Nanotrenches are formed by RIE. (d) Cr is removed. (e) Scheme of dependence of self-aligned nanogap size *G* on Si gate height *H* and shadow evaporation angle *θ*.

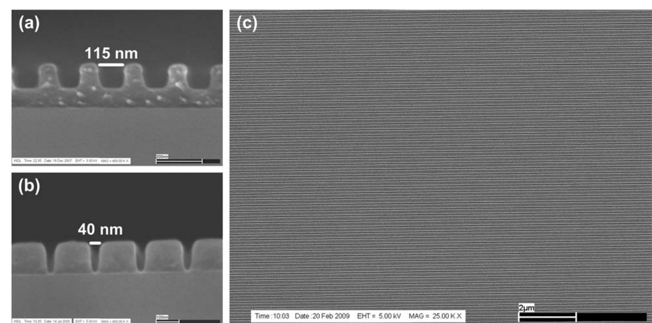

FIG. 4. SEM pictures of imprinted patterns of original grating mold and fabricated narrow grating mold. (a) Cross-sectional view of imprint pattern in resist using original grating mold. (b) Cross-sectional view of imprint pattern in resist using fabricated narrow grating mold. (c) Top view of large area imprint pattern in resist using fabricated narrow grating mold.

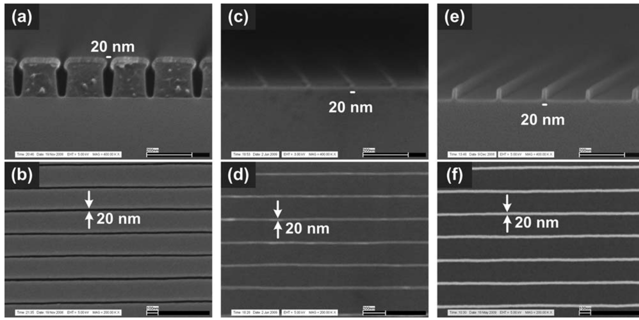

FIG. 5. SEM pictures of different steps toward fabricating 20 nm wide Si testing gates. [(a) and (b)] Cr mask on resist grating. [(c) and (d)] 20 nm wide Cr grating lines on Si substrate. [(e) and (f)] 20 nm wide grating lines in Si. The top pictures are cross-sectional view, and the bottom ones are top view.

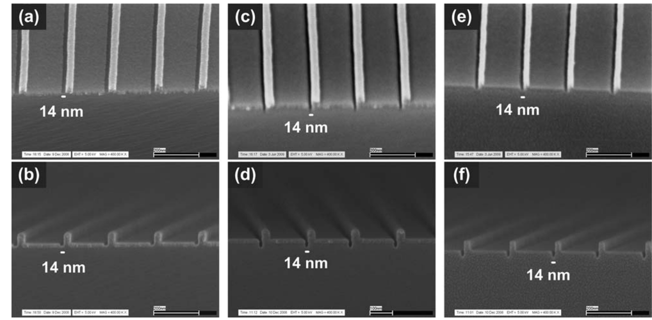

FIG. 6. SEM pictures of different fabrication steps for achieving 14 nm wide asymmetric trenches aligned to one side of Si grating. [(a) and (b)] 14 nm wide gap created by shadow evaporation at $\theta = 20°$. [(c) and (d)] Asymmetric trenches etched into Si by RIE. [(e) and (f)] 14 nm wide trenches aligned to grating after removing Cr. The top pictures are tilted view (45°), and the bottom ones are cross-sectional view.

gun, and finally cleaning in RCA-1 for 1–2 min. The Cr lines are 20 nm wide, the same as the narrowed trench opening. A RIE process was used to etch into Si for about 40 nm to obtain the straight Si grating structures and, subsequently, the Cr mask was removed using CR-7 chromium etchant (Cyantek Corp.), as shown in Figs. 5(e) and 5(f). The linewidth of the final Si grating was calculated to be 20.5 ± 1.7 nm using a homemade MATLAB code. Clearly, rather good fidelity of the narrow grating lines was preserved throughout the whole fabrication process.

Previous work already demonstrated that the bidirectional shadow evaporation technique could be used for wafer-scale pattern transfer with small linewidth variations,[22] in which case the final linewidth was even highly dependent on the evaporation angle as the resist was in triangular profile.[21,22] In our case, the trench opening size should be much less sensitive to the angle, as the trench sidewall could be controlled fairly vertical. Therefore, the bidirectional shadow evaporation technique is expected applicable to wafer scale, making the whole two-step feature-size tuning technique satisfying large-area and repeatable productions. Moreover, the two-step feature-size tuning technique provides a great flexibility in controlling, not only shrinking but also expanding, feature sizes; and it is not limited to only one-dimensional grating structures but can also be used to two-dimensional pillar or hole structures.

The reason why we had to use the two-step linewidth shrinking approach is that just a bidirectional evaporation itself generally cannot offer uniform linewidth reduction, especially when the reduction is over 50 nm since a thick metal layer introduces large grains or clusters during deposition and thus results in unacceptable linewidth roughness and variations.

IV. FABRICATION OF SELF-ALIGNED ASYMMETRIC NANOTRENCHES

Using the 20 nm wide and 41 nm high Si grating obtained by NIL and etching, we fabricated a 14 nm wide gap by shadow evaporation of 10 nm thick Cr from about $\theta = 20°$ [Figs. 6(a) and 6(b)]. An $O_2/CF_4/SF_6/Ar$ based RIE was used to etch asymmetric trenches into the Si substrate [Figs. 6(c) and 6(d)], and then Cr was removed [Figs. 6(e) and 6(f)]. Clearly the desired self-alignment of the asymmetric trenches to the Si gate was achieved.

In another test, we fabricated 35 nm wide and 57 nm high Si grating structure as the gate, and obtained 24 nm sized self-aligned nanotrenches using $\theta = 22°$ and 10 nm thick of Cr shadow evaporation [Fig. 7(a)]. Similarly, by lowering the Si grating height H to 40 nm and changing the shadow evaporation angle to $\theta = 18°$, we achieved nanotrenches as narrow as 10 nm [Fig. 7(b)].

The alignment accuracy was estimated by measuring the offset of the asymmetric trench to the grating edge in Figs. 6 and 7 and found about 2–3 nm, which is far better than the alignment capabilities of current lithography tools.[23] The

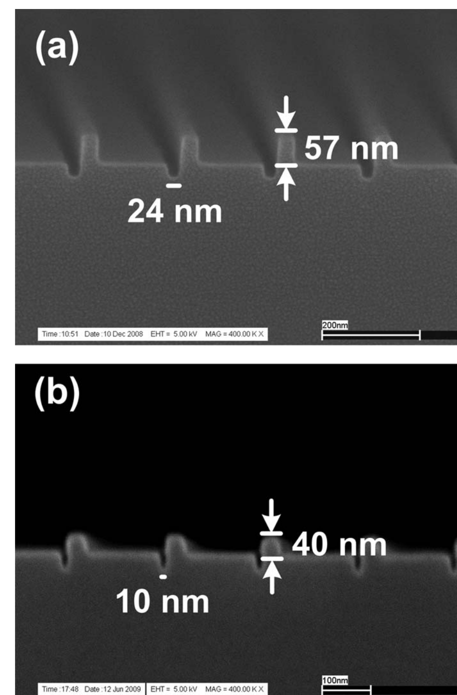

FIG. 7. SEM pictures of different asymmetric trench widths achieved by tuning shadow evaporation angle θ and Si grating height H.

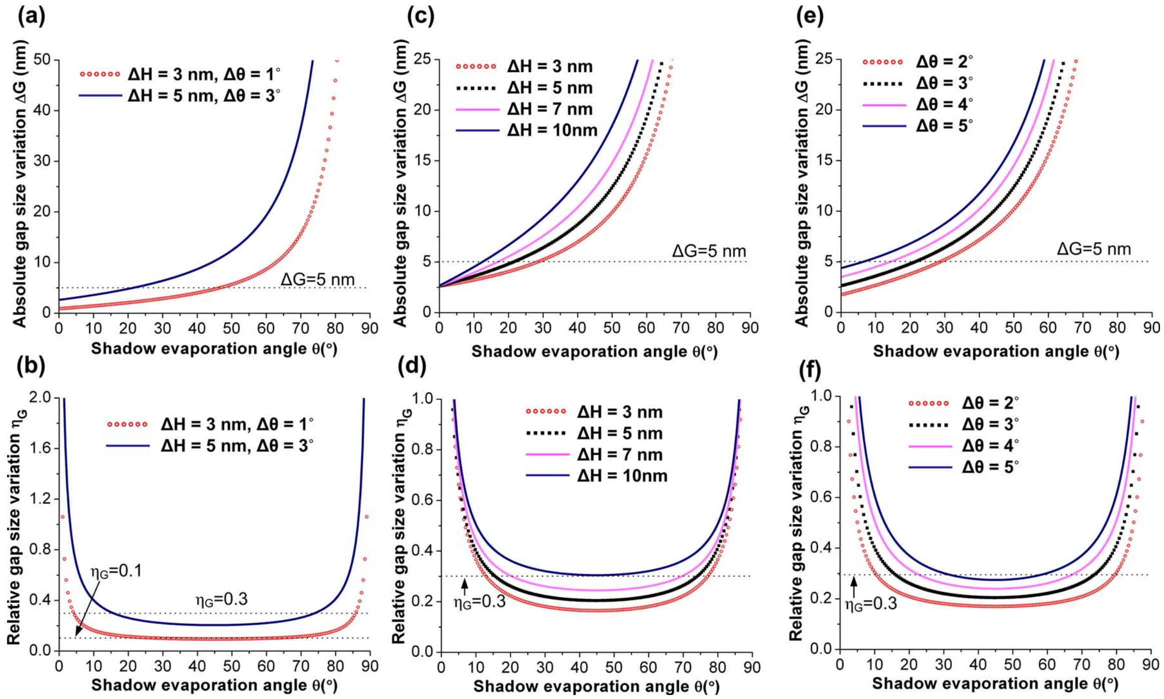

FIG. 8. (Color online) Dependence of absolute and relative gap size variations ΔG and η_G on shadow evaporation angle θ with different variations ΔH and $\Delta\theta$. [(a) and (b)] ΔG and η_G vs θ for an ideal case (ΔH=3 nm, $\Delta\theta = 1°$) and a practical case (ΔH=5 nm, $\Delta\theta = 3°$). [(c) and (d)] ΔG and η_G vs θ for different ΔH (assuming $\Delta\theta = 3°$). and [(e) and (f)] ΔG and η_G vs θ for different $\Delta\theta$ (assuming ΔH=5 nm). It is assumed H=50 nm throughout the analysis.

alignment of the trench to the gate edge is determined by the lateral etching behavior during RIE and can be further fine tuned. The excellent and reliable overlay accuracy of this simple self-aligned method is clearly better than that of the approaches based on manual alignment.

V. ACCURACY IN CONTROLLING TRENCH WIDTH

The absolute and relative variations of asymmetric trench widths (gap sizes) ΔG and $\eta_G = \Delta G/G$ are, to the first order approximation, proportional to the gate height variation ΔH and the evaporation angle variation $\Delta\theta$ through the equations,

$$\Delta G = \Delta H \tan\theta + H \cdot \Delta\theta \cdot \frac{1}{\cos^2\theta}, \qquad (2)$$

$$\eta_G = \frac{\Delta G}{G} = \frac{\Delta H}{H} + \frac{\Delta\theta}{\sin\theta\cos\theta}. \qquad (3)$$

Since the proportional coefficients in the equations are functions of the evaporation angle θ, both ΔG and η_G vary at different θ. To see the angle effects, we can set H=50 nm and plot ΔG and η_G versus θ for different ΔH and $\Delta\theta$ (Fig. 8). They clearly show that ΔG is smaller for a narrower angle; but the relative error η_G achieves its minimum at 45° and increases significantly when the angle approaches either $0°\,(G \approx 0)$ or 90°. As seen from the two cases plotted in Figs. 8(a) and 8(b), i.e., ΔH=3 nm, $\Delta\theta = 1°$ and ΔH=5 nm, $\Delta\theta = 3°$, η_G can be ideally smaller than 10% but practically may only be tuned below 30% when $16° < \theta < 74°$ (or smaller than 21% when $36° < \theta < 54°$). ΔG and η_G can be managed reasonably small simultaneously, e.g., $\Delta G < 5$ nm and $\eta_G < 30\%$, by tuning θ in a certain range, which is 5°–46° ideally and 16°–22° more practically.

The effect of ΔH on the variations is shown in Figs. 8(c) and 8(d), with $\Delta\theta = 3°$ and H=50 nm. It is clear that the values of ΔH not only influence the angle range for achieving small ΔG (e.g., smaller than 5 nm) but also set the lower limits of applicable η_G. On the other hand, if we fix ΔH =5 nm and H=50 nm but change $\Delta\theta$, we have ΔG and η_G versus θ in Figs. 8(e) and 8(f). They show that the angle windows for $\Delta G < 5$ nm or $\eta_G < 30\%$ narrow more significantly as $\Delta\theta$ increases. It means that the variation in the evaporation angle may be a more critical factor to influence the variations of trench widths.

To evaluate the variations experimentally, we measured the grating height H from the SEM pictures, calculated the expected trench sizes G^* from the average of H and experimental values of θ using Eq. (1) and compared G^* to the measured trench gap sizes G, as listed in Table I. It is found that the values of G^* and G are close, namely, with an error smaller than 3 nm, showing that the gap sizes could indeed be well controlled by θ and H. Besides, the derived theoretical gap size variations from experimental parameters using Eq. (2) indicate larger errors are expected and that is mainly because a large but reasonable variation in shadowing angle is estimated and fortunately relatively small errors seemed to happen during the experiments.

VI. SUMMARY

We proposed and demonstrated a simple method to pattern an asymmetric nanotrench in the source regions and

TABLE I. Evaporation of gap size variations in three asymmetric trench samples. [Sample 1: Fig. 6; sample 2: Fig. 7(a) and sample 3: Fig. 7(b).]

Samples	Evaporation angle θ (deg)	Gate height H (nm)	Experimental gap size G (nm)	Expected gap size G^* (nm)	Gap size error $G'=G^*-G$ (nm)	Theoretic gap size variation $\Delta G=\Delta H \tan\theta + H\Delta\theta(1/\cos^2\theta)$ (nm)
1	20 ± 4	41.2 ± 0.8	13.8 ± 1.2	15.0	1.2	3.6
2	22 ± 4	56.9 ± 1.8	24.4 ± 0.8	23.0	−1.4	5.4
3	18 ± 4	40.1 ± 1.8	10.6 ± 0.9	13.0	2.4	3.7

self-aligned to the gate for HETT transistors by using shadow evaporation and RIE. Different trench widths as small as sub-10-nm are fabricated by controlling the gate height H and shadow evaporation angle θ. Our theoretical analysis and experimental results both show good trench size control (gap size variation $\Delta G < 5$ nm) are achievable, and both the absolute and relative variations can be simultaneously minimized by tuning the evaporation angle within a large range (ideally 5°–46°). The dimension of the gate was also fine tuned to sub-20-nm using an O_2 trimming etching of a trilayer structure and also a bidirectional evaporation, indicating a vast device dimension scaling-down potential for future HETT transistors. We believe that this straightforward, reliable, and effective self-aligned fabrication method for narrow asymmetric trenches will have various applications in semiconductor ICs, as well as in nanophotonics, nanobiotechnology, and nanoelectromechanical systems.

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