Fabrication of patterned Ge_xSi_{1-x}/Si layers by pulsed laser induced epitaxy

Y. Chang, S. Y. Chou,[a] J. Kramer, and T. W. Sigmon
Solid State Laboratory and Department of Electrical Engineering, Stanford University, Stanford, California 94305

A. F. Marshall
Center for Materials Research, Stanford University, Stanford, California 94305

K. H. Weiner
Lawerence Livermore National Laboratory, Livermore, California 94550

(Received 14 December 1990; accepted for publication 16 February 1991)

Selective growth of Ge_xSi_{1-x} on Si is demonstrated for the first time using a pulsed laser induced epitaxy technique, combined with either standard oxide or liftoff patterning processes. Two different dimensions of $Ge_{0.12}Si_{0.88}$/Si lateral wells are formed, 3.5 μm wide by 1700 Å deep, and 6 μm wide by 1300 Å deep. High-resolution transmission electron microscopy, combined with energy-dispersive x-ray imaging, reveals a well-defined two-dimensional (2D) Ge redistribution profile with no significant line or surface defects observed. The 2D Ge well distribution profiles, governed by heat and mass transport during the laser processing, are discussed.

Strained Ge_xSi_{1-x}/Si heteroepitaxial layers provide a highly attractive, narrow band-gap material system for use, due to its valence-band discontinuity, isoelectronic behavior, and compatibility with Si integrated circuit processing technology, in the fabrication of high performance Si-based heterojunction bipolar transistors and circuits. Current efforts in the materials growth area for making these layers are mainly based on either molecular beam epitaxy or chemical vapor deposition.[1,2] The selective nature of these growth techniques, however, is exploratory at best, with either redesign of device structures or improved growth techniques being pursued.[3]

Recently the fabrication of heteroepitaxial Ge_xSi_{1-x}/Si and $In_xGa_{1-x}As$/GaAs large-area single-crystal layers using a pulsed XeCl excimer laser to melt through the deposited film and part of the substrate has been reported.[4–6] The characteristic thermal processing cycle for this technique, a few hundred of nanoseconds, allows no significant wafer heating. The melt depths and profiles obtained are therefore precisely controllable, *in situ* and in *real time*, are abrupt and on the order of 10–200 nm thick depending upon the laser parameters and deposited film thickness. Also, by combining the process with integrated circuit fabrication techniques and *in situ* gas immersion laser doping (GILD),[7] this technique can be applied to selective processing on a die-by-die fashion, an example being use in hybrid SiGe bipolar complementary metal-oxide-semiconductor (BiCMOS) circuits. Therefore, development of the selective pulsed laser induced epitaxy (PLIE) combined with *in situ* doping is important for a host of possible applications for making very shallow junction devices based on selective heteroepitaxial layers. This could potentially allow for direct integration of a selective heteroepitaxial process into conventional semiconductor manufacturing technology.

In this letter, we demonstrate the integration of PLIE with conventional device processing for fabrication of patterned Ge_xSi_{1-x}/Si structures. We implement two different semiconductor patterning techniques to make these layers in order to demonstrate the feasibility of developing the selective nature of this technology. The Ge_xSi_{1-x}/Si well width is defined primarily by the photolithography processing while the layer depth is controlled by the deposited film thickness and laser parameters. High-resolution transmission electron microscopy (TEM) imaging and energy-dispersive x-ray (EDX) mapping are used to investigate the two-dimensional (2D) Ge distribution profiles and to detect the existence of any significant line or surface defects in the layers. Successful demonstration of this process will allow fabrication of selectively isolated, thin base Ge_xSi_{1-x}/Si heterojunction bipolar transistors and other structures such as electron or light waveguides by choosing the appropriate material systems.

Two different patterning techniques, Al/SiO_2 masking layers (Fig. 1) or liftoff (Fig. 2), are employed in this study. For the patterned Al/SiO_2 mask processing sequences, shown in Fig. 1, a 3 in. (100) *n*-type (0.1 ~ 0.9 Ω cm) Si wafer is thermally oxidized to form a 500 nm SiO_2 layer. Then, a 1 μm layer of pure Al is deposited, to serve as a highly reflective mask for the 308 nm XeCl laser. Following a standard photolithography process, Al and SiO_2 are patterned to open the well region for the Ge_xSi_{1-x} layer growth. After removal of the photoresist, the wafer is loaded into an *e*-beam evaporator. Following the deposition of ~ 13 nm of amorphous Ge, the wafer is transferred to the pulsed laser system. For the liftoff process, a *p*-type (5×10^{14} cm^{-3}) Si (100) wafer with the substrate axis 4° off toward the [110] is used. Following wafer cleaning, a 0.5-μm-thick photoresist is spun onto the substrate and then baked at 90 °C for 20 min. Patterns of lines with various linewidths are photolithographically exposed in the

[a]Presently with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455.

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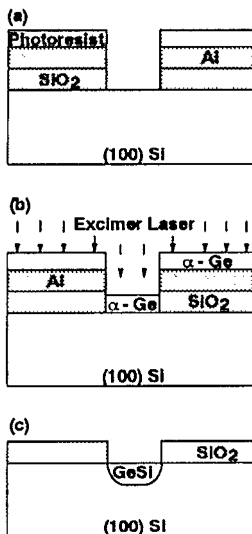

FIG. 1. Schematic illustration of the processing steps for the Al/SiO_2 process.

resist. Just before loading into the *e*-beam evaporator, the wafer is dipped in BOE (6:1) for 10 s and then rinsed in DI water for 30 s. Then, a ~15-nm-thick Ge film is evaporated onto the patterned substrate. Before loading into the laser system, the liftoff process is performed in acetone. The XeCl laser processing steps used for this study are very similar to those employed by Carey *et al.*[7] However, for this experiment, *in situ* doping was not incorporated.

Two different lithography masks are used for this study. Each mask is essentially an array of open lines and oxide spacers which offer enough area for TEM sample preparation and investigation. The Al/SiO_2 mask consists of an array of closely spaced lines 1500 μm long with 3 μm openings and 5 μm spacers.[8] For the liftoff array, the line widths and oxide spacers range from 2 to 50 μm with all lengths being 3 cm.

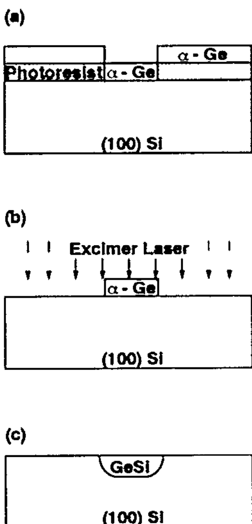

FIG. 2. Schematic processing steps for the liftoff processes.

TEM is used to determine the Ge_xSi_{1-x} well configuration resulting after PLIE processing. The Ge and Si mass contrast although low is visible in the bright-field images if other contrast mechanisms, such as diffraction contrast due to thickness variations, are minimized. The Ge profile is also investigated *in situ* in the TEM by EDX mapping. This is carried out in the scanning TEM mode by focusing the electron beam down to about 5 nm in diameter and scanning across the well. This mapping method is used to overcome the problem when the edge of the Ge_xSi_{1-x}/Si is difficult to define in the TEM image. The Ge concentrations in the Ge_xSi_{1-x}/Si wells are also determined by the EDX analysis. Features near the Ge_xSi_{1-x}/Si interface are examined in detail by lattice imaging to determine if any defects exist. For the Al/SiO_2 mask process, regions are available on the mask which enable subsequent characterization of the layers using Rutherford backscattering spectrometry (RBS). This allows exact determination of the Ge_xSi_{1-x}/Si layer depth and Ge composition which compare well with the TEM/EDX measurements.

In Figure 3(a) we show $Ge_{0.12}Si_{0.88}$ wells fabricated using the Al/SiO_2 mask process while in Fig. 3(b) the results using the liftoff process are presented. The photos are arranged in such a fashion so that the profile differences resulting from the two different processes are easy to compare. In Fig. 3(a), the 5 μm oxide spacers and 3 μm openings are clearly seen in the figure. Also, the 3 μm by 200 nm $Ge_{0.12}Si_{0.88}$ well is clearly defined in the TEM photos from the Ge mass contrast. This is also seen in the higher magnification photo included at the bottom of Fig. 3(a). The laser parameters used for this sample are an energy fluence of 1.0 J/cm^2 resulting in a 70 ns melt duration. The Ge redistribution profile starts from the edge of the Si/SiO_2/Ge_xSi_{1-x} corner and extends both vertically and laterally into the open channel. The oxide spacers have a rounded top corner which tapers down to the Si surface. This results in increased absorption of the laser light causing a hot region at the Si/SiO_2/Ge_xSi_{1-x} corner since the Al will not reflect the incoming laser energy at this tapered edge. For this experiment, we only employed wet etching to remove the Al followed by a plasma etch to open the SiO_2 window. The SiO_2 edge could be improved by using plasma etching to remove both the Al and SiO_2 layers. Current research is focused on developing a compromise in the processing steps which allows tailoring the sidewall profiles

In Fig. 3(b), a 6-μm-wide, 150-nm-deep $Ge_{0.12}Si_{0.88}$/Si lateral well fabricated using the liftoff process is shown in the cross-sectional TEM micrograph. In order to investigate the Ge redistribution behavior at the sidewall, we also show the well picture at higher magnification. It is seen that an abrupt Ge_xSi_{1-x}/Si junction has been obtained. Even at the sidewall region, we still can see the Ge_xSi_{1-x}/Si interface. Also, the very uniform image implies few if any defects in this structure. We have also investigated lattice images (not shown here) in this region tracing along the Ge_xSi_{1-x}/Si interface. No dislocations or stacking faults are found for these structures.

In order to study the heat and mass transport behavior

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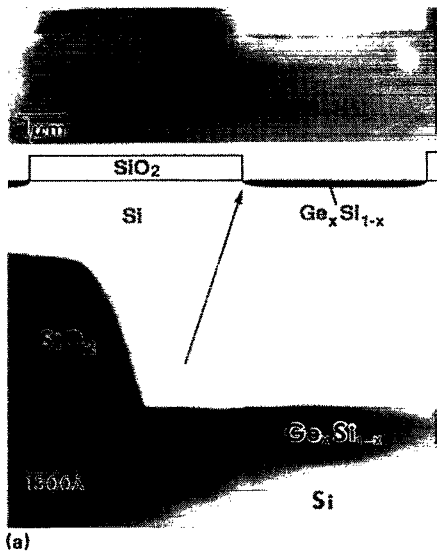

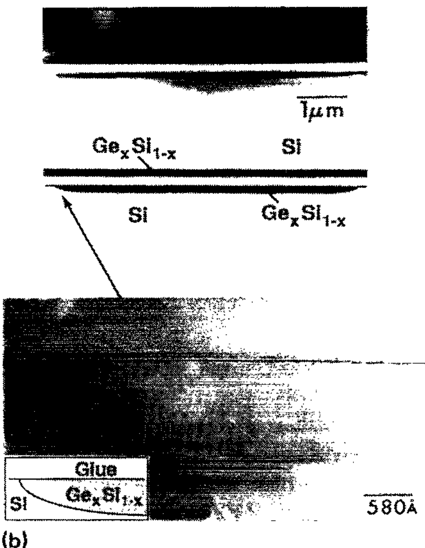

FIG. 3. Cross-sectional TEM photographs of $Ge_{0.12}Si_{0.88}/Si$ wells: (a) after Al/SiO_2 mask and (b) liftoff processing, respectively. The pictures shown in the bottom are the images viewed at a higher magnification.

for the 2D problem at hand, the Ge profiles, obtained from Figs. 3(a) and 3(b) for two different processing steps, are curve fitted, with the results shown in Fig. 4. Since the Ge-Si mass contrast in the TEM bright-field images serves as a good marker, these data can be provided as experimental results for verification using 2D laser processing simulators. In Fig. 4, we are able to fit the curves with a simple logarithm relation rather than a more complicated polynomial fit. Although we do not presently understand

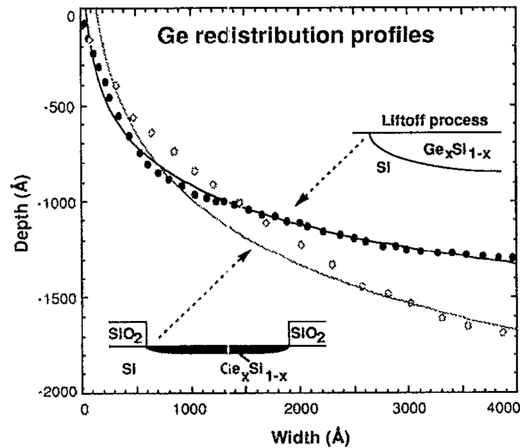

FIG. 4. Ge distribution profiles plotted and curve fitted using the melt depth vs lateral diffusion length. The schematic diagrams shown in the graphs are not in scale.

the physical meaning of this logarithm relationship, it is particularly useful for providing a quantitative relation between the vertical and lateral melt lengths. It is seen that the Ge profile for the liftoff process has a better fit to the logarithm relation than that of the Al/SiO_2 mask process possibly due to the more complicated processes and geometry in the Al/SiO_2 mask process. The characteristic round sidewall shape, however, for both cases is indeed very similar. This almost process independent characteristic shape, which has the lateral diffusion length being very nearly equal to the vertical transport depth, may eventually set limits on the smallest well width which can be fabricated.

In conclusion, we employ two different patterning processes to fabricate Ge_xSi_{1-x}/Si lateral wells. The results indicate that laser-induced epitaxy techniques can be integrated into semiconductor processes for selective growth of patterned Ge_xSi_{1-x}/Si wells.

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