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2011 Nanotechnology 22 445301

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Printing of sub-20 nm wide graphene ribbon arrays using nanoimprinted graphite stamps and electrostatic force assisted bonding

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Received 1 August 2011, in final form 7 September 2011

Published 6 October 2011

Online at stacks.iop.org/Nano/22/445301

Abstract

Nano-graphene ribbons are promising in many electronic applications, as their bandgaps can be opened by reducing the widths, e.g. below 20 nm. However, a high-throughput method to pattern large-area nano-graphene features is still not available. Here we report a fabrication method of sub-20 nm ribbons on graphite stamps by nanoimprint lithography and a transfer-printing of the graphene ribbons to a Si wafer using electrostatic force assisted bonding. These methods provide a path for fast and high-throughput nano-graphene device production.

Graphene [1–3], a two-dimensional carbon crystal [2–5], has been explored for many electronic applications [2, 6–10], because of its high conductivity, mobility, and other intriguing properties, e.g. transparency and flexibility. For high-performance electronics, it is often necessary to pattern high-quality graphene into nano-ribbons, e.g. narrower than 20 nm [6, 11], over the entire wafer. Despite many efforts [1, 6, 12–17], however, a high-throughput method to fabricate large-area graphene nano-ribbons (GNRs) is still not available. Rather than patterning a large single crystal graphene wafer, a promising yet drastically different approach, proposed by one of the authors [18], is to put high-quality graphene patterns only in the active device area on a supporting substrate ('graphene on demand'). Based on this idea, transfer-printing of graphene was realized using the graphene stamps patterned with either micro-features by photolithography [19] or nano-features by electron beam lithography (EBL) [20], and the printing has shown good repeatability and uniformity, addressable control, and potential large-scale patterning capability.

Rather than using EBL, which is a serial point-to-point writing, thus time-consuming and low-throughput, here we report a method of patterning sub-20 nm wide ribbon arrays on graphite stamps using nanoimprint lithography (NIL) [21] and a transfer-printing of the GNR arrays to the SiO₂ surface of Si wafers.

Our fabrication of graphene ribbons on a Si wafer has three key steps (figure 1): (i) UV imprint to pattern a resist on a fresh-cleaved highly ordered pyrolytic graphite (HOPG) stamp (figures 1(a) and (b)); (ii) etch graphene nano-ribbons on the stamp by oxygen plasma reactive ion etching (RIE) and stripping the imprint resist (figure 1(c)); (iii) transfer-print graphene ribbons on a SiO₂ surface of a Si wafer by pressing, applying external voltage, and peeling (exfoliation) (figures 1(d) and (e)).

Before the above processing steps, we first need to fabricate a NIL mold with 20 nm wide nano-trenches. The mold was fabricated from a 4" master NIL mold with a large feature size and by a two-step feature-size trimming method to achieve the designed feature size [22] (figure 2). The first trimming, where the linewidth was reduced from 120 to 35 nm, created a 4" daughter mold, and the second trimming, where the linewidth was reduced from 35 to 20 nm, created a 4" granddaughter and the final mold.

Briefly, the first trimming step (figures 2(a)–(g)) was based on oxygen plasma etching of nanoimprinted gratings in a tri-layer resist structure [23]. The resist structure has a top layer of thermoplastic imprint resist (NXR-1025, Nanonex Corp.), a middle layer of thin (~20 nm) e-beam evaporated SiO₂, and an bottom layer of cross-linked polymer ARC (antireflection coating XHRiC-16, Brewer Science, Inc.).

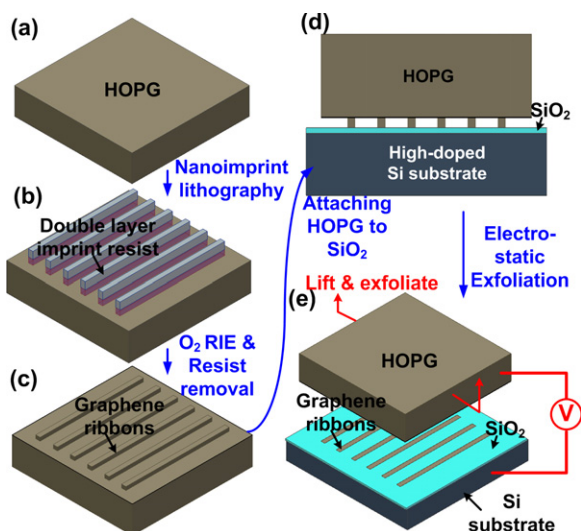


Figure 1. Schematics of patterning and transferring of nano-graphene ribbons: (a) HOPG substrate cleaned with Scotch tape; (b) graphene ribbons patterned on HOPG by UV nanoimprint lithography and oxygen RIE; (c) imprint resist removal to expose graphene ribbons; (d) graphene ribbons attached to SiO₂/Si wafers; (e) graphene ribbons' exfoliation and transfer to SiO₂/Si.

This tri-layer structure is advantageous, because of its compatibility with various lithography approaches (cross-linked ARC is chemically inert in solvents/resists), high etching selectivity to Si or SiO₂ substrate, easily tunable

feature aspect-ratio (e.g. changing the ARC thickness), and convenient resist removal (standard cleaning RCA). By combining with NIL, it further provides flexible and controllable linewidth shrinking (by oxygen etching), multi-functionality as either a positive-tone (ARC liftoff) or negative-tone resist (direct etching), high-fidelity pattern transfer, and a large-area patterning uniformity (based on dry etching, with variation <1% [24, 25]).

Specifically, the tri-layer structure was nanoimprinted (250 psi, 130 °C, 5 min, Nanonex NX-2000 imprinter) on 130 nm thermal silicon oxide using a master grating mold (120 nm wide, 200 nm pitch), obtaining a 150 nm high and 80 nm wide resist grating with a 65 nm residual layer on SiO₂/ARC, as shown in the scanning electron microscope (SEM) image (figure 3(a)). Then, a high-pressure O₂ plasma etching (10 sccm, 50 W, 50 mTorr, 2 min 30 s) reduced the top-layer resist grating width to ~40 nm (figure 3(b)), while removing the residual resist in the trench. An O₂/CHF₃ RIE (1.5/10 sccm, 100 W, 2 mTorr, 2 min 30 s) etched through the 20 nm SiO₂ mid-layer masked by the top resist grating (figure 3(c)). Another oxygen RIE (10 sccm, 50 W, 2 mTorr, 6 min) patterned the bottom-layer resist (i.e. ARC) into 160 nm high 35 nm wide gratings (figure 3(d)), undercutting ARC by 5 nm. The triple-layer resist pattern was used as a mask in etching 35 nm wide 130 nm deep gratings in the SiO₂ mold using CF₄/H₂ RIE (33/7 sccm, 300 W, 50 mTorr, 3 min) (figure 3(e)), with 30% overetch to obtain vertical SiO₂ grating sidewalls and flat Si bottom surfaces, where the Si wafer acted as an etching-stop material due to its low etching rate

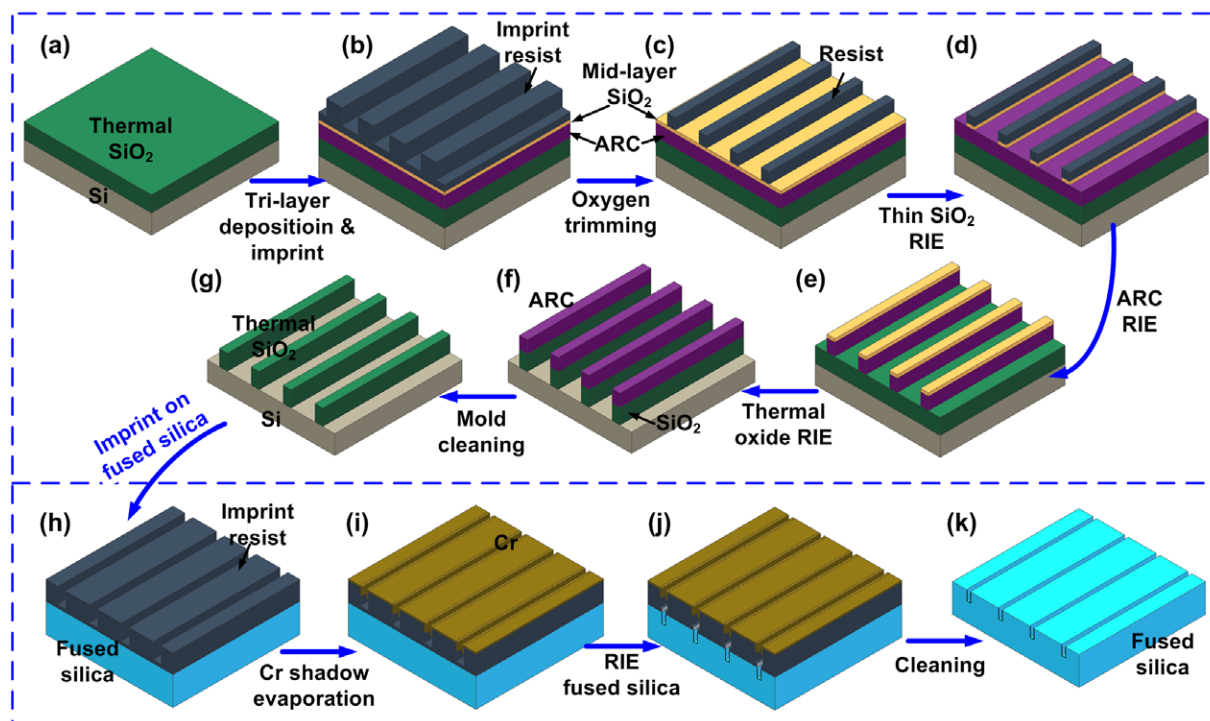


Figure 2. Fabrication schematics of a nano-trench mold using a two-step feature-size trimming technique. (a)–(g) Step 1: fabrication of a daughter mold of narrower gratings in SiO₂/Si using a tri-layer structure (imprint resist/SiO₂/ARC): (a) SiO₂/Si substrate cleaning, (b) tri-layer NIL on SiO₂/Si, (c) RIE residual layer and trimming of the line width, (d) RIE mid-layer SiO₂, (e) RIE antireflection coating (ARC) gratings, (f) RIE SiO₂ substrate, and (g) ARC removal and cleaning. (h)–(k) Step 2: fabrication of a granddaughter nano-trench mold in fused silica: (h) nanoimprint with daughter grating mold, (i) bi-directional Cr shadow evaporation to reduce the trench width, (j) RIE residual resist and etch into fused silica, and (k) resist removal and surface cleaning.

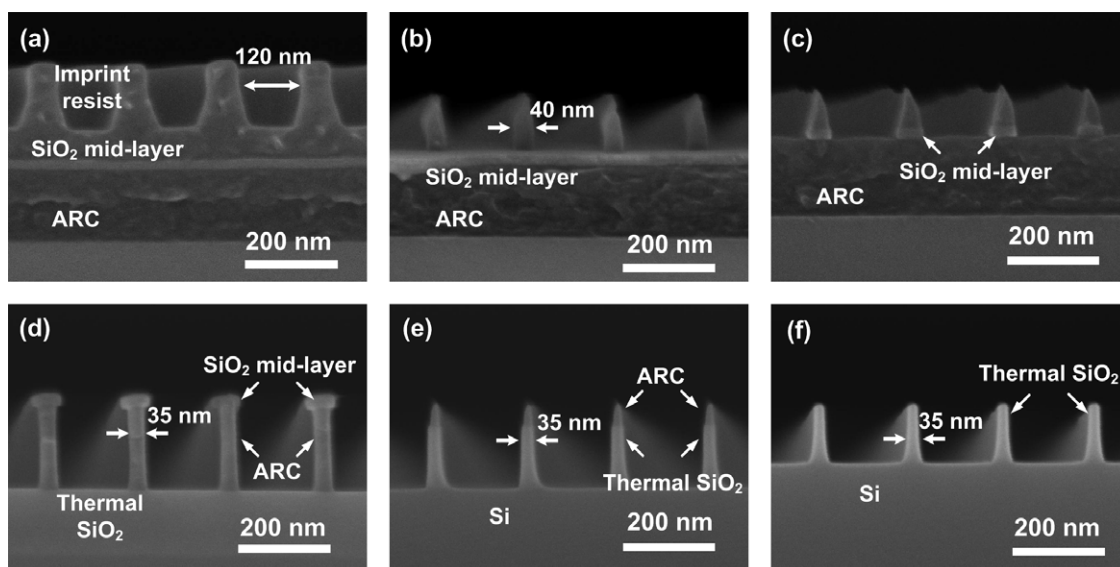


Figure 3. Cross-sectional SEM images of fabrication of a 35 nm wide grating mold: (a) as-imprinted 80 nm wide gratings in tri-layer structure on thermal SiO₂; (b) oxygen plasma reduced 40 nm wide resist gratings; (c) O₂/CHF₃ RIE patterned 40 nm wide SiO₂ mid-layer; (d) oxygen RIE transferred 35 nm wide ARC gratings; (e) CF₄/H₂ RIE defined 35 nm gratings in thermal SiO₂ and (f) final 35 nm wide grating mold after cleaning.

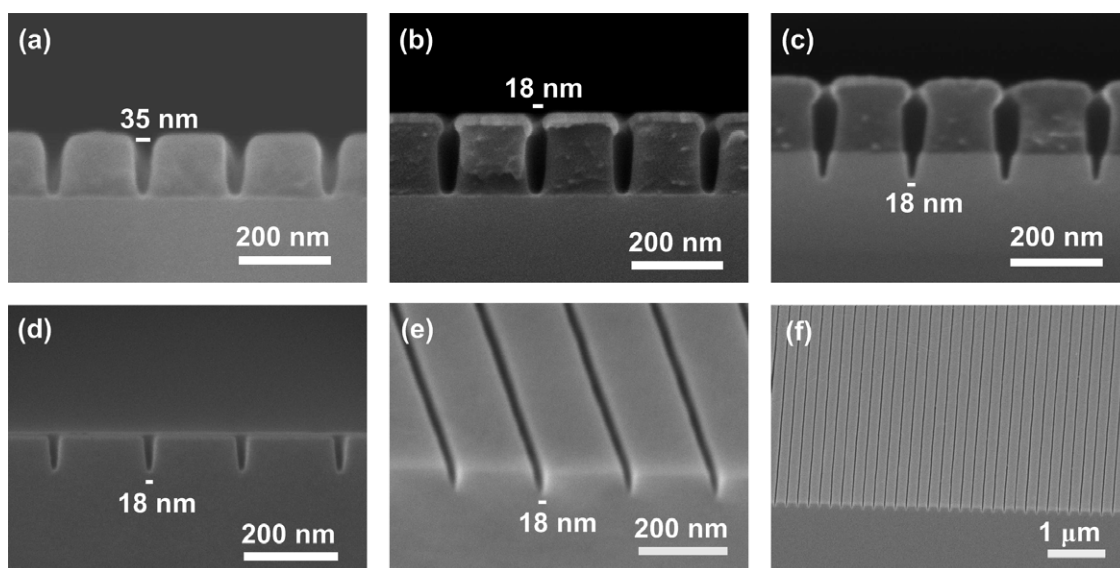


Figure 4. SEM images of the fabrication of a 18 nm wide trench mold in fused silica. (a)–(c) Cross-sectional images of the SiO₂ monitor sample: (a) as-imprinted 35 nm wide trenches in resist, (b) the bi-directional, Cr shadow evaporation defined, 18 nm wide gap Cr mask on resist and (c) 18 nm wide, 60 nm deep trenches in SiO₂. (d)–(f) Final trench mold in fused silica.

in CF₄/H₂ [26]. Finally, a 15 min RCA-1 cleaning stripped off the triple-layer resist (figure 3(f)), and the mold was vapor-treated with anti-sticking mold-release agent (NXT-110, Nanonex Corp., 110 °C, 30 min).

In the second trimming step (figures 2(h)–(k)), the daughter mold from the first trim was used to create a granddaughter mold, and a bi-directional shadow evaporation was used to reduce the feature dimensions. In particular, first, the daughter mold created a resist pattern (Nanonex NXR-1025) on the granddaughter mold substrate by nanoimprint (150 psi, 130 °C, 3 min), then the double Cr shadow

evaporations at an angle of 70° from the substrate surface normal and a thickness of ~10 nm in each direction were used to narrow the resist trench from 35 to ~18 nm (figure 4(b)). Finally, a pure CHF₃ RIE (10 sccm, 300 W, 4.5 mTorr, 10 min, Plasma-Therm PD 2486) was used to transfer the Cr pattern to the fused silica (granddaughter substrate), creating 18 nm wide and 60 nm deep trenches. The fabricated 4" fused silica mold (figures 4(d)–(f)) was also treated with mold-release agent (Nanonex NXT-110).

With the 20 nm linewidth granddaughter mold ready, we patterned and transfer-printed GNR arrays using the three-step

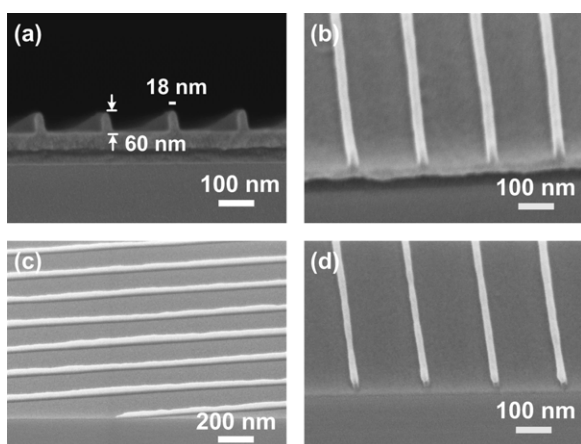


Figure 5. SEM images of pattern transfer of 18 nm wide gratings (Si monitor): (a)–(b) after UV NIL, (c)–(d) with the residual layer removed.

processing as mentioned above. In step (i), an HOPG block (SPI-1, $10 \times 10 \times 0.2 \text{ mm}^3$, Structure Probe, Inc.) was cleaved with Scotch tape to achieve a clean, fresh, and flat surface. UV NIL (100 psi, 3 min, UV 10 s) was performed, using the fabricated granddaughter fused silica trench mold (diced from a 4" wafer into $8 \times 8 \text{ mm}^2$ squares), to pattern sub-20 nm wide gratings in a double-layer resist (60 nm top-layer Nanonex NXR-2030, 60 nm sub-layer NXR-3022) coated on the HOPG surface. The imprint resist, rather than metal, was used as the etching mask, because it is a simpler process and free from metal contamination [27]. The double-layer UV resist, rather than a single layer, was used, because of its better patterning fidelity (less feature distortion from heating), good masking resistance for HOPG etching, and easy resist removal (resist NXR-3022 is water soluble and free from harsh resist remover).

In step (ii) of etching nano-graphene ribbons, RIE was used first to remove the residual top-layer resist ($\text{O}_2/\text{CHF}_3 = 1/10 \text{ sccm}$, 150 W, 5 mTorr) and then etched through the sub-layer resist and the HOPG (10 sccm O_2 , 75 W, 2 mTorr). The resist patterns on the silicon control sample (processed at the same condition with HOPG) are shown in figure 5. After

etching, the double-layer UV imprint resist was stripped in 1:1 mixed methanol and deionized water.

The GNR features (30 nm high and 18 nm wide) patterned on the HOPG stamp were studied by atomic force microscopy (AFM) imaging (figure 6(a)) and SEM imaging (figure 6(b)), respectively. The GNR patterns on the stamp span uniformly over isolated areas of $>5000 \mu\text{m}^2$ ($\sim 900 \mu\text{m}^2$ shown in figure 6(c) for visualization), sufficient to fabricate functional devices and circuits, e.g. transistors, bio-sensors, nano-optics, etc, for research demonstration purposes.

In this work, the GNR patterning area was limited to 20–30% coverage on the stamp by defects during the NIL step, which were generated by two main factors: (a) a non-flat HOPG surface and (b) non-uniform resist flow during imprint caused by large HOPG bending due to its low shear modulus (2–4 GPa [28, 29], i.e. 20 times smaller than silicon [30]). By better smoothing the HOPG surface and adjusting the imprint parameters, the defects could be significantly reduced and a good GNR area could be increased. With the fabricated 4" imprint mold, the same technology can be extended to the wafer scale, if a wafer scale of HOPG wafers or epitaxial graphene [31] wafers are available.

In the processing step (iii), the electrostatic force assisted printing transferred the GNR from the patterned HOPG stamp to a SiO_2 wafer substrate. A home-made setup was used that has two Al holders for the wafer and the stamp. The wafer holder and stamp holder mechanically bonded and electrically connected to the wafer (Si resistivity 0.01–0.02 $\Omega \text{ cm}$, 5 nm SiO_2) and the HOPG stamp, respectively. In exfoliation, the stamp holder was first mechanically pressed onto the wafer, causing an initial contact between the GNR on the stamp and the SiO_2 surface of the wafer. Then a 2 V voltage was applied between the stamp and the SiO_2 surface for 1 min (with $\sim 20 \text{ N}$ holding force). The voltage used was 2 V to avoid breaking down of the 5 nm SiO_2 layer on the Si wafer. The polarity of the voltage was not observed to affect transfer-printing, as it does not affect the magnitude of the electrostatic force. Finally, the wafer was removed and the voltage was turned off.

The mechanical holding pressure is calculated as $\sim 37 \text{ psi}$, using an estimated contact area of $\sim 77 \text{ mm}^2$, which includes both the unpatterned graphite ($\sim 75 \text{ mm}^2$, i.e. 70–80% of

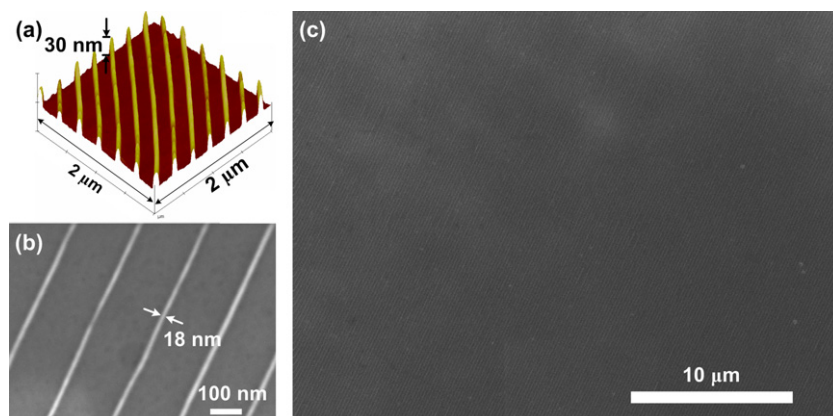


Figure 6. Patterned GNR arrays on HOPG after resist removal. (a) Side-view of AFM images ($2 \times 2 \mu\text{m}^2$). (b) and (c) Top-view SEM images. (This figure is in colour only in the electronic version)

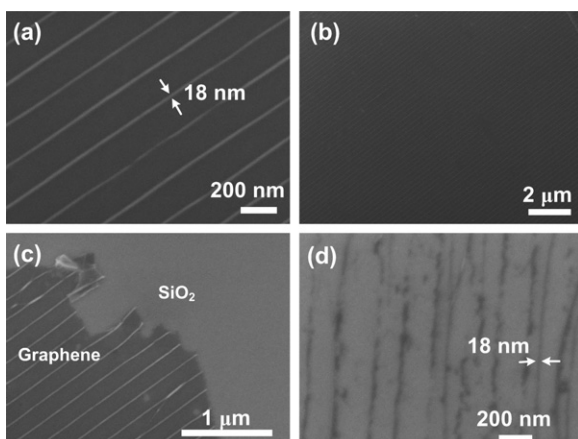


Figure 7. SEM images of GNR arrays transferred onto SiO₂ wafers: (a) and (b) high- and low-magnification images of graphene ribbons; (c) a layer of graphene sheet attached to GNR arrays; (d) few-layer GNR arrays.

100 mm² stamp) and graphene ribbon areas in patterned regions (~2 mm², i.e. 20–30% of stamp area times the ribbon duty cycle 0.09). On the other hand, the electrostatic force applied between the graphite and Si substrate can be calculated as ~200 psi using $P = \frac{\epsilon_0 \epsilon_r V^2}{2d^2}$ (5 nm SiO₂, voltage 2 V), derived from a simplified plate capacitor model. Clearly the electrostatic force is much larger than other pressing forces used, and allows a uniform pressure on the micro/nanoscale in contact areas over the entire sample [32]. Once a good and uniform contact is made, the GNR can be adhered to the clean SiO₂ surface of the wafer. With the good adhesion, when the stamp and the wafer are separated, a thin layer of GNR is attached to the wafer and is exfoliated from the stamp. Without an applied voltage, a much smaller area of graphene, estimated to be ~10% of the transferred area when with the voltage, was transferred, showing the importance of electrostatic pressure in the pattern transfer.

After electrostatic exfoliation, 18 nm uniform graphene ribbons were transferred to the SiO₂/Si wafer (figure 7). Compared to other patterning approaches such as chemical derivation [6] and EBL writing [20] which inherently have a large size variation and/or line-edge roughness, nanoimprint, in combination with other techniques [33–35], is capable of patterning the nano-ribbons more accurately and uniformly (figures 7(a) and (b)), which is critical for homogeneous GNR device performance.

In this work, the current largest transferred GNR area was about 500 μm² (~130 μm² shown in figure 7(b)), smaller than that patterned on the stamp. The reason could be attributed to non-perfect contact between SiO₂/Si wafer and HOPG stamp, caused by defects on the stamp and/or non-parallel alignment of the stamp to the Si wafer.

We observed that the thickness of transfer-printed graphene nano-ribbon arrays was 1–5 nm (from SEM images, figure 7(d)) in some areas (spots of ~200 μm²), however in other areas additional graphene layers (~20 to ~60 nm thick) were detached from the stamp and transferred onto SiO₂ (figure 7(c)). These few-layer graphene ribbons (figure 7(d))

were 5–10 μm long, sufficient to make functional devices. The undesired additional graphene layers (figure 7(c)) could be reduced or eliminated by minimizing HOPG stamp bending in exfoliation and better contacting the stamp with SiO₂. The GNR production yield and uniformity could be improved by cutting the GNR arrays on the HOPG stamp into designed transistor lengths, which should allow a more uniform local contact and better exfoliation.

In summary, we have proposed and demonstrated a method of patterning 18 nm wide graphene ribbons on HOPG by NIL (over an area of >5000 μm²) and transferring them to SiO₂/Si substrate via electrostatic force assisted printing. We believe the yield of GNR arrays could be further improved by optimizing nano-patterning and transfer-printing processing parameters. We also demonstrated an approach to shrink feature size over wafer scale from 120 nm to sub-20 nm, i.e. six-fold downsizing, using a technique combining tri-layer shrinking and shadow evaporation, which could be optimized to pattern the GNR width to the sub-10 nm regime for larger bandgap [6, 11, 14]. Our nano-patterning method is also convertible to a roll-to-roll [36] based NIL process, applicable to pattern graphene produced by other methods, e.g. chemical derivation [37] or catalyzed growth [31], and suitable for many other nano-fabrication and device applications.

Acknowledgment

The authors would like to thank the National Science Foundation (NSF) for their partial support of this work.

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