Lateral Resonant Tunneling Transistors Employing Field-Induced Quantum Wells and Barriers

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Future scaled transistors may well have dimensions significantly less than 100 nm and be operated at temperatures low enough for quantum effects to be appreciable. Such effects, while undesirable for conventional transistors, may be put to good use in future devices. We describe here some preliminary experimental results of quantum-effect modulation-doped field-effect transistors (MODFET's) with a variety of nanometer gate geometries. The gate geometries were such that various quantum wells and barriers were formed in the channel of the MODFET's through the field effect imposed by the novel gate structures, and that the transport of the electrons was affected by resonant tunneling. The devices were fabricated using a combination of molecular beam epitaxy and electron beam lithography. Electrical measurements of the devices at 4.2 K showed resonant tunneling effects and, in particular, showed that resonant tunneling is more pronounced for a system of quantum wells confined in three dimensions than in two. For these quantum effects to be appreciable at practical temperatures, say 77 K, the feature size of the gate geometries should be smaller than 50 nm.

I. Introduction

To improve speed and performance of integrated circuits (IC's), the minimum feature size of transistors has been shrinking from 100 μm for the first IC's (1959) to 0.75 μm for current industrial state-of-the-art IC's. If the trend of the miniature continues, it is expected that in the next 10–15 years the minimum feature size will be reduced below 100 nm. In active regions smaller than 100 nm, electrons may suffer little or no scattering, and may no longer behave as classical particles. In the first case, electrons will move as ballistic particles and drift-diffusion theory that governs the operation of conventional semiconductor devices has to be modified. In the second case, wave properties of electrons will dominate their transport, the drift-diffusion model fails completely, and quantum mechanics must be used to describe motion of the electrons.

Semiconductor devices based on quantum effects of electrons, so called quantum-effect devices (QED's), have many unique advantages over conventional transistors. First, QED's employ dimensions below 100 nm and generally work better as the size becomes smaller; therefore, they may well be suitable for future high density IC's. Secondly, they can be faster. Thirdly, they can perform functions that cannot be performed by a single conventional transistor. This feature can reduce, in many circuits, the total number of transistors required and hence increase speed and performance of IC's. Fourthly, there are many new ways to couple these QED's, and therefore, they may offer solutions to the interconnection problem which is a serious hurdle we must overcome in order to increase the speed of IC's as the scale of integration increases.

Due to rapid development in microelectronics technology, we now have advanced tools to fabricate QED's. Using epitaxial crystal growth technology such as molecular beam epitaxy (MBE) and metal–organic chemical vapor deposition (MOCVD) we can grow high quality artificial crystal layers whose thickness can be controlled down to one mono-atomic layer ($\sim$2 Å) and whose energy bandgap can be tailored, for example, [1], [2]. Using high resolution lithography (e.g., electron beam lithography) and other advanced fabrication technology such as reactive ion etching, we can fabricate, in the lateral direction, metal and semiconductor features with linewidths of 10 nm, for example, [3]–[6]. Semiconductor devices and circuits with feature size less than 100 nm have been reported, for example, [7]–[9].

QED's can be divided into two classes according to whether electron transport is in the direction normal to the

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wafer surface (vertical QED's) or parallel to the surface (lateral QED's). Vertical QED's usually employ the quantum-well structures grown by an epitaxial crystal growth method. Lateral QED's usually require a lithography method to define the quantum wells. The beginning of QED's can be traced back to the proposal of forming one-dimensional superlattice using alternating semiconductor crystal layers by Esaki and Tsu in 1970 [10]. The superlattice potential will create additional subbands and miniband gaps, and therefore can modulate the current–voltage characteristics and generate negative differential resistance. The vertical superlattice was first demonstrated by Esaki and Chang using GaAs–AlAs superlattice grown by MBE in 1974 [11]. On the other hand, the beginning of lateral QED's can be traced back to the independent proposals by Sasaki [12] in 1976 and Bate [13] in 1977 on forming lateral one-dimensional superlattice potential in the channel of a metal–oxide–semiconductor field-effect transistor (MOSFET) using a periodic electrical field induced by a grating gate. Stile in 1978 suggested replacing the grating gate with a grid gate; therefore, the superlattice potential in a FET becomes two dimensional [14]. In 1985, Warren, Antoniadis, Melngailis, and Smith at MIT first fabricated a silicon MOSFET with a grating gate of a 200 nm period [15]. Recently, negative differential resistances have been demonstrated in GaAs modulation-doped FET's (MODFET's) with a grating gate and a grid gate by Ismail, Chu, Antoniadis, and Smith [16], [17].

Another class of lateral QED's—resonant tunneling FET's (RTFET's)—was proposed by the authors in 1987 [18]. An RTFET has a structure similar to a MODFET, except the single planar gate is replaced by several closely placed nanometer gate electrodes. These gates can induce, through electric field effect, potential barriers and quantum wells in the channel of a FET. An example of RTFET's is the triple-gate device as depicted in Fig. 1. The operation of an RTFET is based on resonant tunneling of electrons from the source to the drain through the field-induced quantum wells. An RTFET differs from a vertical resonant tunneling transistor in many ways. First, in an RTFET, the barrier height and quantum-well depth can be adjusted continuously and independently to control the resonant tunneling. While in a vertical resonant tunneling (RT) transistor, the barrier height and quantum-well depth are fixed once the wafer is grown, and resonant tunneling is achieved by moving the entire quantum well. Secondly, it is very flexible to define the shape and geometry of the gates of an RTFET. As we will show later, this feature allows one to design various interesting quantum systems, including systems confined in three dimensions, which in general have much stronger quantum effects than one- or two-dimensionally confined systems. Thirdly, in an RTFET, the gates and quantum wells are coupled capacitively; therefore, very little gate leakage current and very little power is needed to switch the device. But in a vertical RT transistor, the quantum well is ohmically contacted, which results in large leakage currents and greater power to switch the device. Finally, RTFET's have a planar structure which is more suitable for circuit integration. Because of these features, RTFET's offer the potential of unique systems for studying quantum transport and exploring new QED's.

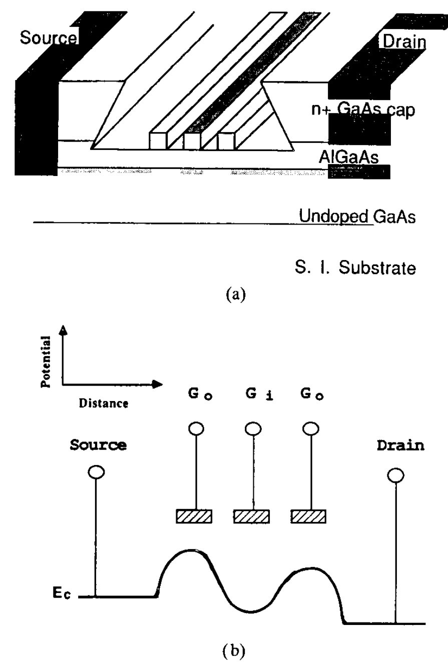


Fig. 1. (a) Schematic of a lateral resonant tunneling FET which has three close placed finger gates. (b) Schematic of energy band diagram of the device.

II. When Quantum Effects Become Dominant

Before going into the details of RTFET's, we would like to first discuss when quantum effects will dominate the transport of electrons in a semiconductor device. If scattering and thermal effects are ignored for the moment, quantum effects due to the wave properties of electrons must be considered in the following two situations. One is for electrons confined in a region of a size that is comparable with the deBroglie wavelength of electrons. In this case, the spacing between two allowed energy levels is about the same order of magnitude as the kinetic energy itself, which is significant enough to invoke quantum mechanics. The wavelength of an electron, λ, is related to its kinetic energy, E, by

$$\lambda = \frac{\hbar}{\sqrt{2m^* E}} \tag{1}$$

where m^* is the effective-mass of an electron in a semiconductor and $\hbar$ is Planck's constant. The relation is plotted in Fig. 2 for two different semiconductors, GaAs and InAs. From the figure we can see that if the electrons are confined to a region of 100 nm across, then quantum effects become significant for electrons with kinetic energy of 55 meV or less in GaAs and 170 meV or less in InAs (the energy corresponds to five times the electron wavelength).

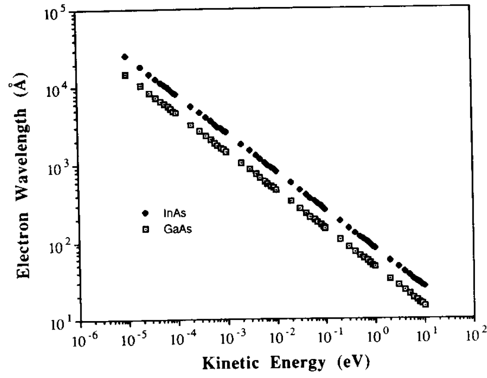


Fig. 2. Electron wavelength versus electron kinetic energy in GaAs and InAs.

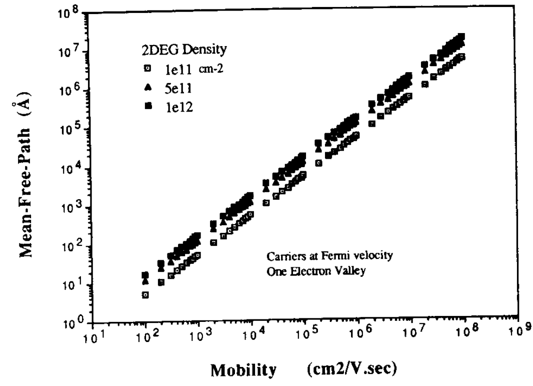


Fig. 3. Mean-free-path of two-dimensional electron gas versus mobility at electron densities of 10^{11}, $5 \cdot 10^{11}$, and 10^{12} cm^{-2}.

The second situation is when the thickness of a potential barrier is comparable with or less than the imaginary wavelength of an electron inside the barrier. In this case, the electron has a very good chance of penetrating (tunneling through) the barrier. If we change the kinetic energy in Fig. 2 to the barrier height that an electron sees, the wavelength will become the imaginary wavelength of the electron inside the barrier. For a 0.1-eV barrier, an electron can tunnel rather easily through the barrier of a thickness up to about 20 nm in GaAs and ~30 nm in InAs.

Both scattering and thermal effects tend to destroy quantum effects. Scattering will randomize the phase of quantum wave of electrons, and therefore destroy quantum-wave interference and quantum effects. In order to observe a quantum effect, electrons should not be scattered in the region of interest, and therefore, the mean-free-path of electrons has to be longer than the size where the quantum effect occurs. In practice, one can determine the mean-free path, l, from the mobility, μ. The relation between l and μ for a two-dimensional electron gas system is given by

$$l = \frac{\hbar\mu}{q}\sqrt{2\pi n} \qquad (2)$$

where n is electron concentration per unit area, q is the magnitude of electron charge, $\hbar$ is Planck's constant over 2π (Fig. 3). In deriving the above equation we assumed that electrons travel at the Fermi velocity, and that there is only one electron valley. Note that the mean-free-path is independent of electron mass. From Fig. 3 we see that to observe a quantum effect in region of 100 nm, the mobility should be greater than 10^4 cm^2/V · s. Another way to look at this is that scattering broadens an energy level through the uncertainty principle $\Delta E_{sc} = \hbar/\tau$, where τ is the scattering time. If the energy broadening, ΔE_{sc}, is larger than the spacing between two quantum levels, the energy levels will not be distinguished. Thus ΔE_{sc} represents the minimum energy spacing which is observable when scattering exists. The relation between ΔE_{sc} and the mobility is given by

$$\Delta E_{sc} = \frac{\hbar q}{\mu m^*} \qquad (3)$$

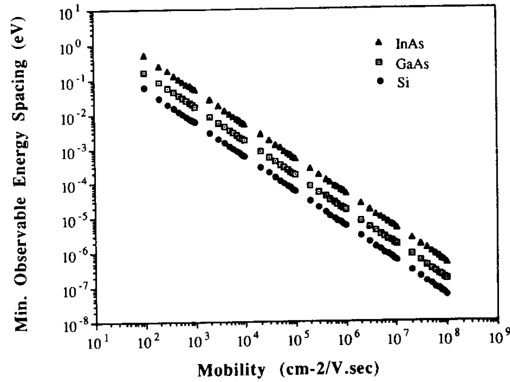


Fig. 4. The minimum observable energy spacing versus electron mobility in GaAs, InAs, and Si.

and is plotted in Fig. 4.

Thermal effects will cause the initial distribution of electron energy to have a width of kT, where k is the Boltzmann constant and T is the temperature. Certainly, if this energy distribution width is significantly larger than a quantum level spacing, then the quantum effect will not be observable. Therefore, in order to observe a quantum effect, the spacing between two neighboring quantum levels must be larger than the energy broadening caused by scattering and thermal effects.

III. Device Structures and Operating Principles

The first lateral resonant tunneling FET proposed (Fig. 1) has a structure similar to a MODFET, except that it has three finger gates placed close to each other instead of a single gate; each finger gate can be biased independently [18]. The two outer gates can be biased in such way that they deplete charges underneath them and therefore form two potential barriers in the channel of the FET. The inner gate can be used to control the charge concentration below it and hence the depth of the potential well. Since these gates

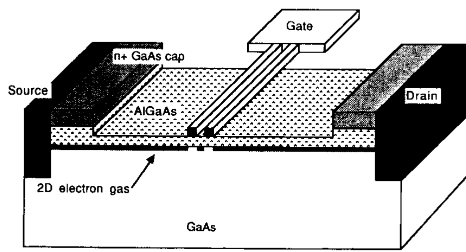


Fig. 5. Schematic of a lateral RTFET which has dual closely placed finger gates.

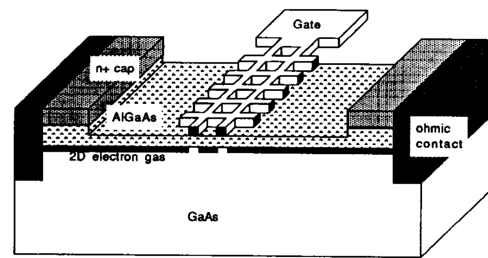


Fig. 6. Schematic of a lateral RTFET which has a railway gate.

usually have width and spacing in a range of sub-100 nm, they can induce a double barrier quantum well in the channel of a FET, and electron energy in the quantum well is quantized. By controlling the voltages on each individual gate, one can change the barrier height or the quantum-well depth, and therefore, the values of allowed electron energy levels in the well. Matching an energy level in the well to that of an electron at the source maximizes the probability of these electrons tunneling through the double potential barriers and reaching the drain side. We call this matched situation resonant tunneling of electrons. If the energy does not match, the chance of tunneling becomes very small. Experimentally, the source–drain current is large when the majority of electrons at the source are in resonance and small when off resonance.

From Fig. 1(b), we can see that there are several ways to operate the triple-gate RTFET to achieve resonant tunneling of electrons from the source to the drain. In the first mode, the potentials at the outer gates and between the source and the drain are fixed, and the inner gate potential is varied to change the depth of the quantum well. The change of the well depth will make the energy levels in the well move up or down relative to the source, and cause resonant tunneling when an energy level in the well matches the energy of the electrons at the source. In the second operation mode, the potentials at the inner gate and between the source and the drain are fixed; the outer gate potentials are changed. The change varies the barrier height, and therefore moves the energy levels in the well up or down, creating resonant tunneling. In the third operation mode, just like in a resonant tunneling diode, the potential between the source and the drain is varied to make the energy levels in the well move, generating resonant tunneling. In the fourth mode, a backgate could be used to adjust the electron concentration in the channel and, therefore, to adjust the Fermi level and conditions for resonant tunneling. Certainly, resonant tunneling can also occur by using combinations of the above four operation modes.

One variation of the multi-gate RTFET is the double gate version (Fig. 5) which is easier to make than the triple-gate RTFET, but, obviously, it can be only operated in modes 2, 3, or 4. The two gates can be connected to two independent contacts and so biased separately.

In the triple-gate and dual-gate RTFET's, the energy of the electrons in the quantum well are quantized only in two directions: vertically to the wafer and along the channel. However, in the direction across the channel (along the gate finger) the electron energy is continuous, thus allowing electron scattering in that direction. From the discussion of Section II we know that scattering tends to suppress quantum effects. To reduce such scattering and to enhance quantum effects, we can put partitions along the gate fingers (Fig. 6), so that the quantum wire becomes an array of quantum boxes, and the energy of the electrons in the box is quantized in all three dimensions [19].

From the above discussions, the unique advantages of RTFET's mentioned in Section I become very apparent; these are: a) tunable potential barrier height and tunable quantum-well depth, b) freedom and flexibility in defining gates to construct various quantum systems, c) capacitive coupling to the quantum well and barriers leading to a little gate current and small power needed to switch, and d) planar structure suitable for high density circuit integration. The first and second advantages of RTFET's make them versatile research vehicle for investigating quantum effects and exploring new QED's.

RTFET's do have shortcomings. First, due to the resolution of current lithography technology the gate width and spacing are in the range of 20–100 nm, which is about an order of magnitude larger than a typical size of quantum well and barriers in vertical QED's. This should be ameliorated as the lithography technology advances. Secondly, in RTFET's the potential barrier height, the wall of the potential barriers, and the quantum-well depth are not as high, abrupt, and deep as those in a vertical RT transistor. One of the reasons is that the potentials on the gates will get screened and reduced rapidly from the surface of a MODFET to the channel. To minimize this problem, some novel techniques have to be used to put the gates very close to the channel and keep the channel mobility significantly high at the same time.

Finally, it should be pointed out that some of these multiple-gate FET's also can operate classically. In this case, the gates are used to create a favorable electrical field distribution for transport, or to influence the electric fields of neighboring gates for some special device functions such as shifting the threshold voltage of a FET. An example of such applications is the split-gate FET proposed by Shur [20].

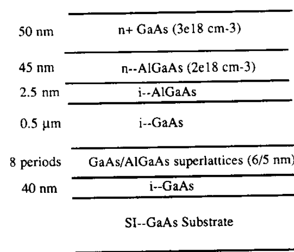


Fig. 7. Schematic of a MODFET structure for an RTFET.

IV. Fabrication

Because RTFET's and MODFET's have similar structures, their fabrication is also similar except that more care has to be taken in defining the gate electrodes which have a size of a nanometer scale. The fabrication process generally consists of five major steps: MBE growth, ohmic contacts, isolation, gate definition, and final metal contacts. Here we discuss one of our fabrication processes.

A modulation-doped structure (Fig. 7) was grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE) at a substrate temperature of 580 °C. A 40-nm GaAs layer was grown first followed by 8 periods of $Al_{0.3}Ga_{0.7}As/GaAs$ superlattice (6/5 nm), and a 0.5-μm thick GaAs buffer layer. Then grown were a 2.5-nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, a 45-nm doped $Al_{0.3}Ga_{0.7}As$ layer with Si doping concentration of $2 \cdot 10^{18}$ cm^{-3}, and a 50-nm doped GaAs layer with Si doping concentration of $3 \cdot 10^{18}$ cm^{-3}. The sheet resistance for this wafer was 250 Ω/sq. More recently we have fabricated devices on a wafer with thicker AlGaAs spacer layer, 6 nm, and a very thin n^+GaAs cap, 10 nm. The thicker spacer layer increases the electron mobility at the heterojunction interface by reducing the coulomb scattering. The cap layer is so thin that the gate electrodes can be placed directly on top, avoiding recess of the gate area and simplifying the fabrication sequence. Furthermore, to reduce DX centers, the doped AlGaAs in some samples was replaced with five periods of $Al_{0.3}Ga_{0.7}As/GaAs$ superlattice where only the GaAs layers were doped.

In device fabrication, optical lithography was used for all levels except the gate electrodes which were defined by e-beam lithography. The ohmic contact metallization was 40 nm of Au, 10 nm of Ge, 12.5 nm of Ni, and 150 nm of Au deposited sequentially with e-beam evaporation and then lifted off in acetone. This contact was rapidly annealed at 450 °C for 30 s in forming gas. The contact resistance for the wafer with the thick cap layer was 0.2 Ω · mm. As expected, the wafer with the thin cap layer had a much higher contact resistance of 2.5 Ω · mm. The relatively high resistance in the latter case reduces the extrinsic transconductance, but it is not particularly important for these QED's because the conductance oscillations usually occur at a drain current on the order of 10 nA (for a 7-μm wide channel).

The devices were then isolated with dual argon ion implantations masked by 600 nm of plasma enhanced chemical vapor deposition (PECVD) SiOx. The two implant energies were 50 and 130 keV; the dose for each implant was optimized to $1.5 \cdot 10^{12}$ cm^{-2}. This combination successfully disordered the n^+ cap layer as well as the heterojunction interface resulting in an isolation resistance greater than 10^7 Ω between devices at room temperature (480-μm device separation). Planar implantation isolation was used because of the difficulty of fabricating continuous nanometer scale gate electrodes over the mesa edges left by wet etching isolation.

For the wafer with the thick (50 nm) n^+GaAs cap layer, a broad recess etch over the gate area was necessary. The recess area for a 10-μm source–drain spacing is 5-μm long by the device channel width. A selective wet etch (1:200 $NH_4OH:H_2O_2$), that stops at the surface of the AlGaAs, was used.

The nanometer gate electrodes were defined by writing on a 70-nm thick PMMA layer with a high resolution electron beam lithography system. The resist was spin cast from a 2% solution of PMMA with a molecular weight of 950 K in chlorobenzene. The spin speed was 8000 rpm for 30 s to minimize resist nonuniformity. The resist was prebaked for 4 h at 175 °C. The high resolution electron beam lithography system used for exposing the gates was a custom-built system [19], [5]. The beam diameter was about 2 nm and the accelerating voltage was 40 keV. The line exposure doses ranged from 0.5 to 5 nC/cm, depending on geometry of the gates and the proximity effect. After e-beam exposure, the PMMA was developed in 3:7 cellosolve:methanol followed by a methanol rinse. The gate electrode was formed by evaporation of Ti/Au (15/15 nm) and metal lift-off in acetone. Finally, large contact pads for the source, gate, and drain were formed by optical lithography, e-beam evaporation of Ti/Au (20/300 nm), and lift-off in acetone. The devices were then cleaved and bonded into packages for testing.

Figure 8 shows the electron micrographs of the triple gates, dual gates, and railway gates for RTFET's. The triple gates are 90 nm wide and 60 nm apart. The dual gates are 80 nm wide and 100 nm apart. For the railway gates, the width of the ties and rails is 50 nm, and the spacing between the two rails and between the ties are 150 and 230 nm, respectively. Recently, a novel technique has been developed that can fabricate double 17-nm gates separated by 15 nm on GaAs, as shown in Fig. 9 [6].

V. Electrical Characteristics

To compare device performance, single-gate MODFET's with gate lengths from 80 to 300 nm were also fabricated on the same substrate as the dual-gate and railway-gate RTFET's. At room temperature, the current–voltage characteristics of RTFET's are similar to those of the single-gate short channel devices, and no quantum effects were observed, since the quantum level spacings in these quantum device are much less than the energy broadening due to thermal excitation, 26 meV. At 4.2 K, in the dark and at a source–drain voltage of 0.5 mV, the single-gate

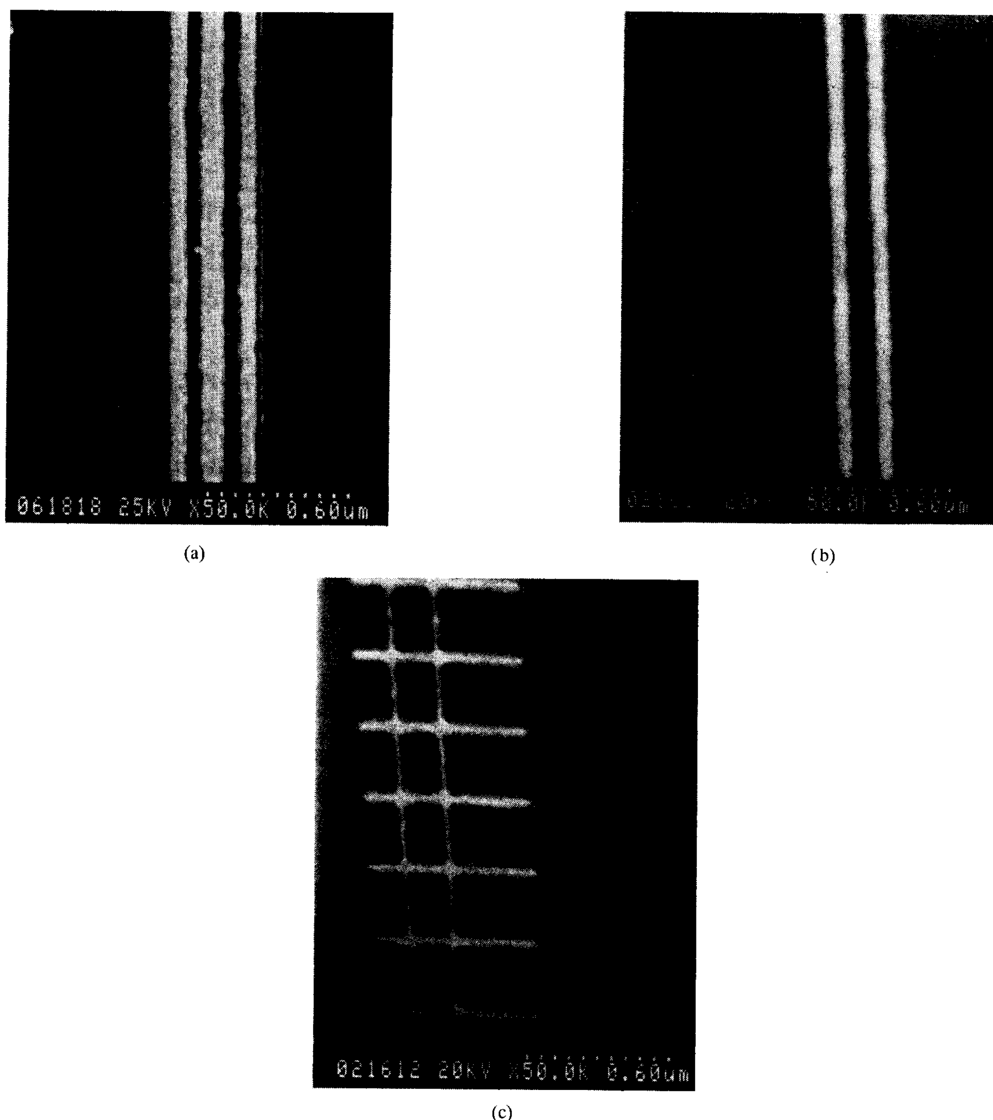
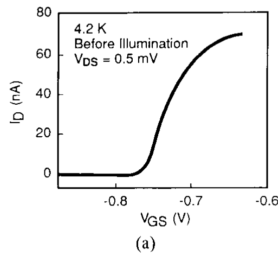


Fig. 8. Scanning electron micrographs of (a) triple Ti/Au gates, (b) dual gates, and (c) railway gates on GaAs.

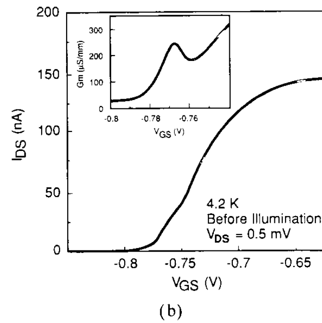
MODFET has a typical smooth turn on in the drain current versus the gate voltage curve, as shown in Fig. 10(a). Unlike the control device, a single oscillation in the drain current is clearly visible for a dual-gate RTFET which has two 80-nm gates separated by 100 nm, as shown in Fig. 10(b) [21]. It is interesting to note that although there are many quasi-bound states in the quantum well, only one shoulder is observable in the current measurement. We believe that this is because the energy separations between quantum levels in the well are very small and the separations decrease continuously as the gate bias become less negative (due to barrier height lowering), therefore only the first resonance is observable. To get an idea of the energy separation we use the parabolic well model. Assuming that the barrier height is 50 meV and the width of the well is 180 nm, the energy separation between levels, $\Delta E = \hbar\omega = 3.7$ meV. The conductance variation decreases as the source–drain voltage increases, and disappears when the source–drain voltage exceeds 5 mV. This observation is consistent with the fact of a small energy level separation, since the increase in electron temperature due to heating caused by the source–drain bias will eventually mask the quantum effect.

In a railway-gate RTFET (with the ties and the rails each of 50 nm wide, and the spacings between the rails and between the ties of 150 and 230 nm, respectively), five stronger conductance oscillations have been observed, as shown in Fig. 11 [22]. Furthermore, we found that more than 50 mV of the drain voltage can be applied before the oscillations disappear. This voltage is an order

Fig. 9. Scanning electron micrograph of dual Ti/Au gates 17-nm wide and separated by 15 nm on GaAs.



(a)



(b)

Fig. 10. The drain current versus the gate voltage at a fixed drain voltage of 0.5 mV at 4.2 K without illumination for (a) the single 80-nm gate control device exhibiting a smooth turn-on and (b) the dual gates RESFET with two 80-nm gates separated by 10-nm exhibiting a current peak.

of magnitude higher than that for the dual-gates RTFET. These observations indicate that the additional confinement of electrons indeed enhanced the quantization effects. The periodicity of the conductance oscillations becomes smaller as the gate voltage becomes less negative, consistent with the fact that increasing the gate voltage decreases the barrier heights and decreases the separation of the quasi-bound states. The separation of the states is roughly proportional to the square root of the depth of the well. All measurements mentioned above were made in the dark. These observations may be repeated after thermally cycling the devices.

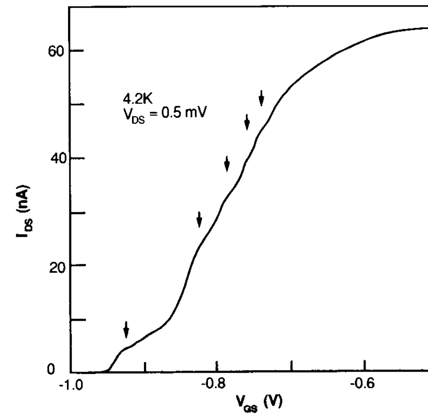


Fig. 11. The drain current versus the gate voltage with a drain bias of 0.5 mV at 4.2 K without illumination for the railway gate RTFET. The arrows indicate the approximate location of the current peaks.

The strength of the oscillations observed in all these RTFET's is somewhat less than what we expected. We attribute this to low electron mobility in the channel. It is likely that the thickness of SiOx layer used for masking the isolation implantation was not thick enough, and some implanted ions entered the channel region and caused lattice damage, degrading the channel mobility. Recently, the group at MIT has demonstrated that the conductance oscillations in a dual-gate RTFET can be very strong if the mobility is high [23].

Finally, we would like to point out that single-gate control devices fabricated on the same substrate are necessary for interpreting the conductance oscillations observed at 4.2 K in RTFET's. In our early experiments, two conductance oscillations were observed at 4.2 K in a single-80-nm gate MODFET after illuminating the device (Fig. 12(a)), whereas no such oscillations were observed before the illumination. A nearby double-80-nm gate RTFET showing only one oscillation before illumination showed three after illumination (Fig. 12(b)). Examination of these oscillations showed that the two peaks in the single-gate FET matched the two in the dual-gate RTFET—in that in both cases the separation of the peak is 26 meV. In our later devices, the MODFET's structure has a larger AlGaAs spacer, low Al mole fraction, and less Si doping. Under these conditions single-gate FET's do not show any conductance oscillations after illumination, indicating that these additional oscillations might be caused by the donor-related deep levels (DX centers) in doped AlGaAs, which are known to have two major deep levels that can extend into GaAs [24], [25].

VI. Conclusion

As a semiconductor device is scaled down to the sub-100-nm regime, the conventional treatment of a transistor begins to break down, and ballistic and quantum-wave properties

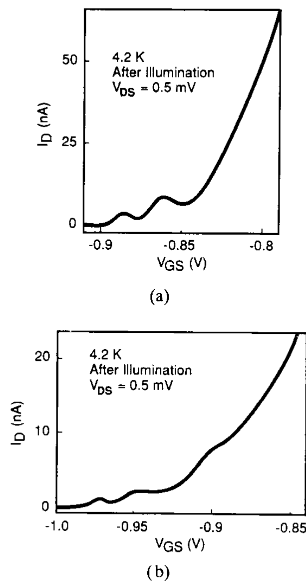


Fig. 12. The drain current as a function of the gate voltage with a 0.5 mV drain voltage at 4.2 K after illumination for (a) the single 80-nm gate control device and (b) a dual 80-nm gate device.

of electrons start to play an important role in device operation. The concept of resonant tunneling field-effect transistors has been demonstrated in two device configurations: a dual-gate RTFET and a railway-gate RTFET. By comparing the characteristics of these two devices, we have shown that quantum effects are stronger in a three-dimensionally confined system than in a two-dimensionally confined system. Currently, the RTFET's have to work at low temperatures and with low source–drain voltages because the energy level spacing in RTFET's is rather small, limited by present resolution of the lithography. As nanometer lithography and fabrication further improve, one can expect that these devices will exhibit quantum effects at higher temperatures and with stronger bias voltages. Already, however the unique features of RTFET's, such as tunable barrier heights, tunable quantum-well depths, and flexibility of creating a sophisticated quantum system by using various shapes and geometries of gates, make them a versatile vehicle for studying quantum transport effects and exploring new electronic devices.

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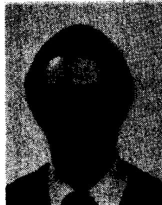

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