Sub-100-nm channel-length transistors fabricated using x-ray lithography

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Enhancement-mode n-channel Si field-effect transistors with channel lengths ranging from 60 nm to 5 μm have been fabricated using combined optical and x-ray lithographies, and were characterized from room temperature to 4.2 K. At room temperature, the 80 nm channel-length device showed quasi-long-channel behavior with high transconductance. At 4.2 K, a significant increase in transconductance was observed which may indicate velocity overshoot.

I. INTRODUCTION

Previous investigations have used scanning electron beam lithography (SEBL) in the fabrication of Si MOSFET's with channel lengths in the 0.1 μm range.[1-3] In the present work, we have used soft x-ray lithography. The x-ray mask was fabricated by a combination of conventional photolithography, anisotropic etching, and oblique shadowing—techniques which are accessible at low cost in a university laboratory. The use of x-ray lithography has particular significance in that it is compatible with mass production at high pixel transfer rate, in contrast to SEBL.[4] X-ray lithography with C_K or Cu_L sources is advantageous because patterns can be replicated with a precision $\lesssim 10$ nm.[5]

II. LITHOGRAPHY

Figure 1 illustrates the x-ray mask. It consists of a polyimide membrane supported on an Al ring. On the front side are narrow absorber lines corresponding to the short channels, and on the back side are coarse patterns corresponding to the source and drain implantation regions of the short-channel devices. Also on the back side are patterns for 5-μm-channel-length transistors. We believe this is the first time that x-ray masks with absorber patterns on both front and back have been used successfully.

The procedure for fabricating the x-ray mask has been described in detail elsewhere.[6] Here we give only a brief outline. Thermal oxide is grown on (110) Si wafers and patterned with rectangular windows using photolithography and buffered HF etching. Two parallel edges of the windows are aligned perpendicular to the ⟨111⟩ direction in the (110) plane. The Si is then etched anisotropically in a KOH/isopropyl alcohol/H_2O solution with the volume ratios 3 : 2 : 8. This yields wells with flat bottoms and two sidewalls that are close to {111} planes and extremely smooth on a scale $\lesssim 10$ nm. Next, the SiO_2 is removed and a 1-μm-thick layer of polyimide (Dupont PI 2555) spun on and cured. A film consisting of 10 nm of Cr and 150 nm of Au is then evaporated onto the polyimide. Rectangular openings, centered over one of the {111} sidewalls of the front-surface wells, are formed in the gold using photolithography and ion beam etching, and, at the same time, pairs of rectangular openings corresponding to source and drain implantation regions for 5-μm-channel-length devices are also formed in the gold. An Al ring is bonded to the polyimide and the (110) Si is removed in HF/HNO_3. The narrow absorber lines on the front side of the mask are formed by obliquely shadowing gold onto one of the smooth sidewalls of the rectangular mesas which are now in relief on the polyimide. The thickness of gold is readily adjusted, and, in fact, we always arranged to have four regions on the same mask, each with a different nominal gold thickness on the mesa sidewalls. In this way, resist patterns corresponding to four different nominal short-channel lengths would be exposed on the same Si wafer substrate, in addition to resist patterns for the 5-μm-channel-length devices. After shadowing, excess gold is removed from flat regions by ion beam etching.

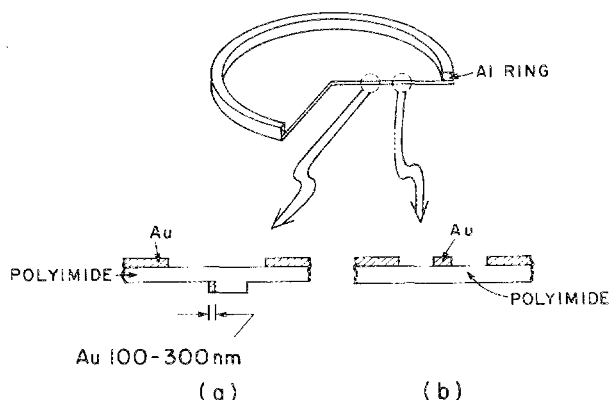

FIG. 1. Schematic of x-ray mask. (a) Absorber pattern for submicron MOSFET, on both front and back surfaces. (b) Absorber pattern of 5-μm-channel-length MOSFET, on back surface only.

In each region of the mask corresponding to a given nominal thickness of gold there were a large number of transistor patterns. The actual thickness of gold varied by about 10% of the nominal thickness from one edge of the region to the opposite edge. We believe this was due to partial obstruction of the gold evaporation. This small variation in gold thickness and the corresponding small variation in channel length about a nominal value proved extremely useful in determining channel length.

Exposures were carried out in a laboratory-built x-ray system using C_K radiation ($\lambda = 4.5$ nm). (Cu_L radiation, $\lambda = 1.33$ nm, could also have been used.[5]) The mask was held in intimate contact with the substrate by electrostatic means. After development in 40% methylisobutyl ketone/60% isopropyl alcohol, well-defined resist structures were obtained that are straight, reproducible, and nearly free

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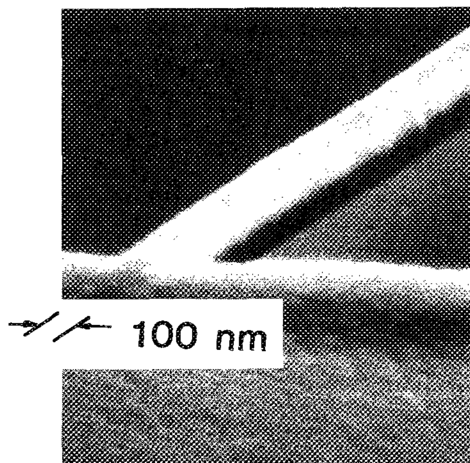

FIG. 2. (a) Scanning electron micrographs of PMMA resist pattern.

of edge ripple. This is shown in Fig. 2. What small ripple does occur is probably due to granularity of the evaporated Au. (Evaporated W would be free of such ripple.)

III. DEVICE FABRICATION

P-type (100) wafers of 20 Ω cm were implanted with B at 30 keV and a dose of 2×10^{13} cm^{-2}. This was followed by dry oxidation at 900 °C for 40 min, which increased the surface acceptor concentration to 5×10^{17} cm^{-3}. Devices did not have a self-aligned gate structure. Instead, the PMMA resist lines produced by the x-ray lithography (see Fig. 2) were used to mask the channels during source and drain ion implantation. This was done through a 20-nm-thick oxide with 30 keV As at 7×10^{15} cm^{-2}. A second implant, of P, was done in the contact areas, 5 μm away from the channel, to prevent punchthrough of Al when forming source and drain contacts. After As and P ion implantations, the PMMA and the oxide were removed and an 11-nm-thick gate oxide was grown at 900 °C for 25 min. This also served to anneal the damage caused by ion implantation. Next, a 0.4-μm-thick Al gate was formed using conventional projection photolithography and chemical etching. The Al gate was 4 μm wide and thus overlapped source and drain. The capacitance resulting from this overlap was not a problem since our interest was in evaluating the low frequency behavior of the short-channel devices. After forming the gate, 0.3 μm of CVD SiO_2 was deposited over the samples. Finally, contact cuts and Al contacts were made to the Al gate and source and drain regions.

IV. RESULTS

Figure 3 shows the *I–V* characteristics of the 60- and 80-nm-channel-length devices, and Fig. 4 shows subthreshold behavior for the latter device. Channel length was measured by two independent methods, both of which gave essentially identical results. One method depended on measuring the width of PMMA at which source and drain begin to overlap due to the combined effects of lateral ion scattering and diffusion during oxidation. This indicated a lateral spreading of the As beyond the edge of the PMMA of 80 nm on either side. Thus, the 60-nm-channel-length MOSFET was made from a PMMA stripe of 220 nm width. The second method extracted the channel length from electrical measurements, as proposed by Suciu and Johnston.[7] The variation of PMMA resist linewidth in a predictable way about a given nominal value, discussed above, was helpful in establishing the consistency of the two methods of measuring channel

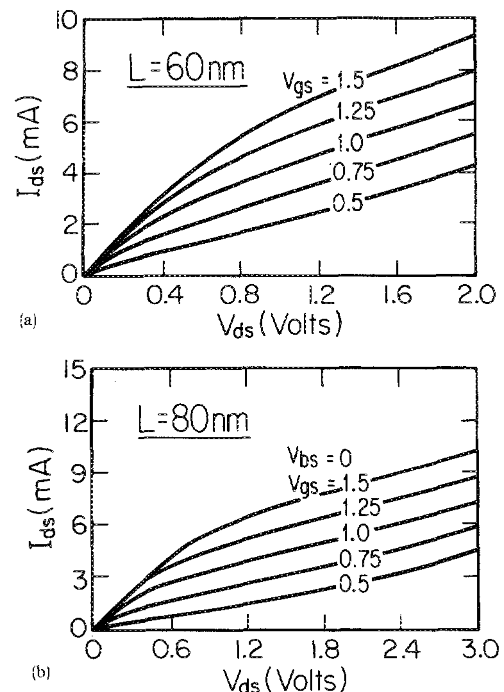

FIG. 3. *I–V* characteristics of (a) device with 60-nm-channel length; (b) device with 80-nm-channel length.

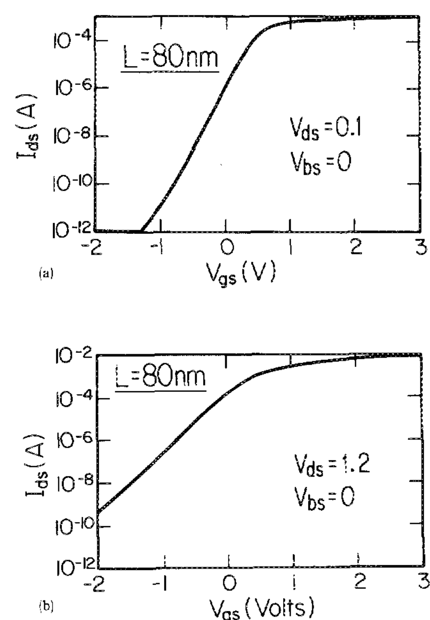

FIG. 4. Subthreshold characteristics of an 80-nm-channel MOSFET for (a) $V_{DS} = 0.1$ V; (b) $V_{DS} = 1.2$ V.

length. The 60-nm-channel-length device shows high drain conductance, as expected for a short-channel device. The 80-nm device shows quasi-long-channel behavior: threshold voltages of 0.35 V at $V_{DS} = 0.1$ V and 0.3 V at $V_{DS} = 1.2$ V. The saturated transconductance is 140 mS/mm. Parasitic sheet resistance for all our devices was 4.4 Ω mm, which is the major factor limiting transconductance. With proper design of source and drain doping profiles and contacts we believe this resistance can be reduced several fold. Taking the parasitic resistance into account one can calculate the intrinsic transconductance. We obtain 250 mS/mm.

From intrinsic transconductances g_{mi} the average electron velocity v_e can be calculated according to $v_e = g_{mi}/C_{ox}$, where C_{ox} is the capacitance of the gate oxide. At 4.2 K, we found that the average electron velocity in a 75-nm-channel MOSFET is 1.7×10^7 cm/s, which is 1.8 times higher than the electron saturation velocity in a Si inversion layer as reported by Fang and Fowler[8] and 1.3 times higher than the electron saturation velocity in bulk Si at 4.2 K [1.32×10^7 cm/s (Ref. 9)]. As channel length is increased, the average carrier velocity drops sharply. These experimental results strongly suggest that we have observed velocity overshoot in the 75-nm-channel-length MOSFET.[10]

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