

# Single-electron Coulomb blockade in a nanometer field-effect transistor with a single barrier

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The first experimental study of a new nanometer field-effect transistor with a single barrier in its one-dimensional channel is presented. At low temperatures and as charge density in the channel was varied, nine reproducible periodic oscillations of conductance, in addition to  $2e^2/h$  conductance plateaus, were observed before the onset of the first  $2e^2/h$  conductance plateau. It was found experimentally that each conductance oscillation corresponds to the Coulomb blockade of a single electron in the one-dimensional channel. A model that describes the operation of the new single electron transistor is suggested.

As the size of semiconductor devices continues to shrink, their capacitance may decrease to a point where the effects of single electron charging significantly affect device operation. Such Coulomb effects are not only interesting in physics, but also open up new possibilities for new electronic devices. Previously, the effects of single electron charging have been studied in metal films consisting of small metal particles<sup>1</sup> and in small metal junctions.<sup>2,3</sup> In some of these structures, conductance oscillations, although weak, were observed and explained as a result of single electron charging. In semiconductor devices, single electron Coulomb blockade in a field-effect transistor (FET) that has a quantum well confined between two barriers was reported.<sup>4</sup> In all previous single electron charging experiments, two or more barriers were used to retain a single electron. Such a structure was believed to be critical to single electron charging.

Here, we present the first experimental study of a nanometer FET with a *single* barrier in its one-dimensional channel and suggest a model for its operation. We report observing, in addition to  $2e^2/h$  conductance plateaus, nine reproducible periodic conductance oscillations before the onset of the first  $2e^2/h$  plateau, and we show that these oscillations are due to the Coulomb blockade of a single electron.

The single-barrier nanometer FET has a structure similar to a constricted-gate FET (also called split-gate FET in some literature), except that a metal barrier is placed in the middle of the gate gap. Using a negative gate bias, the electrons underneath the gate will be depleted, creating two one-dimensional (1D) channels separated by a single potential barrier [Fig. 1]. The gate was fabricated using ultrahigh resolution electron beam lithography and a liftoff process.<sup>5</sup> The width of the metal barrier and the gap between the two constricted gates were as small as 50 nm (Fig. 2). The single-barrier FET (SBFET) has a heterostructure, grown by MBE, consisting of a 500 nm thick layer of undoped GaAs on top of a semi-insulating GaAs substrate, followed by a 10 nm undoped  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  spacer layer, a 40 nm  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  layer doped with a Si concentration of  $1 \times 10^{18} \text{ cm}^{-3}$ , and a 15 nm GaAs cap layer with a Si doping concentration of  $1.4 \times 10^{18} \text{ cm}^{-3}$ . The two-dimensional electron gas (2DEG) formed at the

GaAs/AlGaAs interface had a Hall mobility of 120 000  $\text{cm}^2/\text{V s}$  and a carrier concentration of  $8.9 \times 10^{11} \text{ cm}^{-2}$  at 77 K in the dark. For comparison, constricted-gate FETs without any barriers were also fabricated on the same substrate.

The devices were cooled to 0.5 K using a sorption-pumped helium-3 refrigerator. Before cooling to 0.5 K, the devices were illuminated by a light-emitting diode (LED) at 10 K and were found to hold a constant 2DEG concentration at 0.5 K for hours. As the gate voltage was scanned, a SBFET with a 50 nm gate gap and a 50 nm wide metal bar showed nine repeatable periodic oscillation peaks in the drain current, in addition to  $2e^2/h$  conductance plateaus, before the onset of the first  $2e^2/h$  conductance plateau (Fig. 3). The oscillation period was 15 mV. Another SBFET with a 100 nm gate gap and a 50 nm wide metal bar showed five repeatable periodic oscillation peaks in the drain current with a periodicity of 9 mV before the onset of the first  $2e^2/h$  conductance plateau (Fig. 4). Such periodic conductance oscillation peaks were absent when the conductance of these devices was greater than  $2e^2/h$ . They were also absent in the devices that were fabricated on the same substrate but had a straight constricted gate of the same size without any barrier.

Interestingly, the conductance oscillations in Fig. 4, measured with a direct  $I$ - $V$  measurement using HP4145 semiconductor parameter analyzer, are much stronger than those in Fig. 3, which are measured with a lockin

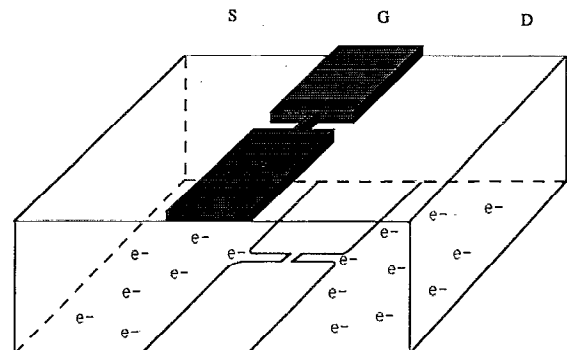


FIG. 1. Schematic of 2DEG in a nanometer FET with a 1D channel and a single barrier in the middle.

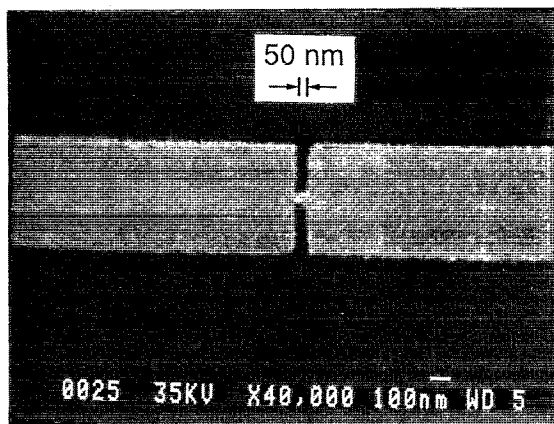


FIG. 2. Scanning electron micrograph of the gate of a SBFET that has a 50 nm wide metal bar inside a gate gap of 50 nm.

amplifier. The reason is that the source-drain bias we used in all measurements is much greater than the ambient temperature; the bias heated the sample. The measuring time with the lockin amplifier is much longer than that with HP4145; therefore, the heating effect is much more severe.

We found that the peak-to-valley ratio of the oscillation will decrease as the source-drain bias becomes larger or the temperature becomes higher. When the source and drain bias is greater than 3 mV or the temperature is higher than 4.2 K, the periodic oscillations almost disappear.

Furthermore, we found that regardless of thermal cyclings, photon excitations, and direction of the source-drain current, the periodic oscillations were reproducible and the oscillation period remained constant. We thermally cycled the 50 nm gate gap SBFET seven times and the 100 nm gate gap SBFET two times from 0.5 to 300 K, and found that the oscillation period did not change. We illuminated the devices at 0.5 K using a light-emitting diode, and found that the only change was a shift of the entire  $I$ - $V$  curve toward the negative gate voltage by a few tenths of a volt; there was no change in the oscillation period. Finally, we exchanged the source and the drain and found that the oscillation amplitude varied slightly, but

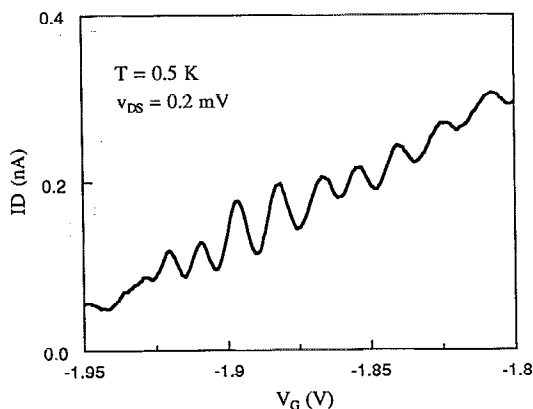


FIG. 3. The drain current vs the gate voltage before the onset of the first  $2e^2/h$  conductance plateau for a SBFET with a 50 nm gate gap. In addition to the ac source-drain bias, 1 mV dc bias were applied between the source and the drain.

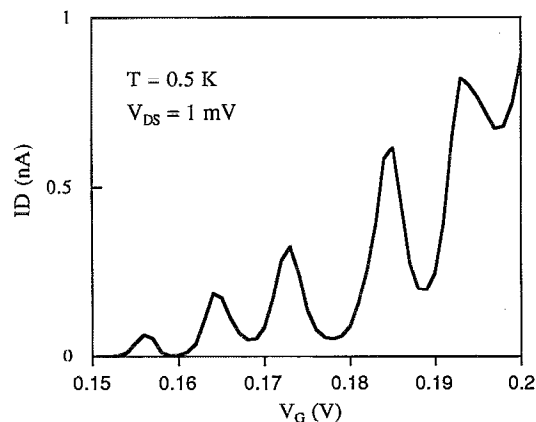


FIG. 4. The drain current vs the gate voltage of a SBFET of 100 nm gate gap, before the onset of the first  $2e^2/h$  conductance plateau. This is a direct  $I$ - $V$  measurement without a lockin amplifier.

again there was no change in the oscillation period. These observations indicate the oscillations are not due to impurities.

To find the physical origin of the conductance oscillations, we first used experimental data to investigate the gate voltage that is needed to place a single electron into one of the two 1D channels. The number of electrons placed in a 1D channel at the 1D-to-2D transition point can be determined from the drain current versus the gate voltage curve and from the conductance and the channel width at the transition point.<sup>6</sup> The channel width at the transition point is approximately the gate gap defined by lithography.<sup>7</sup> Dividing the gate-voltage difference between the threshold and the transition point by the number of electrons at the transition point gives the gate voltage needed to put a single electron into the 1D channel. Thus, we found that the gate voltage needed for placing a single electron into one 1D channel is about 14.6 mV for the SBFET with the 50 nm gate gap and 9.7 mV for the 100 nm gate gap. This agrees well with the experimentally observed current oscillation periods, 15 and 9 mV, indicating that the oscillation originates from the Coulomb blockade of a single electron. We should emphasize that the determination of the gate voltage needed for a single electron charging is completely based on experimental data and that no fitting parameter is involved.

Second, we found that each oscillation peak fits well with the derivative of the Fermi-Dirac distribution function (Fig. 5). This means that the width of the current oscillation peak is due to the thermal broadening of a discrete energy level, since the conductance at finite temperature will be the convolution of the conductance at zero temperature and the derivative of the Fermi-Dirac distribution function.

Third, the fact that the periodic oscillations in the SBFETs were seen only when the conductance was less than  $2e^2/h$  (i.e., before the onset of the first  $2e^2/h$  conductance plateau) is an important signature of the Coulomb blockade of a single electron. Single-electron Coulomb blockade theory requires that, in order to observe the Cou-

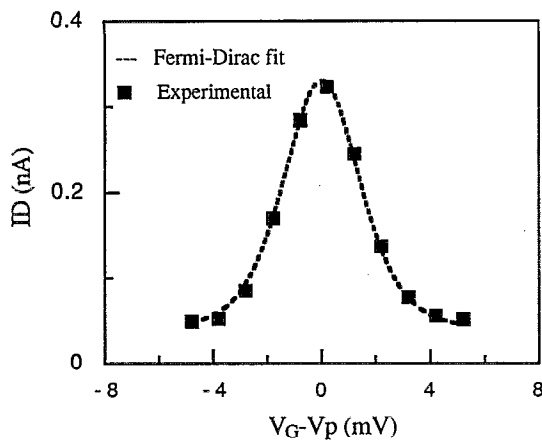


FIG. 5. Fitting a conductance oscillation peak by the derivative of the Fermi-Dirac distribution. The good fit indicates that each oscillation peak comes from the thermal broadening of a discrete energy level.

lomb blockade effects, a single electron has to remain in a Coulomb state long enough to make energy uncertainty less than the spacing between the two adjacent Coulomb levels  $\Delta E$ , where  $\Delta E = e^2/2C$ ,  $e$  is the charge of an electron, and  $C$  is the device capacitance.<sup>8</sup> Namely, the RC constant of the device has to be greater than  $\hbar/\Delta E$ . The result from the above equation requires the conductance of the device be less than  $2e^2/h$ , which is consistent with our experimental observation.

From the above data analysis, we now suggest a model that describes the operation of the single barrier FETs. As depicted in Fig. 6, the electrons put into the 1D channel will occupy the discrete Coulomb energy levels, while the 2DEG outside the 1D channel has a constant Fermi level. As the gate voltage is changed, the Coulomb levels in the 1D channel are shifted either up or down relative to the Fermi level of the 2DEG. When a Coulomb level is aligned with the Fermi level, the current peaks, because if an electron occupying that Coulomb level goes from the source side to the drain side leaving an empty state, another electron from the 2DEG can come and occupy the empty state, leading to the current flow between the source and the drain. On the other hand, the current drops when the Fermi level is between the two Coulomb levels. Since the Coulomb levels below the Fermi level are occupied, the Coulomb repulsion forces the next electron to occupy the Coulomb levels above the Fermi level, which is energetically unfavorable and leads to the blockade of the current between the source and the drain. As the gate voltage moves the Coulomb energy levels in the 1D channel across the Fermi level, the conductance oscillates.

Since the model suggests that electrons go from the source to the drain one by one, there should be a maximum drain current, which is equal to the product of the electron charge and the maximum frequency that electrons travel from the source to the drain. The maximum frequency is equal to the inverse of the transit time that an electron goes across the channel with the Fermi velocity. For a device with a channel length of  $0.5 \mu\text{m}$  and an electron Fermi velocity of  $1 \times 10^7 \text{ cm/s}$ , the maximum drain current is 32

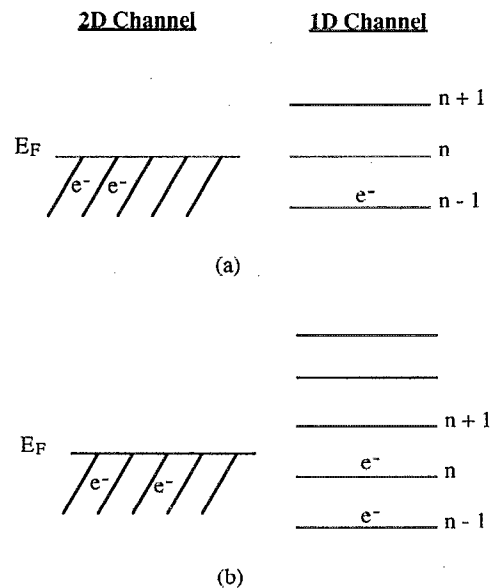


FIG. 6. A model for the operation of the single electron transistor with a single barrier. (a) A Coulomb level in the 1D channel is aligned with the Fermi level of 2DEG, giving a current peak, and (b) the Fermi level of 2DEG is between two Coulomb levels, giving a current valley.

nA. Certainly, the actual current observed experimentally should be less than this maximum, since the electrons were slowed down by the single barrier in the channel. From Figs. 3 and 4, we see that the conductance oscillation peak current is about 1 nA, which does not contradict with the model. Furthermore, we see that the peak current increases as the gate voltage increases toward positive. We believe that one of the reasons for this is that as the gate voltage increases toward positive, the single barrier height becomes smaller and the time that an electron dwells in the channel becomes shorter.

In all previous single electron charging experiments, two or more barriers were used to retain a single electron. In our devices, although there is only a single barrier in the channel, we believe that a single electron can still be retained in the 1D channel at the source side for a period of time. This is because the electric field between the source and drain tilts the energy band, so that the tilted energy band and the single barrier form a triangle potential well.

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