

Engineering sub-50 nm quantum effect devices and single-electron transistors using electron-beam lithography

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(Received 2 July 1992; accepted 31 July 1992)

Fabrication and characteristics of various nanoscale quantum and single-electron devices are described. Using high-resolution electron beam lithography and double layer PMMA resist, we have successfully fabricated a 20 nm split-gate device, a novel 50 nm single barrier single-electron transistor, and a 75 nm triple barrier tunneling device. Effects of beam dose and the number of writing passes on the actual lithography pattern were investigated for various device gate geometries. Pronounced quantum and single-electron effects have been observed in these devices.

I. INTRODUCTION

New devices based on quantum or single-electron effects are opening up a fascinating new field of research thanks to advances in nanofabrication technology. In particular, devices using field-effect induced lateral confinement in combination with vertical confinement in semiconductor heterostructures have attracted much attention because they are very flexible in changing the confinement size and electron concentrations.^{1,2} One of the requirements as well as the challenges in fabricating these field-induced nanodevices is to make the device size as small as possible since generally the smaller the size of the devices, the larger the quantum and single-electron effects will be. In this article, we report the fabrication of various nanoscale quantum effect and single-electron effect devices using a custom-built high-resolution electron beam lithography (EBL) system. These devices include a 20 nm split-gate field-effect transistor (FET), a 50 nm single barrier field-effect transistor (SBFET), and a 75 nm triple barrier field-effect transistor (TBFET). We show that the size of these devices can be well controlled by suitable choice of e-beam exposure dose. Pronounced quantum and single-electron effects have been observed in these devices.

Split-gate FETs have been widely used to study ballistic electron transport in a one-dimensional (1D) wire over the past several years.³ The 1D wire is created at the AlGaAs/GaAs interface when the electrons beneath the negatively biased split gate are depleted. A SBFET has a structure similar to a split-gate FET except that an extra metal bar is placed inside the gap of the split gate. The metal bar that induces a potential barrier inside the 1D wire, together with the source-drain bias, can trap electrons in a triangular potential well. Due to coulomb repulsion, the trapped electrons will block the source-drain current.⁴ A TBFET consists of three metal bars inside the gate gap. In such a device, both single electron charging effects and resonant tunneling exist.

II. FABRICATION

All of the devices were fabricated on an AlGaAs/GaAs heterostructure grown by molecular-beam epitaxy (MBE), which has a 500 nm thick undoped GaAs layer on top of a

semi-insulating GaAs substrate, a 10 nm undoped Al_{0.3}Ga_{0.7}As spacer layer, a 40 nm Al_{0.3}Ga_{0.7}As layer with Si doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$, and 15 nm GaAs cap layer with Si doping concentration of $1.4 \times 10^{18} \text{ cm}^{-3}$. The two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs interface has a Hall mobility of $12 \text{ m}^2/\text{V s}$ and a carrier concentration of $8.9 \times 10^{11} \text{ cm}^{-2}$ at 77 K in the dark.

The fabrication process consists of four steps: mesa isolation using wet etch, formation of source and drain ohmic contacts, nanoscale gate fabrication, and final metallization for bonding pads. The critical part of the fabrication is the nanogate definition which is performed using EBL followed by a lift-off process.⁵ A double layer resist scheme consisting of a 2% 950 K PMMA layer on top of a 3% 100 K PMMA layer was used. Each layer was spun at 7000 rpm for 1 min and baked at 168 °C for at least 10 h. The total PMMA thickness is about 110 nm measured using an ellipsometer. The main reason for using bilayer resist is to reduce the effect of electron backscattering and to produce a desirable undercut profile in the resist for easy lift-off. However, the undercut in bilayer resist may also have some adverse effects when the gap of a split gate becomes very narrow as will be discussed later.

The EBL system consists of a modified scanning electron microscope, JEOL-840A, and a custom pattern generator designed and built in-house.⁵ The electron accelerating voltage used for EBL is 35 keV, and the beam diameter is about 3 nm. After e-beam exposure, the PMMA was developed in 3:7 cellosolve:methanol followed by a methanol rinse. The gate electrodes were formed by lift-off of e-beam evaporated Ti/Au (10 nm/20 nm).

A. Split-gate FET with 20 nm gate gap

The gate of the split-gate FET was defined using e-beam exposure of two long rectangles separated by a small gap in PMMA. After development, the width of a narrow PMMA line between two developed rectangles determines the gap width of the split gates. Due to the proximity effect and the finite resist contrast, the actual gate gap width, W_g , achieved after lift-off will be different from the nominal gate gap width W_n , defined by the e-beam pattern generator. In order to reliably obtain desired nanoscale gate gap

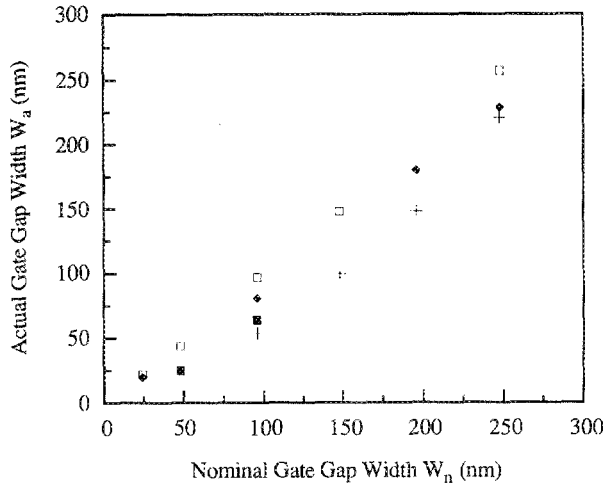


FIG. 1. Actual gap width W_a vs nominal gap width W_n for three different doses and two gate lengths. \square $D=0.53$ mC/cm², $L=0.5$ μ m; \blacklozenge $D=0.70$ mC/cm², $L=0.5$ μ m; \blacksquare $D=0.88$ mC/cm², $L=0.5$ μ m; $+$ $D=0.70$ mC/cm², $L=1$ μ m.

for split-gate FETs, we have investigated (1) how to control the actual gate gap width, and (2) how to achieve the smallest gate gap.

First, we investigate the relationship between the actual gate gap width and the nominal gate gap width for a fixed dose. Three different doses (0.53, 0.70, and 0.88 mC/cm²) were used. The relationship is plotted in Fig. 1. For a dose of 0.53 mC/cm² and a gate length of 0.5 μ m, the data can be fitted into $W_a=1.05 W_n-5.0$ nm, indicating the actual gate gap is essentially the same as the nominal one. This implies that the proximity effect is very small. Figure 2 shows scanning electron micrograph (SEM) of a 20 nm split gate with $L=0.5$ μ m written at a dose of 0.70 mC/cm². The sharp corners of the metal gates indicate, again, small proximity effect. One explanation for the small proximity effect is that the gate length is much smaller than the proximity length, which is believed to be over several microns. Therefore writing the split gate with a 0.5 μ m gate length is more like writing a line with a break in

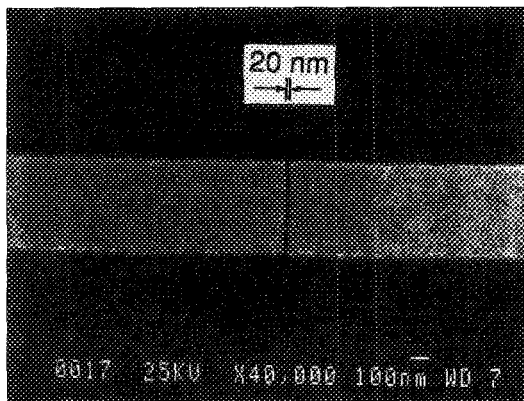


FIG. 2. SEM picture of a split gate with a 20 nm wide and 0.5 μ m long gate gap.

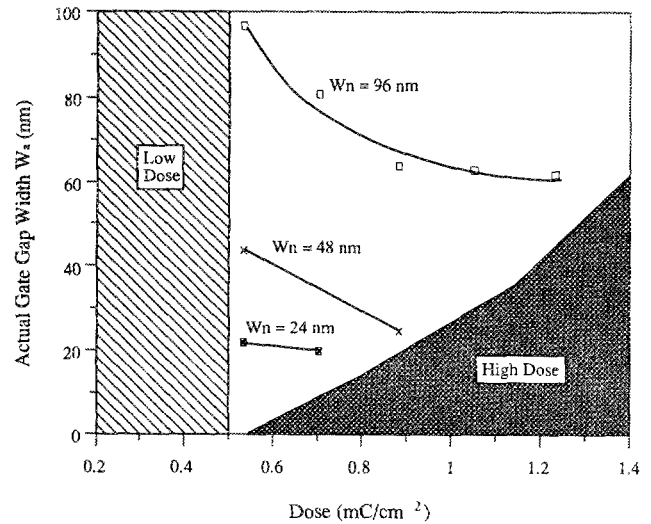


FIG. 3. Actual gap width vs dose for three different nominal gap widths. \square $W_n=96$ nm; \times $W_n=48$ nm; \blacksquare $W_n=24$ nm. Three regions are shown corresponding to low dose, usable dose, and high dose.

the middle. On the other hand, as the gate length becomes comparable to the proximity length, the proximity effect becomes severe. In fact we are unable to achieve 20 nm gate gap when the gate length is 1 μ m or longer. For comparison, in Fig. 1, we have also plotted the data for a gate length of 1 μ m written at a dose of 0.70 mC/cm². The linear fitting gives $W_a=1.09 W_n-56.7$ nm. The proximity effect is clearly much larger than that for a gate length of 0.5 μ m written at the same dose (the linear fitting of the latter is $W_a=0.94 W_n-5.2$ nm). Fortunately, in most ballistic transport devices, the gate length should not exceed 0.6 μ m because random potential will severely degrade the ballistic behavior.⁶ The most commonly used gate length is 0.3 μ m, for which the proximity effect is expected to be even smaller.

In Fig. 3, we plot, for a given nominal writing gap width, how the dose affects the actual gate gap size. Certainly, if the dose is too high, the PMMA line between the two exposed rectangles disappear and the lift-off becomes impossible. On the other hand, if the exposure dose is too low, residual underdeveloped resists are left in the exposed area and the gate metal becomes granular after lift-off. Figure 3 shows the region where a good lift-off is possible and the regions where the doses are either too low or too high. The dose range for a successful lift-off becomes narrower as the nominal gate gap becomes smaller. This means, to obtain small gate gap width, the choice of dose becomes very critical. The boundary of the neighboring regions drawn in Fig. 3 is somewhat arbitrary due to sparse data.

In the double layer resist scheme, since the 100 K PMMA is more sensitive to the exposure than 950 K PMMA, there will be an undercut profile after development. For a very narrow gate gap, the 100 K PMMA in the gate gap region may be developed completely, leaving an air bridge of 950 K PMMA. Such a PMMA air bridge is

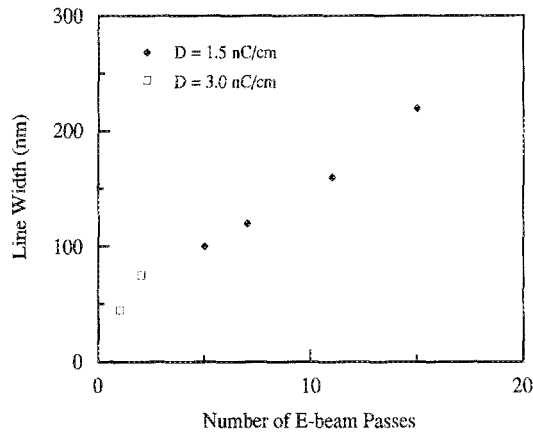


FIG. 4. Linewidth vs the number of e-beam passes for two different doses.

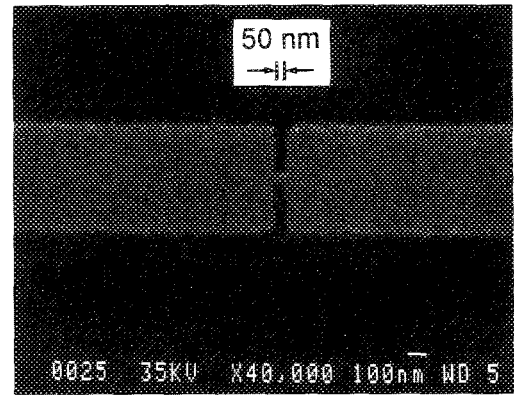
mechanically unstable. In fact, we have found twisting of the PMMA air bridge in some devices due to processing.

B. 50 nm SBFET and 75 nm TBFET

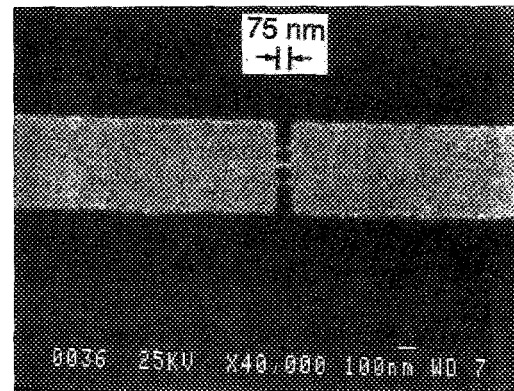
To fabricate SBFETs or TBFETs, in addition to the e-beam exposure of two long rectangles separated by a narrow gap, one or three short lines connecting the two rectangles are exposed at the same time by a single pass or multiple passes of the e-beam. The exposed short line is transferred into a metal bar after development, metallization, and lift-off. The width of the potential barrier induced in the FET's channel by the metal bar depends not only on the applied gate bias but also on the width of the metal bar. The bar width and thus the potential barrier width can be controlled by varying the dose of a single pass e-beam or using multiple passes.

Figure 4 gives the linewidth versus the number of e-beam passes for two different line doses. The linewidth varies linearly with the number of e-beam passes. With a higher dose, the linewidth increases much faster with the number of e-beam passes. Although the line doses in Fig. 4 are obtained from writing a single isolated line of 34 μm long, the same doses can be used for writing short lines in SBFET and TBFET. This is because (1) the proximity effect from the split-gate pattern is quite small; and (2) for the exposure dose of 1.5 nC/cm, the linewidth is dominated by forward scattering⁷ and therefore is insensitive to the line length.

Figures 5(a) and 5(b) are the SEM pictures of a 50 nm SBFET and a 75 nm TBFET, respectively. The split-gate patterns were exposed with an area dose of 0.6 mC/cm², and the short lines were all exposed by a single e-beam pass with a line dose of 1.5 nC/cm. Notice that in Fig. 4, for line dose of 1.5 nC/cm, the extrapolated linewidth from a single e-beam pass is 50 nm, which is close to the linewidth of the short lines in Figs. 5(a) and 5(b). This supports the previous argument that the linewidth is, indeed, insensitive to the exposed line length.



(a)



(b)

FIG. 5. SEM picture of (a) a 50 nm SBFET (b) a 75 nm triple barrier FET. Both of the gate lengths are 0.5 μm .

III. DEVICE CHARACTERISTICS

We have demonstrated that a split gate with a gap width as narrow as 20 nm can be fabricated. To observe 1D subbands in such a narrow gate gap device, however, we need a heterostructure with a small gate-to-channel distance and a large 2DEG concentration. The heterostructure we use has a gate-to-channel distance of 65 nm. Therefore, a 20 nm gate gap can be easily pinched off by the fringing field from the gate bias and no 1D subband can exist.

In Fig. 6, we show the drain current versus gate voltage curve for a split-gate device with a 100 nm gate gap and a 0.5 μm gate length. The measurement was taken at 4.2 K with 1 mV drain bias. No series resistance correction has been made. The drain current shows plateaulike structures indicating ballistic transport through the 1D wire.³ As gate voltage increases, the width of the 1D wire increases, and more 1D subbands are occupied. Each 1D subband contributes a constant conductance of $2e^2/h$ and thus leads to the quantization of drain current. The quantization in Fig. 6 is not perfect but still quite impressive considering the high temperature, the large drain bias, the long gate length, and the nontapered channel.⁸

Figure 7 gives the measured drain current of the SBFET shown in Fig. 5(a). The measurement was done at 0.5 K in a sorption pumped He³ system. Strong conductance oscil-

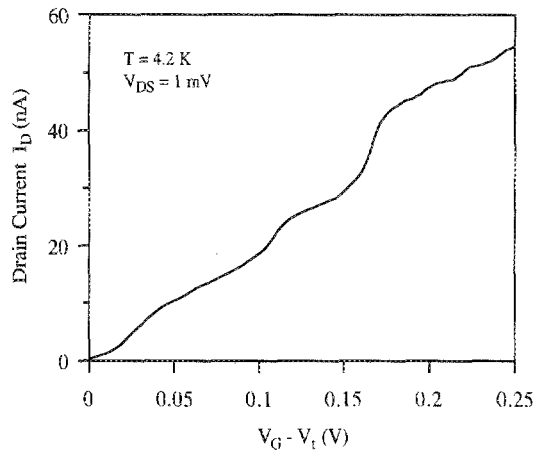


FIG. 6. Drain current vs gate voltage for a split-gate device with a gate gap width of 100 nm and a gate length of 0.5 μm . Measured at 4.2 K with 1 mV drain bias.

lations have been observed. The oscillations are reproducible under thermal cyclings between 0.5 K and room temperature. The average peak-to-peak separation in gate voltage is about 15 mV, which agrees with the estimated gate voltage needed for adding or removing a single electron from the 1D wire.⁴ The result is thus interpreted as being due to the Coulomb blockade of a single electron. Similar oscillations have been reported previously in the double barrier FET.² There, the double barriers were used to retain a single electron. In our device, although there is only a single barrier in the channel, we believe that a single electron can still be retained in the 1D channel at the source side. This is because the electric field between the source and drain tilts the energy band, so that the tilted energy band and the single barrier form a triangular po-

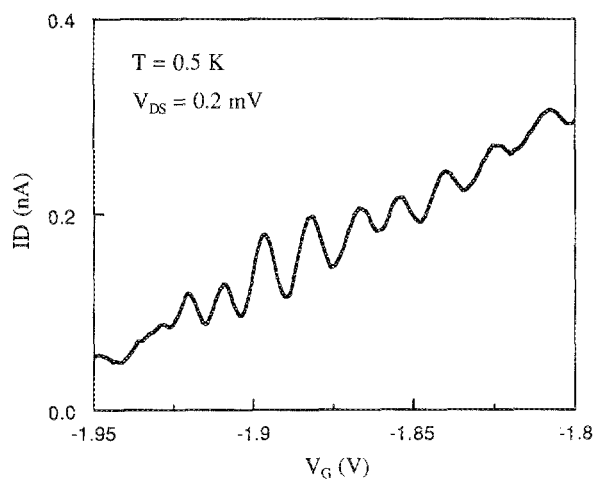


FIG. 7. Drain current vs gate voltage for the SBFET shown in Fig. 5(a).

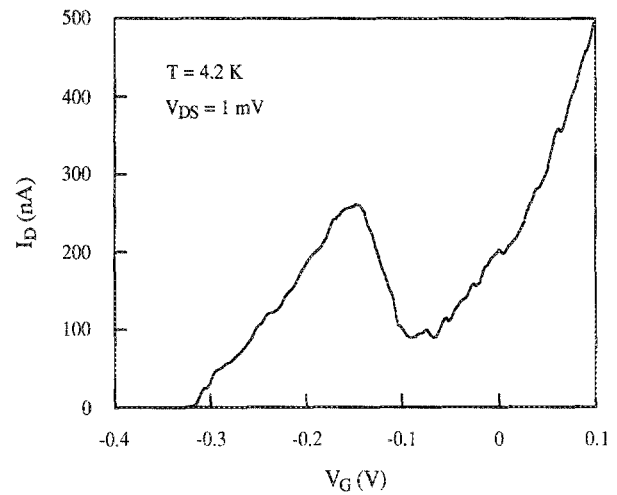


FIG. 8. Drain current vs gate voltage for the TBFET shown in Fig. 5(b).

tential well, which retains electrons in a way similar to a potential well created by double barriers.

Finally, in the TBFET shown in Fig. 5(b) and in several similar devices, a giant resonance has been observed at 4.2 K under photon excitation (Fig. 8). The origin is still unknown. Further investigation is currently underway.

IV. CONCLUSION

We have successively fabricated various nanoscale quantum devices on AlGaAs/GaAs heterostructure using high-resolution EBL and double layer PMMA resist. Effects of beam dose and the number of writing passes on the actual lithography pattern were investigated for various device gate geometries. We have observed interesting electron transport in these nanoscale devices caused by quantum and single-electron effects.

ACKNOWLEDGMENTS

The authors would like to thank Paul Fischer for his technical assistance and useful discussions. This work is partially supported by the Packard Foundation through a Packard Fellowship Award, the Office of Naval Research under Contract No. N00014-92-J-1306, and the Army Research Office.

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