

# Planar double gate quantum wire transistor

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A planar double gate quantum wire transistor (QWT) is proposed and demonstrated. The transistor uses a narrow wire gate placed inside the gap of a split gate to create a single one-dimensional (1D) quantum wire (QW). We demonstrate theoretically and experimentally that the wire gate can create a QW potential with a better confinement and therefore larger subband separations than that in other split-gate QWTs, and that the split gate can adjust the number of electrons inside the QW while keeping the 1D QW potential almost unchanged. Furthermore, we found that, in the double gate QWT, a 1D electron channel can spatially overlap with a 2D electron channel without significant mixing.

In recent years, a split-gate scheme on top of a semiconductor heterostructure has been widely used to achieve a quasi-one-dimensional (1D) quantum wire (QW).<sup>1-3</sup> The split gate squeezes two-dimensional (2D) electrons at the heterojunction interface into a narrow region beneath the gap of the split gate to form a 1D wire. One of the shortcomings of such conventional split-gate quantum wire transistors (QWT) is that the width and depth of the 1D wire as well as the number of electrons inside the wire are simultaneously changed by the same gate voltage. This shortcoming makes it difficult to create a narrow 1D wire while populating sufficient electrons inside.

To achieve better control and better confinement of a 1D QW, two types of stacked double gate QWTs were proposed previously. Both of them use a split gate to define the width of a 1D QW in the same way as that in a conventional split-gate QWT, except one of them has a planar gate on top of the split gate<sup>4</sup> and the other has a planar gate on the back side of the wafer.<sup>5</sup> The planar gate can offer a new degree of freedom in adjusting the electron population, but does not improve the 1D confinement substantially.

Here, we propose a new transistor—a planar double gate QWT—where, as shown in Fig. 1, a narrow wire gate is placed inside the gap of a split gate. This QWT is very different from the previously reported QWTs. It uses a positively biased narrow wire gate to create a 1D QW potential and uses a negatively biased split gate to adjust the Fermi level (therefore the number of electrons) inside the 1D QW while keeping the shape of 1D QW potential almost unchanged. In this letter, we present a theoretical and experimental study of the QWT. We show that in addition to a stronger confinement potential and separate control of the Fermi level, the QWT can make a 1D channel spatially overlap with a 2D electron channel without significant mixing.

The planar double gate QWT is fabricated on top of a molecular beam epitaxy (MBE)-grown  $\delta$ -doped AlGaAs/GaAs heterostructure consisting of a 0.5  $\mu\text{m}$  GaAs buffer layer on a semi-insulating GaAs substrate, a 20 nm undoped Al<sub>0.3</sub>Ga<sub>0.7</sub>As spacer layer, a  $\delta$ -doped layer with a Si concentration of  $7 \times 10^{12} \text{ cm}^{-2}$ , a 15 nm undoped Al<sub>0.3</sub>Ga<sub>0.7</sub>As layer, and a 5 nm *n*-GaAs cap layer with a Si concentration of  $3 \times 10^{18} \text{ cm}^{-3}$ . At 77 K in the dark, the

two-dimensional electron gas (2DEG) has a concentration of  $4 \times 10^{11} \text{ cm}^{-2}$  and a Hall mobility of  $90\,000 \text{ cm}^2/\text{V s}$ . The distance between the gate metal and the 2DEG is 40 nm, allowing the gate to modulate the channel more effectively.<sup>6</sup> Figure 1(b) shows the scanning electron micrograph of the device, which consists of a 30 nm wide wire gate in the middle of a 0.3  $\mu\text{m}$  gap of a split gate. The QWT has four ohmic contact pads (two for the sources and two for the drains). The gate patterns are defined using high-resolution electron beam lithography followed by a liftoff of Ti/Au.<sup>7</sup>

There are two biasing modes for operating the device. In mode I, the positive bias on the wire gate is fixed while the bias on the split gate is scanned. In mode II, the bias on the wire gate is scanned while the bias on the split gate is

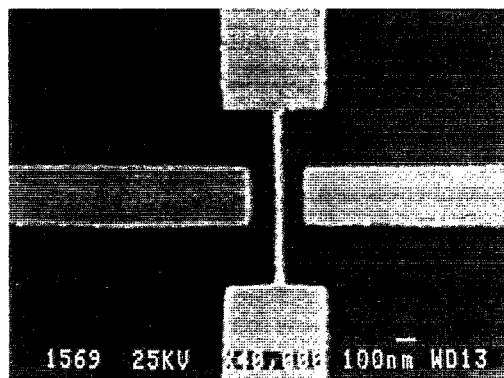
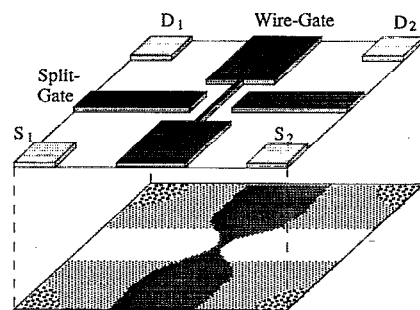


FIG. 1. (a) Schematics and (b) scanning electron micrograph of a planar double gate quantum wire transistor that has a wire gate placed inside the gap of a split gate. The wire gate is 30 nm wide. The split gate has a length of 0.3  $\mu\text{m}$  and a gap width of 0.3  $\mu\text{m}$ .

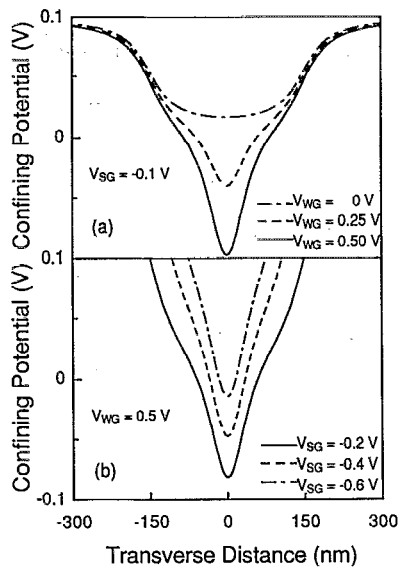


FIG. 2. Computer simulation of the potential profile in the double gate quantum wire transistor. (a) Different wire gate  $V_{WG}$  with the split-gate voltage  $V_{SG}$  fixed at  $-0.1$  V, and (b) different  $V_{SG}$  with  $V_{WG}$  fixed at  $0.5$  V.

fixed. In our device operation, the wire gate is always positively biased, hence only a single QW is created. If the wire gate is biased negatively, however, the electrons will be depleted under the wire gate, creating two coupled QWs, which have been investigated previously.<sup>8</sup>

Computer simulation of the potential profiles for operation modes I and II are shown in Fig. 2. The simulation is based on a simple non-self-consistent calculation discussed by Davies,<sup>9</sup> which takes into account only the electrostatic contribution from the gate bias. The approximation holds near the threshold when no electron or only a few electrons are induced under the gate. This model, though oversimplified, provides a qualitatively correct picture of the actual potential profile.

Figure 2(a) shows that as the wire-gate voltage,  $V_{WG}$ , is increased, a 1D QW is gradually formed in the middle of a much wider potential well that was created by the split gate. Figure 2(b) shows that as the split gate is scanned, the 1D QW potential is moved up or down relative to the Fermi level, while keeping the shape of 1D QW almost unchanged. This result is significant because it implies that scanning the voltage on the split gate,  $V_{SG}$ , modulates only the carrier concentration in the 1D QW but not the energy level spacing between the 1D subbands. Therefore, the knees of each  $2e^2/h$  plateau in the  $I_D$  vs  $V_{SG}$  characteristics directly map the edges of 1D subbands in the QW. This feature cannot be achieved in other types of QWTs. The application of such mapping in studying energy spacing between the subbands in a 1D QW will be discussed in a separate article.<sup>10</sup> In addition, Fig. 2(b) shows that the width of the 1D QW can be very narrow and its sidewall can be very steep, partly because the 1D QW potential in the QWT is controlled by a well-defined positive gate bias instead of the surface potential of GaAs at the top surface of the heterostructure.

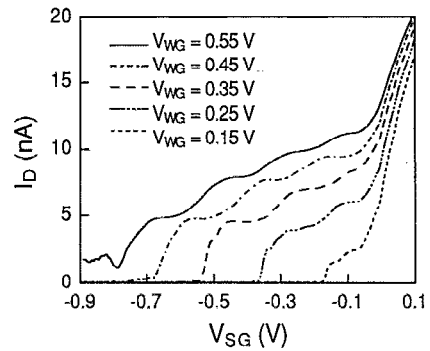


FIG. 3. The drain current  $I_D$  vs the split-gate voltage  $V_{SG}$  for different fixed wire-gate bias  $V_{WG}$  at 5 K with a source-drain voltage of  $70 \mu\text{V}$ . The device operates in biasing mode I. The number of 1D plateaus increases with  $V_{WG}$ .

Now, we present the experimental study of this QWT. Figure 3 shows the  $I_D$  vs  $V_{SG}$  of the planar double gate QWT for different fixed  $V_{WG}$  (i.e., operating in mode I) measured at 5 K with a  $70 \mu\text{V}$  drain-source bias. At  $V_{WG} = 0.15$  V, a 1D QW just forms and in it only one subband exists, therefore one  $2e^2/h$  plateau appeared in the current-voltage ( $I$ - $V$ ) characteristics. As  $V_{WG}$  increases from 0.15 to 0.55 V, the 1D QW becomes deeper and more 1D subbands are formed in the 1D QW, giving more  $2e^2/h$  plateaus in the  $I$ - $V$  characteristics. There are two subbands at  $V_{WG} = 0.25$  V, three at  $V_{WG} = 0.35$  V, and four at  $V_{WG} = 0.55$  V. It should be pointed out that the conductance of each plateau is not an exact integer number of  $2e^2/h$ . However, data fitting showed that by subtracting the contribution from a constant series resistance, the conductance of each plateau will become an exact integer number of  $2e^2/h$ . This means that the discrepancy is mainly due to the series resistance instead of electron backscattering in the channel.

Figure 3 also shows that when  $V_{SG}$  is larger than  $-0.1$  V, electrons start to populate under the split gate. These electrons are 2D, since the split gate has a gate width of  $10 \mu\text{m}$  and the gate length of  $0.3 \mu\text{m}$ . This 1D to 2D transition point always occurs at the same  $V_{SG}$  regardless of  $V_{WG}$ , because the Fermi level at 2DEG reservoir remains constant.

Further study, which will be reported elsewhere,<sup>11</sup> showed that because of the stronger confinement, the 1D ballistic transport persists to a temperature up to 26 K or a bias of 12 mV.

Figure 4 shows the  $I_D$  vs  $V_{WG}$  for different  $V_{SG}$ , (i.e., operating in mode II). The measurement is taken at 0.5 K. Again it shows well-defined  $2e^2/h$  plateaus due to 1D ballistic transport. Figure 4(a) shows that as the split-gate bias becomes more negative, it become increasingly difficult to observe  $2e^2/h$  plateaus with the wire gate. This is because the more negative the split-gate bias is, the further the Fermi level is below the bottom of the wide potential well that was formed by the split gate, requiring a deeper 1D well to create a 1D subband that is below the Fermi level.

Very interestingly, Fig. 4(b) shows that for a  $V_{SG}$  higher than  $-0.1$  V, the 2DEG starts to populate under

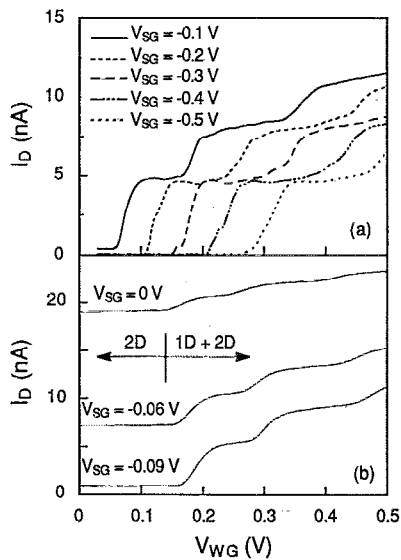


FIG. 4. The drain current  $I_D$  vs the wire-gate voltage  $V_{WG}$  for different fixed split-gate bias  $V_{SG}$  with a source-drain voltage of  $70 \mu\text{V}$  at  $0.5 \text{ K}$ . The device operates in biasing mode II. (a) Only 1D channels but no 2D channels, (b) 1D and 2D channels spatially overlap.

the split gate (the threshold for the 2D channel is a little less than  $-0.1 \text{ V}$  as shown in Fig. 3), but the  $2e^2/h$  plateaus are still distinguishable in the  $I$ - $V$  characteristics. In this case, the 2D channel spatially overlaps with the 1D channel—a situation unexplored yet. Figure 4(b) shows that whenever a new 1D subband is induced below the 2DEG sea, a new  $2e^2/h$  conductance peak appears, even though the 1D and 2D channels overlap spatially. The total current in Fig. 4(b) is simply the sum of the individual contributions from the 1D and 2D channels. This indicates that there is no significant mixing between 1D and 2D channels. The  $2e^2/h$  plateaus were still distinct even when the conductance of 2D channel became as large as  $8e^2/h$ . This means that the separation between the 1D subbands and 2D subband is quite large. Clearly, this is an interesting model system which could give rise to new phenomena. Details of the study will be reported elsewhere.

As a few additional experimental details, we found that in our devices the  $I$ - $V$  characteristics were essentially identical for the four different source-drain pair configurations:  $S_1D_1$ ,  $S_1D_2$ ,  $S_2D_1$ , and  $S_2D_2$  [see Fig. 1(a)]; and for the configuration where  $S_1S_2$  were connected together as the source and the  $D_1D_2$  together as the drain. This verifies

that only a single 1D wire is created. In addition, we found that a large wire gate current could cause a negative dc shift in drain current and large noise in the  $I$ - $V$  characteristics. But these problems are readily eliminated by using a lock-in amplifier. The more fundamental problem for a large gate current is the heating of the channel electrons. Although depending on the quality of the Schottky barrier, the leakage current in our device is typically less than  $10 \text{ pA}$  at  $V_{WG} < 0.2 \text{ V}$  but becomes as large as  $500 \text{ nA}$  at  $0.6 \text{ V}$ . In fact, we found that for a wire-gate biased above  $0.65 \text{ V}$ , the  $2e^2/h$  plateaus disappear quickly.

In conclusion, we proposed and demonstrated a planar double gate quantum wire transistor. We showed theoretically and experimentally that the wire gate can create a QW potential with a better confinement and therefore larger subband separations than that in other split-gate QWTs, and that the split gate can adjust the number of electrons inside the QW while keeping the 1D QW almost unchanged. We believe that the additional degree of freedom in controlling the planar double gate quantum wire transistor would make it a more flexible and therefore more powerful tool in studying low dimensional quantum transport. Furthermore, we found that, in our QWT, a 1D electron channel can spatially overlap with a 2D electron channel without significant mixing.

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