

EFFECTS OF BIAS AND TEMPERATURE ON ONE-DIMENSIONAL BALLISTIC TRANSPORT IN A PLANAR DOUBLE-GATE QUANTUM WIRE TRANSISTOR

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The combined effects of bias and temperature on one-dimensional ballistic transport in a planar double-gate quantum wire transistor are investigated. A simple formula that quantitatively describes both effects is derived and found to fit experiments well. Other energy broadening factors are found to be significant. Furthermore, due to the strong confinement potential in the device, the current quantization is still observable at a temperature up to 26 K or with a drain bias up to 12 mV.

1. Introduction

Recently, we proposed and demonstrated a planar double-gate quantum wire (QW) transistor,¹ which consists of a wire-gate inside the gap of a split-gate. This gate structure creates a single one-dimensional (1D) QW with a strong confinement potential and allows us to separately adjust the width of the 1D wire and the electron concentration inside the wire. In this paper, we investigate the effects of drain bias and temperature on 1D ballistic transport in the new QW transistor. The individual effect of bias at negligible temperature and effect of temperature at small bias were studied previously.^{2,3} However, to date, no quantitative experimental study has been reported on the combined effects of bias and temperature. For this reason, we study the 1D transport in the regime of both finite bias and temperature, and compare the experimental results with the theory. Because of the good confinement achieved in the new QW structure, a much wider range of bias and temperature can be studied. In addition, we will discuss the effects of other energy broadening factors, such as the gate-heating and the shape of the constriction potential.

2. Theory

The effects of bias and temperature on 1D ballistic transport in a quantum wire transistor can be described using the maximum transconductance: $g_{\max} = (dI_D/dV_G)_{\max}$, where I_D is the drain current and V_G is the

gate voltage. This maximum transconductance, which can be directly obtained experimentally, measures the sharpness of a transition in the drain current from one $2e^2/h$ plateau to the next as the gate voltage is scanned. For ideal 1D transport, the transition in the current-voltage (I_D - V_G) characteristics is a step function, the transconductance is a δ -function, and g_{\max} is infinite. However, in a real 1D quantum wire transistor, the transition is gradual over a range of V_G , the transconductance is broadened into a peak of a certain width, and g_{\max} becomes finite. This is due to heating from ambient temperature and drain bias⁴ as well as energy broadening from scattering, mode mismatching,⁵ and shape of the confinement potential.⁶

Theoretically, at a finite temperature T , and a finite drain bias V_D , the drain current I_D can be written as⁴

$$I_D(E_F, V_D, T) = I_{D0}(E_F) \otimes \frac{f_0(E_F) - f_0(E_F + eV_D)}{eV_D} \quad (1)$$

where I_{D0} is the drain current at zero temperature with an infinitesimal drain bias, E_F is the Fermi energy, \otimes means convolution with respect to E_F , e is the magnitude of an electron charge, and f_0 is the Fermi-Dirac distribution function. Using Landauer's formula⁷ and assuming a unit transmission matrix, I_{D0} becomes a sum of step functions. By setting $d^2I_D/dE_F^2 = 0$ at the maximum of dI_D/dE_F , we have

$$\left(\frac{dI_D}{dE_F}\right)_{\max} = \frac{2e}{h} \tanh\left(\frac{eV_D}{4kT}\right) \quad (2)$$

If $eV_D \gg 4kT$, Eq. (2) reduces to

$$\left(\frac{dI_D}{dE_F}\right)_{\max} = \frac{2e}{h} \quad (2a)$$

If $eV_D \ll 4kT$, Eq. (2) reduces to

$$\left(\frac{dI_D}{dE_F}\right)_{\max} = \frac{2e}{h} \left(\frac{eV_D}{4kT}\right) \quad (2b)$$

These two limits agree with that discussed by Bagwell *et al.*⁴

Experimentally, in a field-effect-transistor, the change of Fermi level is controlled by a gate voltage V_G and is, for a first order approximation, proportional to the change of V_G : $\delta E_F = \alpha e \delta V_G$, where α is the gate modulation efficiency. Using this relation and Eq. (2), we have

$$g_{\max} = \alpha \frac{2e^2}{h} \tanh\left(\frac{eV_D}{4kT}\right) \quad (3)$$

3. Experiment and Results

The transistor we use to examine Eq. (3) consists of a 30 nm wide wire-gate in the middle of a 0.3 μm wide split-gate gap (Fig. 1). The wire-gate is positively biased at 0.6 V to create a narrow quantum wire at the interface of the heterojunction beneath the gate, and the split-gate voltage V_G

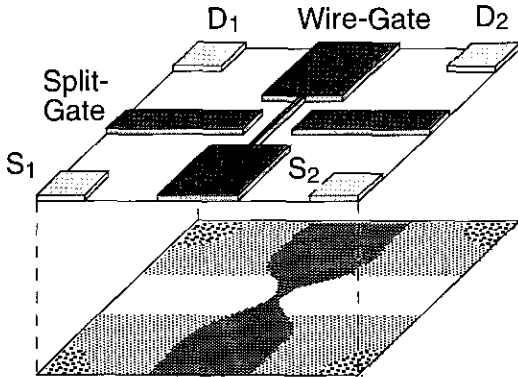


Fig. 1 Schematic diagram of a planar double-gate quantum wire transistor that has a 30 nm wide wire-gate inside a 0.3 μm wide split-gate gap. The length of the split-gate gap is 0.3 μm .

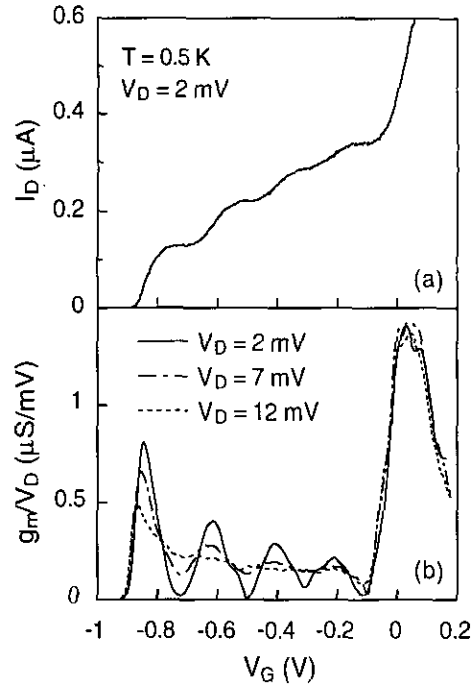


Fig. 2 (a) Drain conductance vs. split-gate voltage for $V_D = 2$ mV; and (b) normalized transconductance vs. split-gate voltage for three different drain biases. The measurements were taken at $T = 0.5$ K.

is scanned to change the Fermi level and hence the electron concentration inside the wire. It should be pointed out that although the gate structure of this device is similar to that of the coupled quantum wire studied by del Alamo *et al.*⁸, the operation principles are different. In our device, the wire-gate is positively biased so that only one wire is induced; while in theirs, it is negatively biased and hence two coupled wires are created.

The gates were fabricated on top of a δ -doped AlGaAs/GaAs heterostructure. The distance between the gate metal and the two-dimensional electron gas (2DEG) is 40 nm. At 4.2 K in the dark, the 2DEG has a mobility of 26 $\text{m}^2/\text{V}\cdot\text{s}$ and a mean free path above 2 μm . The details of the device structure have been discussed in Ref. 1.

Figure 2(a) shows a typical I_D - V_G curve from a dc measurement at 0.5 K with a drain bias of 2 mV. Four plateaux in the 1D transport region are clearly seen. After subtraction of series resistance, the plateaux are found to be quantized at multiples of $2e^2/h$. The highest plateau has a quantization error of 10%. For the lower current plateau, the quantization accuracy is better; in fact, for the first plateau, the quantization error is smaller than 1%. This indicates the impurity scattering is negligible in the first subband, therefore, we will mainly focus on the transition of the first current plateau.

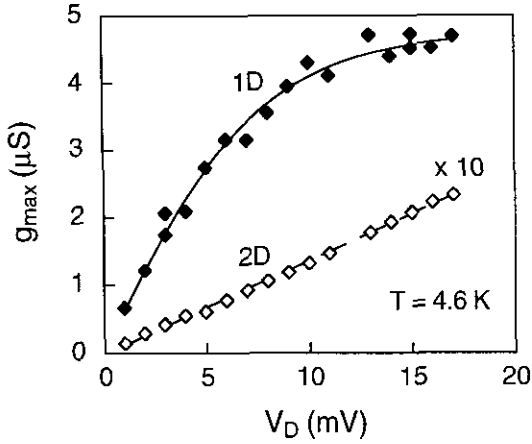


Fig. 3 The first 1D peak transconductance vs. the drain bias at $T = 4.6$ K (solid diamonds). The solid line is the curve fitting using Eq. (3). For comparison, the 2D peak transconductance is also plotted (open diamonds) with a linear fitting (dashed line).

3.1 Effect of Drain Bias

To see the drain bias effect, in Fig. 2(b), we plot the normalized transconductance, g_m/V_D , as a function of the split-gate voltage V_G at three different drain biases. Each of the four peaks in the 1D region corresponds to the transition from one $2e^2/h$ plateau to the next. The peak in the 2D region is due to the saturation of drain current at high gate voltage. As expected, when V_D increases from 2 mV to 12 mV, the heights of the four 1D peaks decreases and their widths are broadened. But the peak in the 2D region remains the same.

To compare with Eq. (3), we plot the height of the first transconductance peak, g_{max} , against the drain bias (Fig. 3). The measurement was taken at 4.6 K. The experimental data can be well fitted by Eq. (3), if $\alpha = 6.2\%$ and $T = 22.5$ K. The value of α is reasonable since, as shown later, it gives a 1D subband spacing that agrees well with that from other estimations.

However, the fitting temperature, 22.5 K, is much higher than the ambient temperature, 4.6 K. This implies that there are other factors which increase the effective temperature of electrons. In our transistor, two factors may be important. One is the heating effect from gate leakage current in the positively biased Schottky gate. To verify this, we vary the voltage on the wire-gate and observe the sharpness of the transition for the first current plateau. We found that, as the wire-gate voltage increases, the transition becomes more gradual; in particular, when the wire-gate voltage exceeds 0.65 V, the plateaux disappear quickly. This indicates that the gate-heating plays an important role in energy broadening. The heating effect requires one to

add into Eq. (1) a new convolution of a derivative of the Fermi-Dirac distribution function with an effective temperature, T_g .

The other factor is energy broadening due to the shape of the confinement potential. This broadening, as shown by Glazman *et al.*⁶ can be described by a function similar to a Fermi-Dirac distribution function which essentially arises from the tunneling through an adiabatic constriction. Then another convolution of a derivative of the Fermi-Dirac distribution with an effective temperature, T_s , should be added into Eq. (1).

The convolutions of three derivatives of Fermi-Dirac distribution can be approximated by a single distribution with an effective temperature $T_{eff} = \sqrt{T_a^2 + T_g^2 + T_s^2}$, where T_a denotes the ambient temperature. The approximation would be exact if the distributions were Gaussian. Thus, Eq. (3) should be replaced by

$$g_{max} = \alpha \frac{2e^2}{h} \tanh\left(\frac{eV_D}{4k\sqrt{T_a^2 + T_o^2}}\right) \quad (4)$$

where $T_o = \sqrt{T_g^2 + T_s^2}$ represents broadening factors other than bias and ambient temperature. For $T_{eff} = 22.5$ K and $T_a = 4.6$ K, we get $T_o = 22$ K. This indicates that at 4.6 K, the broadening is dominated by the gate heating and confinement potential shape.

For comparison, the 2D peak transconductance is also plotted in Fig. 3 (open diamonds). As expected from a simple charge control model, it is always linear with V_D .

3.2 Effect of Ambient Temperature

Next, we study the effect of the ambient temperature on the ballistic transport at $V_D = 2$ mV. Fig. 4(a) shows a family of normalized transconductance curves corresponding to the first current plateau, measured at different temperatures. As the temperature increases, the height of the 1D transconductance peak decreases and the width is broadened. This trend is similar to that in Fig. 2(b) where the temperature was fixed but the drain bias increased. In Fig. 4(b), we plot the temperature dependence of the first peak transconductance. The dependence can be well explained using Eq. (4). For $T_a < 10$ K, g_{max} stays flat indicating the broadening is dominated by T_o . As T_a rises and becomes comparable with T_o , g_{max} starts to drop.

To fit the experimental data, T_o was adjusted but $\alpha = 6.2\%$ was kept the same as before. The best fitting as indicated by the solid line in Fig. 4(b) gives $T_o = 28.6$ K, which is close to the previous value obtained from the study of bias dependence. As shown in Fig. 4(b), for $T_a < 26$ K the fitting curve agrees well with the experimental data, but disagree for larger T_a . This implies that, above 26 K, the energy level broadening has exceeded the subbands' energy spacing.

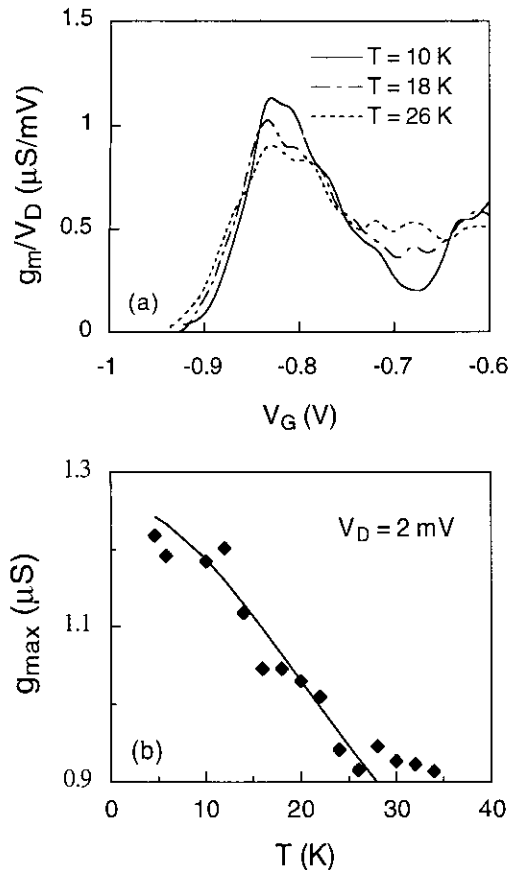


Fig. 4 (a) Normalized transconductance vs. split-gate voltage at different temperatures, (b) first ID peak transconductance vs. the temperature. The drain bias is 2 mV. The solid line is the curve fitting using Eq. (4).

Once the gate modulation coefficient is known, the separation between the first and the second 1D subbands can be estimated by $\Delta E_{12} = \alpha \Delta V_G$, where ΔV_G is the gate voltage separation between the first and the second peaks in g_m vs. V_G plot. From Fig. 2, $\Delta V_G \approx 0.22\text{ V}$, thus we obtain $\Delta E_{12} \approx 13.6\text{ meV}$. This value agrees with the maximum drain bias, $(V_D)_{\text{max}}$, that can be applied to observe the 1D ballistic transport. When the drain bias

approaches the subbands' separation, the 1D ballistic transport is suppressed.^{2,9} The subband spacing also can be estimated using $\Delta E_{12} \approx 3.5kT_{\text{eff}}$. For $T_0 = 28.6\text{ K}$ and $T_a = 26\text{ K}$, we obtain $T_{\text{eff}} = 38.7\text{ K}$, and hence $\Delta E_{12} \approx 11.7\text{ meV}$. Again, this value is in good agreement with the previous estimations.

4. Summary

In summary, the combined effects of bias and temperature on 1D ballistic transport are investigated. A simple equation that describes both effects is derived and found to fit experiments well. The other broadening due to gate leakage current heating and constriction potential shape are found to be significant, and they can be described in the form of equivalent temperatures. However, in the present work, the two factors cannot be separated. Work is underway to distinguish them by studying structures with different gate length.

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5. References

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