

Relationship Between Measured and Intrinsic Transconductances of FET's

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Abstract—In exploratory study of FET's, such as the study of deep-submicrometer-channel FET's, carrier transport quantities are extracted from the measured transconductance of a FET. The extraction requires that the intrinsic transconductance of the device be calculated from the measured one, which is generally degraded by source and drain parasitic resistances. We have derived an equation that allows the calculation of the intrinsic transconductance of a FET from the measured transconductance, under the assumption that source and drain series resistances are independent of bias. The derivation does not assume zero drain conductance, nor does it involve any specific FET model. Therefore, the derived equation works in both saturation and linear regions of a FET, regardless of its channel length. The equation was tested by adding external resistors in series with source or drain of ultra-short-channel MOSFET's. Within the accuracy of the measurements, experimental results have proved that the equation is correct.

I. INTRODUCTION

The measured transconductance of a FET g_m is always smaller than the intrinsic transconductance g_{mi} because of the effect of source-drain series resistance. In the case of high source-drain series resistance and/or of high intrinsic transconductance, the difference between the g_m and g_{mi} can be large. Since the intrinsic transconductance is directly related to the FET theory and in particular carrier transport properties, it is often required to extract accurately the intrinsic transconductance from the measured one. However, the commonly used equation [1], [2]

$$g_{mi} = g_m / (1 - R_S g_m) \quad (1)$$

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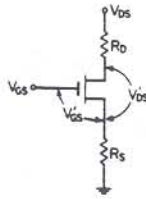


Fig. 1. Model for the source-drain series resistance of a FET.

where R_S is the parasitic series resistance at the source side, is accurate only when the drain conductance equals zero. Obviously, this condition is satisfied in a long-channel FET in saturation. In the linear region of any FET or in short-channel FET's with high drain (output) conductance, (1) becomes inaccurate. Using the usual small-signal equivalent model for a FET in the following section, we derive an equation that relates g_m to g_{mi} , with only one assumption, namely that the source and drain series resistances are independent of voltage bias. The derivation is independent of any specific FET model. Although source-drain series resistance effect is included in many CAD FET models, we believe that this is the first time that a comprehensive analytic equation is given. In Section III, experimental results show that (1) is indeed inadequate, and that the new equation works very well in both saturation and linear regions of short-channel MOSFET's.

II. DERIVATION

Suppose that a FET has a parasitic source-drain series resistance $R_{SD} = R_S + R_D$ as shown in Fig. 1, and that the R_S and R_D are independent of the voltage bias. The differential of drain current dI_{DS} can be written as

$$\begin{aligned} dI_{DS} &= (\partial I_{DS}/\partial V'_{GS})|_{V_{DS}} dV'_{GS} + (\partial I_{DS}/\partial V'_{DS})|_{V_{GS}} dV'_{DS} \\ &= g_{mi} dV'_{GS} + g_{di} dV'_{DS} \end{aligned} \quad (2)$$

where g_{di} is, by definition, the intrinsic drain conductance. Since

$$V'_{DS} = V_{DS} - R_{SD} I_{DS}$$

$$V'_{GS} = V_{GS} - R_S I_{DS}$$

it follows that at constant V_{DS} (i.e., $dV_{DS} = 0$)

$$dV'_{DS} = -R_{SD} dI_{DS} \quad (3)$$

$$dV'_{GS} = dV_{GS} - R_S dI_{DS}. \quad (4)$$

Putting (3) and (4) into (2), we have

$$g_{mi} = (1 + R_{SD} g_{di}) g_m / (1 - R_S g_m) \quad (5)$$

where $g_m \equiv (\partial I_{DS}/\partial V_{GS})|_{V_{DS}}$ is the measured transconductance. By a similar derivation, it can be readily shown that

$$g_{di} = (1 + R_S g_{mi}) g_d / (1 - R_{SD} g_d) \quad (6)$$

where $g_d \equiv (\partial I_{DS}/\partial V_{DS})|_{V_{GS}}$ is the measured drain conductance. From (5) and (6), we have the intrinsic transconductance

$$g_{mi} = g_m^0 / [1 - R_{SD} g_d (1 + R_S g_m^0)] \quad (7)$$

and the intrinsic drain conductance

$$g_{di} = g_d^0 / [1 - R_S g_m (1 + R_{SD} g_d^0)] \quad (8)$$

where $g_m^0 \equiv g_m / (1 - R_S g_m)$ and $g_d^0 \equiv g_d / (1 - R_{SD} g_d)$. Note that when drain conductance g_d is equal to zero, (7) becomes the same as (1).

III. COMPARISON WITH EXPERIMENTS

Two ultra-short-channel Si MOSFET's were used to test (7). Devices 1 and 2 have electrical channel lengths 145 and 125 nm, respectively, and were fabricated using X-ray lithography [3]. The channel lengths were determined by the so-called "closed channel" method (CC) and by an electrical measurement method (EM)

TABLE I
ELECTRICAL MEASUREMENT OF SOURCE-DRAIN SERIES RESISTANCE R_{SD} OF TWO SHORT-CHANNEL MOSFET'S

DEVICE	$R_{SD}(\Omega)$	ON DRAIN SIDE			ON SOURCE SIDE	
		$R_{ext}=0$	$R_{ext}=28\Omega$	$R_{ext}=51.3\Omega$	$R_{ext}=28\Omega$	$R_{ext}=51.3\Omega$
1	$\Delta(\Omega)$	95.4	124.6	149	123.5	147.6
	$\sigma(\%)$	0	29.2	53.6	28.1	52.2
	$\sigma(\%)$	0	1	1.5	0.01	0.6
2	$R_{SD}(\Omega)$	91.4	120.4	144.7	120.5	144.1
	$\Delta(\Omega)$	0	29	53.3	29.1	52.9
	$\sigma(\%)$	0	0.8	1.4	0.9	1

TABLE II
ELECTRICAL MEASUREMENT OF SOURCE-DRAIN SERIES RESISTANCE R_{SD} OF 5- μm -CHANNEL MOSFET AT DIFFERENT EXTERNAL SERIES RESISTANCE

R_{ext} (Ω)	R_{SD} (Ω)	Δ (Ω)	Error (%)
0	193.2	0	0
51.2	243.6	50.4	-0.4
100.1	293.9	100.7	0.2
201.7	394.7	201.5	-0.05
528.1	729.5	536.3	1.2
964.8	1152.8	959.6	-0.5

[3], [4]. Both devices showed well-behaved quasi-long channel I - V characteristics. An external resistor R_{ext} was put in series with source or drain of the devices. R_{SD} was measured by an electrical measurement method as described in the next paragraph. We assumed that $R_D = R_S$, when $R_{ext} = 0$. Therefore both R_{SD} and R_S can be determined. Then the transconductance g_m and the drain conductance g_d with various nonzero values of R_{ext} were measured at V_{DS} and V_{GS} , which corresponded to the same V'_{DS} and V'_{GS} to avoid errors introduced by the dependence of g_{mi} and g_{di} on these quantities. Finally, g_{mi} were calculated according to (7).

The electrical measurement of R_{SD} (EMR) is similar to the method proposed by Suci and Johnston [5]. In our case, the mobility degradation coefficient U_0 is negligible compared with $\beta_0 R_{SD}$, where $\beta_0 \sim 50$ mS/V. We dropped the U_0 term, so the R_{SD} of a device can be determined from its own I_{DS} versus V_{GS} measurement at low source-drain bias, without the cooperation of any additional devices. R_{SD} was assumed to be independent of gate voltage. This is justified in our case, because the n^+ sheet resistance dominates the total R_{SD} (due to nonself-aligned structure) and the spreading resistance at the corner of the n^+ region, which depends on gate voltage, is only about 3 percent of the n^+ sheet resistance. The accuracy of EMR was checked by putting external resistors R_{ext} in series with source or drain. The results are given in Table I, which shows that the error, $\sigma = (\Delta - R_{ext})/R_{SD}$, of EMR measurements is less than 2 percent, where $\Delta = R_{SD} - R_{SD}(0)$ and $R_{SD}(0)$ is the source-drain resistance measured at zero external series resistance. The measurement of source-drain series resistance of a 5- μm -channel Si MOSFET, which displayed impeccable long-channel characteristics, is shown in Table II. As can be seen, similar accuracy is obtained.

We measured the transconductance g_m and drain conductance g_d of the short-channel devices in the saturation region first. The g_{mi} calculated from (7) are shown in Table III. g_{mi}^0 is the conventionally corrected transconductance calculated from (1), and $\sigma^0 = (g_{mi}^0 - g_{mi}^0(R_{ext}=0))/g_{mi}^0(R_{ext}=0)$ and $\sigma = (g_{mi} - g_{mi}(R_{ext}=0))/g_{mi}^0(R_{ext}=0)$ are the relative errors of the two transconductances g_{mi}^0 and g_{mi} . Table III shows that g_{mi} calculated from different R_{ext} have errors smaller than 1.5 percent, except for device 2 when $R_{ext} = 28$ and 51.3 Ω . We believe that these larger errors are due to the inaccuracy in the g_m measurement, which is estimated about ± 5 percent (it can be shown from (7) that in our case the accuracy of R_S and R_D measurement is not as crucial as that of g_m measure-

TABLE III
INTRINSIC TRANSCONDUCTANCE AT SATURATION g_{mi} CALCULATED FROM MEASURED TRANSCONDUCTANCE g_m AND DRAIN CONDUCTANCE g_d AT DIFFERENT EXTERNAL SERIES RESISTANCE R_{ext}^D (IN SERIES WITH THE DRAIN) AND R_{ext}^S (IN SERIES WITH THE SOURCE)

		R_{SD} (Ω)	R_S (Ω)	g_m (mS)	g_d (mS)	g_{mi}^0 (mS)	σ^0 %	g_{mi} (mS)	σ %
DEVICE 1	$R_{ext}^D = 0$	95.4	47.7	4.53	1.2	5.78	0	6.77	0
	$R_{ext}^D = 20 \Omega$	124.6	47.7	4.4	1.16	5.56	-3.0	6.82	+0.7
	$R_{ext}^D = 51 \Omega$	149	47.7	4.27	1.12	5.36	-7.3	6.78	+0.2
	$R_{ext}^S = 20 \Omega$	123.5	75.8	4.0	0.92	5.74	-0.7	6.86	+1.3
	$R_{ext}^S = 51 \Omega$	147.6	99.9	3.55	0.84	5.50	-4.8	6.80	+0.4
DEVICE 2	$R_{ext}^D = 0$	91.4	45.7	5.04	1.8	6.55	0	8.33	0
	$R_{ext}^D = 20 \Omega$	120.4	45.7	4.73	1.76	6.03	-8	8.27	-0.7
	$R_{ext}^D = 51 \Omega$	144.7	45.7	4.52	1.70	5.70	-13	8.26	-0.8
	$R_{ext}^S = 20 \Omega$	120.5	74.8	4.1	1.45	5.91	-9.8	7.91	-5
	$R_{ext}^S = 51 \Omega$	144.1	98.4	3.7	1.2	5.81	-11.3	7.99	-4.1

TABLE IV
INTRINSIC TRANSCONDUCTANCE AT LINEAR REGION G_{mi} CALCULATED FROM MEASURED TRANSCONDUCTANCE g_m AND DRAIN CONDUCTANCE g_d AT DIFFERENT EXTERNAL SERIES RESISTANCE R_{ext}^D (IN SERIES WITH THE DRAIN) AND R_{ext}^S (IN SERIES WITH THE SOURCE)

		External Resistor	R_{SD} (Ω)	R_S (Ω)	g_m (mS)	g_d (mS)	g_{mi}^0 (mS)	σ^0 %	G_{mi} (mS)	σ %
DEVICE 1	$R_{ext}^D = 0$		95.4	47.7	0.42	5.8	0.429		0.984	
	$R_{ext}^D = 20$		124.6	47.7	0.39	4.9	0.397	8.3	1.052	+7%
	$R_{ext}^D = 51$		149	47.7	0.33	4.45	0.335	-21.9	1.027	+4%
	$R_{ext}^S = 20$		123.5	75.8	0.41	4.7	0.423	-1.5	1.055	+7.2%
	$R_{ext}^S = 51$		147.6	99.9	0.32	4.2	0.33	-23.1	0.919	-6.6%
DEVICE 2	$R_{ext}^D = 0$		91.4	45.7	0.34	6.95	0.345		0.974	
	$R_{ext}^D = 20$		120.4	45.7	0.3	5.8	0.304	-11.9	1.042	+7%
	$R_{ext}^D = 51$		144.7	45.7	0.24	5.15	0.242	-30	0.984	+1%
	$R_{ext}^S = 20$		120.5	74.8	0.28	5.7	0.286	-17.1	0.997	+2.4%
	$R_{ext}^S = 51$		144.1	98.4	0.22	5.2	0.224	-35	0.961	-1.3%

ment). If the g_m 's in this case were increased by less than 3 percent, the errors of g_{mi}^0 would become smaller than 0.5 percent. Note, however, that g_{mi}^0 has consistently larger errors than g_{mi} . Also note that the relative errors of g_{mi}^0 , σ^0 , are not random. Instead, it is always negative, and increasing as R_{ext} increases. This implies that σ^0 is caused by the inaccuracy of (1).

Equation (7) was further tested in the linear region of the MOSFET's. Results are shown in Table IV. It is well known that (1) fails in the linear region. Table IV shows that this is indeed the case. However, the errors of g_{mi} , calculated from (7), are less than 8 percent. Given an estimated ± 10 percent inaccuracy in g_m and g_d measurements in the linear region, the data fit (7) remarkably well.

A further indirect test of (7) in the linear region is to calculate the channel lengths L of devices from the extracted g_{mi} , using the quasi-long-channel model

$$L = WC_{ox}\mu_0 V_{DS}'/g_{mi} - V_{DS}'/E_c \quad (9)$$

(the derivation is given in the appendix), where W is the width of the device, C_{ox} is the capacitance of the gate oxide, μ_0 is the low lateral field mobility, and E_c is the critical field for velocity saturation. Use of the quasi-long-channel model is justified because the devices showed long-channel-like behavior at low V_{DS} . If g_{mi} is extracted accurately, L calculated in this way should be the same as that obtained from the other methods such as *CC* and *EM*. In fact, the L 's calculated from (9) with g_{mi} from (7) are 145 nm for

device 1 and 120 nm for device 2, which agree with L 's determined from the *CC* and *EM* methods within ± 5 percent.

Finally we comment on the effect of the drain conductance g_d . It can be seen from (7) that for a fixed intrinsic transconductance, the higher the drain conductance, the lower the measured transconductance. In other words, to achieve high measured transconductance, the drain conductance should be minimized.

IV. CONCLUSION

An equation relating the measured to the intrinsic transconductance of a FET has been derived. Within the measurement errors, experimental data show that the equation is correct in both saturation and linear regions, regardless of the channel length.

APPENDIX

For a long-channel MOSFET in the linear region ($V_{DS}' \ll V_{GS}' - V_T$), $g_{mi} = WC_{ox}\mu V_{DS}'/L$, where $\mu = \mu_0/(1 + V_{DS}'/E_c L)$. Putting the two equations together, we have (9) in the text. Two things should be pointed out: 1) equation (9) is accurate only when $V_{DS}' \ll E_c L$, and 2) E_c depends on temperature. At low temperatures, E_c can be much smaller than that at room temperature because $E_c \sim v_{SAT}/\mu_0$ where v_{SAT} is the saturation velocity, and μ_0 becomes very large at low temperatures. Therefore when doing measurements to extract MOSFET channel lengths at low temperatures, the condition $V_{DS}' \ll E_c L$ is more stringent than $V_{DS}' \ll (V_{GS}' - V_T)$.

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