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High resolution electron beam lithography and high accuracy overlay using a modified SEM

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Abstract

10 nm wide metal lines 30 nm apart, and 10 nm wide gaps over 300 nm long between two metal rectangles have been repeatedly achieved on thick GaAs substrates using a modified scanning electron microscope (SEM) operated at 35 keV and lift-off of Ni/Au. Sub-50 nm overlay accuracy in multi-level e-beam lithography has also been achieved using the same modified SEM.

1. INTRODUCTION

The fabrication of 10 nm lateral structures has been motivated by research on novel and high speed semiconductor devices. For example, lateral quantum effect devices require ultra-small gate geometry, and metal-semiconductor-metal photodetectors require extremely dense patterns of very fine structures for high performance. High overlay accuracy is necessary for complex device structures. Modified SEMs are ideal for nano-fabrication and nano-device research due to their high resolution, high flexibility, and low cost, but offer no direct means for high-accuracy multi-level overlay.

Previously, modified SEMs have been used to produce 10 nm wide isolated lines and gratings of 40 nm period with 12 nm linewidth on membranes [1], as well as 10 nm wide isolated lines and gratings of 40 nm period with 10 nm linewidths on bulk GaAs substrates using a 250 keV beam and chemically assisted ion beam etching [2]. However, little work has been reported on ultra-high overlay accuracy in multi-level e-beam lithography using a modified SEM.

The purpose of this paper is to present the study of lithographic resolution and overlay capability using a modified SEM operated at 35 kV. 10 nm metal features, either isolated or periodic with periods as small as 40 nm, have been consistently achieved on bulk GaAs substrates. Sub-50 nm overlay accuracy has also been accomplished using a lift-off technique with polymethyl methacrylate (PMMA) resists.

2. 10 nm E-BEAM LITHOGRAPHY

In order to achieve ultra-small structures in PMMA, the exposure of the resist by backscattered and laterally scattered electrons must be minimized.

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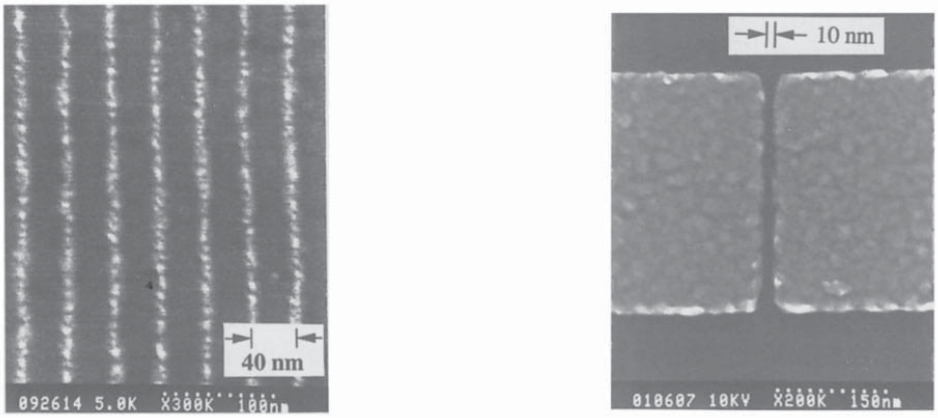
This can be accomplished by using thin resists and minimizing the exposure area. In our experiment, GaAs wafers were coated with a 45 nm thick layer of 950 K PMMA by spinning a 1.6% solution of 950 K PMMA (in chlorobenzene) at 6.0 krpm for 60 sec. The samples were then baked for 12 hrs at 165 °C. Our e-beam lithography system consists of a modified JEOL-840A SEM with a tungsten filament gun and a pattern generator designed and built ourselves. The pattern generator is a computer controlled system with 16 bit DACs, and the writing field can be divided into $2^8 \times 2^8$ to $2^{14} \times 2^{14}$ pixels. Several measures have been taken to reduce noise from floor vibrations and electronics. High resolution exposures are performed using a field size of 34 x 26 μm^2, and DAC resolution of $2^{12} \times 2^{12}$ pixels.

Exposures were performed with an accelerating voltage of 35 kV, a beam current of 4.5 pA, and a beam diameter of about 4 nm. Development was done at 23 °C using 2-ethoxyethanol:methanol (3:7) for 7 sec, methanol for 10 sec, and isopropanol for 30 sec. After development, metals were deposited by e-beam evaporation. Lift-off was performed by alternately soaking in warm acetone and spraying with a pressurized acetone jet.

Both isolated and densely spaced patterns with 10 nm features have been obtained. Figure 1 (a) shows a scanning electron micrograph of a 40 nm period grating with 10 nm linewidths on bulk GaAs. In this particular example only 3.5 nm of Ni and 4 nm of Au have been used, but lift-off is still possible with total thicknesses of at least 15 nm. The dose for the grating was 0.90 nC/cm and must be carefully controlled. The exposed grating lines were 2 μm long and lift-off of metal lines was successful for areas as wide as 1.3 μm. Figure 1 (b) shows a scanning electron micrograph of a Ni/Au (7 nm/8 nm) constricted gate with a gap of 10 nm and a gate length of 330 nm on bulk GaAs. The constricted gate was exposed with a dose of 480 $\mu C/cm^2$. This indicates that not only 10 nm lines but also 10 nm spaces can be achieved using a modified SEM operated at 35 kV with PMMA lift-off techniques. All of the above results are repeatable.



(a) (b)

Figure 1. Scanning electron micrographs of: (a) 40 nm period Ni/Au grating with 10 nm linewidth and (b) Ni/Au constricted gate structure with a gap of 10 nm and a length of 330 nm, both are on bulk GaAs

3. SUB-50 nm OVERLAY

To use a modified SEM to achieve high overlay accuracy, we selected a writing field size of 12 x 9.3 μm^2, corresponding to a magnification of 10 kX. The writing field is further divided into (a) the "device" area of 9 x 9.3 μm^2 located in the middle of the field, and (b) two alignment areas of 1.5 x 9.3 μm^2 located on each side of the "device" area.

In the first level of the multi-level e-beam lithography, test patterns consisting of paired nanoscale metal squares with various separations were defined in the central 9x9 μm^2 "device" area by a lift-off process, and 4.5 µm x 0.5 µm metal alignment marks for the second level e-beam lithography were defined in the alignment areas. A total metal thickness of 50 nm was sufficient for later alignment.

As illustrated in figure 2, in the second level of lithography, rectangular viewing windows were opened in the alignment area. The windows have a size which is just 0.1 µm larger than each edge of the alignment mark produced in the first level of the lithography. For perfect alignment, each alignment mark from the first level should be centered in each viewing window. The alignment marks were detected using a backscattered electron detector. Coarse alignment was performed using the SEM stage micrometers; final alignment was achieved using electronic image shifts and electronic rotation.

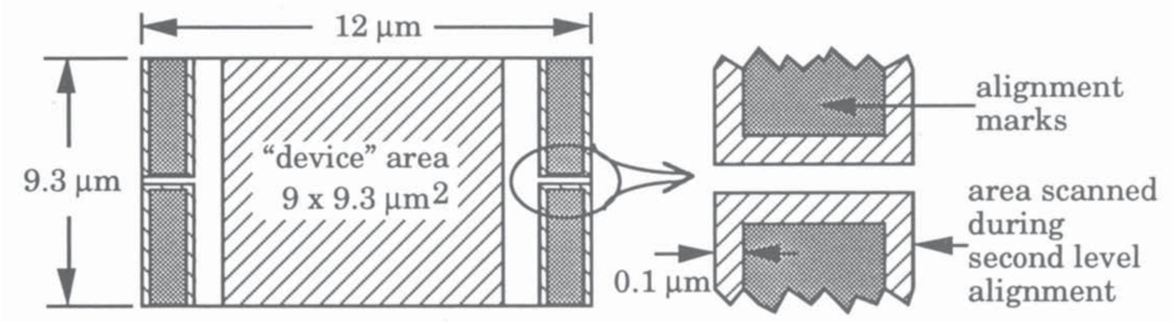
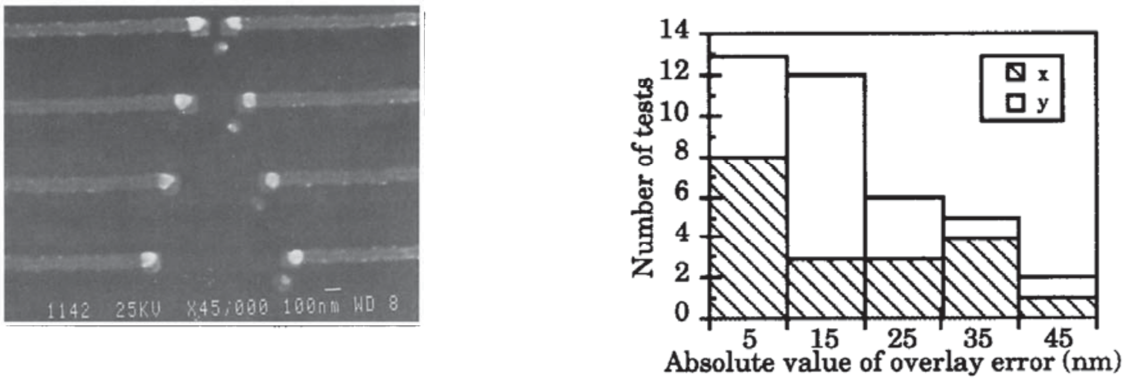


Figure 2. Schematic of the alignment scheme.

The "device" area was blanked during the alignment. Even so, the resist in the device area can be exposed by backscattered electrons from the alignment areas since the alignment windows are only 0.8 µm away from the device area. To minimize such proximity effects, the pixel resolution was reduced to 2^{10} x 2^{10}, to reduce the exposure intensity while still maintaining sufficient resolution for the alignment.

To check the overlay accuracy of the second level of the lithography, paired metal lines of nanoscale linewidth were defined in the "device" area, after alignment, exposure and lift-off. With perfect alignment, one end of each metal line in the second level should lay in the center of the squares placed by the first level. Figure 3 (a) is a scanning electron micrograph showing typical results. The four unintended dots were due to a software error in the second level of lithography. Figure 3 (b) is the summary of 19 alignment tests, indicating that the standard deviation of the overlay accuracy is 17 nm. Both x and y results have been superimposed on the same plot due to the limited number of data points. The results show that high overlay accuracy can be achieved with a modified SEM.



(a) (b)

Figure 3. (a) Scanning electron micrograph of two e-beam lithography levels with 20 nm accuracy. (b) Histogram showing the overlay accuracy in the x and y directions vs. the number of tests. The standard deviation is 17 nm.

4. CONCLUSIONS

A modified SEM has been used to fabricate ultra-small features and achieve ultra-high overlay accuracy, thus demonstrating the usefulness of modified SEMs for nanoscale device research. By using thin resists and minimizing exposure areas, 10 nm wide lines 30 nm apart, and 10 nm wide gaps over 300 nm long have been consistently defined on bulk GaAs substrates using a modified SEM operated at 35 keV, and lift-off of Ni/Au. Sub-50 nm overlay accuracy in multi-level e-beam lithography has also been achieved using the same modified SEM.

5. ACKKNOWLEDGMENTS

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6. REFERENCES

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