[2] J. Söderström and T. G. Andersson, "A multiple-state memory cell based on the resonant tunneling diode," *IEEE Electron Device Lett.*, vol. 9, pp. 200–202, 1988.
[3] Z. X. Yan and M. J. Deen, "A new resonant-tunnel diode-based multivalued memory circuit using a MESFET depletion load," *IEEE J. Solid-State Circuits*, vol. 27, no. 8, pp. 1198–1202, 1992.
[4] S. J. Wei and H. C. Lin, "Multivalued SRAM cell using resonant tunneling diodes," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 212–216, 1992.
[5] A. Raychaudhuri and M. J. Deen, "New state storage scheme for analog signals using four-state resonant tunneling devices," *Electron. Lett.*, vol. 29, no. 16, pp. 1435–1437, 1993.
[6] R. C. Potter, A. A. Lakhani and H. Hier, "Three and six logic states by the vertical integration of InAlAs/InGaAs resonant tunneling structures," *J. Appl. Phys.*, vol. 64, pp. 3735–3736, 1988.
[7] A. C. Seabaugh, Y. C. Kao and H. T. Yuan, "Nine-state resonant tunneling diode memory," *IEEE Electron Device Lett.*, vol. 13, no. 9, pp. 479–481, 1992.
[8] C. Y. Huang, J. E. Morris, Y. K. Su and T. H. Kuo, "New method of modeling a multipeak resonant tunneling diode," *Electron. Lett.*, vol. 30, pp. 1012–1013, 1994.
[9] C. Visweswariah and R. A. Rohrer, "Piecewise approximate circuit simulation," *IEEE Trans. Computer-Aided Design*, vol. 10, no. 7, pp. 861–870, 1991.
[10] *PSpice User's Guide*, MicroSim Corp., Fairbanks, CA, July 1989.

Threshold Voltage Sensitivity of 0.1 μm Channel Length Fully-Depleted SOI NMOSFET's with Back-Gate Bias

Effendi Leobandung and Stephen Y. Chou

***Abstract*— We found threshold voltage sensitivity to silicon thickness variation in 0.1 μm channel length fully-depleted SOI NMOSFET's can be reduced with lightly-doped channel and back-gate bias. However, after the back-interface is accumulated, the reduction is small and threshold voltage roll-off due to high drain bias increases.**

I. Introduction

For 0.1 μm channel length MOSFET's, high channel doping ($>5 \times 10^{17}$ cm^{-3}) is required to suppress short channel effects. This requirement creates special problems for fully-depleted SOI MOSFET's because the threshold voltage is very sensitive to silicon thickness variation. The threshold voltage variation can be eliminated by using a thick silicon layer thereby creating partially-depleted devices [1]. However, these devices suffer from floating body effects which translate into kink effects in the output characteristics. One way to eliminate the threshold voltage variation and maintain a fully-depleted channel is to eliminate high channel doping altogether and use back-gate bias to suppress short channel effects. Back-gate bias has been known to suppress short channel effects [2] regardless of the channel doping; therefore, a combination of lightly-doped channel doping and back-gate biasing can be used to produce 0.1 μm channel length fully-depleted SOI MOSFET's with minimal short channel effects and threshold voltage variation.

Manuscript received January 5, 1995; revised April 28, 1995. The review of this brief was arranged by Associate Editor K. Shenai. This work was supported in part by SRC under Contract 92-SJ-231 and NSF.
The authors are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 USA.
IEEE Log Number 9413288.

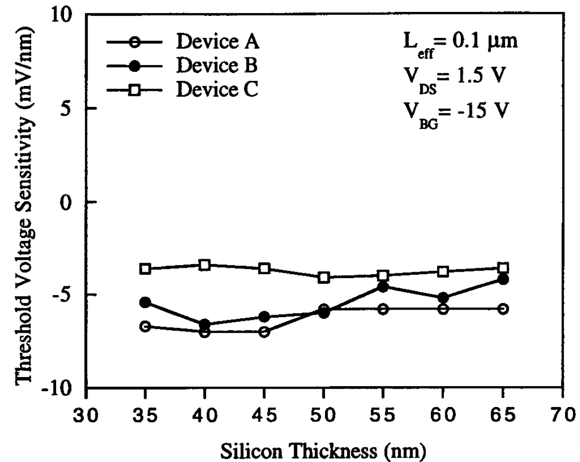


Fig. 1. PISCES simulation of threshold voltage sensitivity to silicon thickness variation. Device A: $N_A = 3 \times 10^{15}$ cm^{-3} and $t_{ox} = 9.5$ nm. Device B: $N_A = 5 \times 10^{16}$ cm^{-3} and $t_{ox} = 9.5$ nm. Device C: $N_A = 3 \times 10^{15}$ cm^{-3} and $t_{ox} = 5$ nm.

Even though numerous papers have been published regarding back-gate bias in SOI MOSFET's, none have discussed the study of back-gate bias effect on threshold voltage variation. In this paper, we report the first of such study on 0.1 μm channel length fully-depleted SOI NMOSFET's with very lightly-doped channel (3×10^{15} cm^{-3}).

II. Fabrication

The devices were fabricated on IBIS SIMOX wafer with 220 nm top silicon layer and 375 nm buried oxide. The wafer was thinned to 50 nm using wet oxidation and wet oxide etching. The channel was doped with 3×10^{15} cm^{-3} boron. LOCOS isolation was done with no field implant because all the silicon layer was consumed. The 9.6 nm gate oxide was grown in dry oxygen at 900°C. N-polysilicon gate electrodes were defined using electron beam lithography and reactive ion etching. The source and drain were implanted with 1×10^{15} cm^{-2} arsenic at 25 keV followed by a 20 minutes 850°C anneal in nitrogen. Pure Aluminum was used for metallization. All devices have channel width of 10 μm.

III. Analysis

PISCES simulation was used to determine the sensitivity of threshold voltage to silicon thickness for NMOSFET's with lightly-doped channel and back-gate bias. Fig. 1 shows the result with back-gate bias of -15 V. As can be seen, the threshold voltage sensitivity is around -6 mV/nm to -7 mV/nm for channel doping of 3×10^{15} cm^{-3}. The sensitivity is reduced slightly to around -6 mV/nm with higher channel doping of 5×10^{16} cm^{-3}. However, if the gate oxide is reduced to 5 nm, which is more common for 0.1 μm MOSFET's, the sensitivity can be reduced more to around -4 mV/nm. These numbers are betters than what is reported in [3] with constant dose approach. Fig. 2 shows the threshold voltage sensitivity as a function of back-gate bias. The threshold voltage sensitivity improves dramatically to -6 mV/nm at -15 V because the short channel effects are suppressed by the negative back-gate bias. After -15 V back-gate bias, the improvement is small because the back-interface is accumulated.

0018-9383/95$04.00 © 1995 IEEE

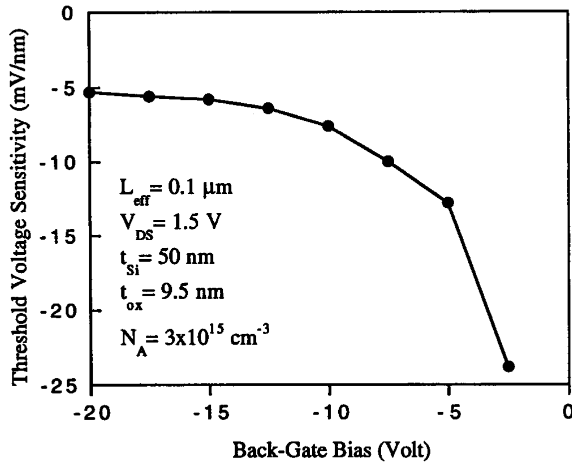
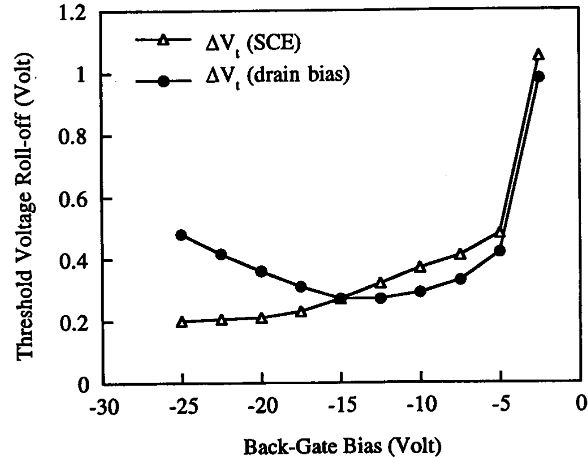


Fig. 2. PISCES simulation of threshold voltage sensitivity to silicon thickness variation as function of back-gate bias.

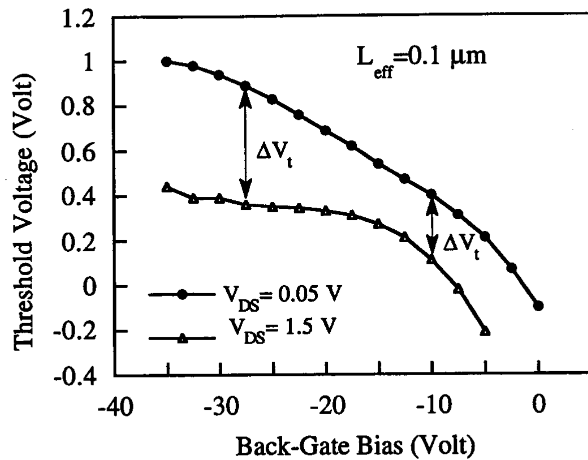
The experiment shows that biasing the back-gate beyond −15 V actually degrades the threshold voltage roll-off at high bias because the back-interface is accumulated. Fig. 3(a) shows the experimental threshold voltage roll-off due to SCE and drain bias as function of back-gate bias for 0.1 μm channel length devices. The threshold voltage roll-off due to drain bias is defined as threshold voltage difference at 1.5 V and 0.05 V drain biases. Threshold voltage roll-off due to SCE is defined as threshold voltage difference between 1 μm channel length device and 0.1 μm channel length device at 1.5 V drain bias. The threshold voltage roll-off due to SCE decreases with more negative back-gate bias. This is expected because of the reduction in short channel effects. However, the threshold voltage roll-off due to drain bias decreases with back-gate bias up to −15 V back-gate bias and then unexpectedly increases again. This can be explained by Fig. 3(b).

Fig. 3(b) shows the experimental threshold voltage of the 0.1 μm channel length SOI NMOSFET's as function of back-gate bias with two kind of drain biases. For low drain bias (50 mV), the threshold voltage increases with back-gate bias up to −32.5 V which means the back-interface accumulates at −32.5 V back-gate bias. However, at high drain bias (1.5 V), back-interface accumulates at significantly less back-gate bias (−15 V). This is what causes larger separation of low and high drain bias threshold voltage beyond −15 V back-gate bias as seen in Fig. 3(b).

The reason for the early accumulation at high drain bias is as follows. For very low channel doping and a thin silicon layer, the influence of front-gate bias on the back-interface is very strong. That is why large negative back-gate bias (−32.5 V) is needed in order to accumulate the back-interface at low drain bias. At high drain bias, impact ionization creates holes which will recombine at the source due to the fully-depleted layer. This recombination has been known to create a larger separation between hole and electron quasi Fermi-levels at the source-channel junction near the back-interface without lowering the source-channel junction potential barrier [4]. In other words, the source-channel junction is effectively forward biased without lowering the potential barrier. This is only possible because the holes effectively increase the channel doping near the back-interface. The extra channel doping shields the back-interface from the front-gate bias making it easier for back-gate bias to accumulate the back-interface. This is very pronounced in our case,



(a)



(b)

Fig. 3. (a) Measured threshold voltage roll-off due to drain bias and SCE as function of back-gate bias. (b) Measured threshold voltage as function of back-gate bias for 0.1 μm channel length NMOSFET's. ΔVt is the threshold voltage roll-off due to drain bias.

as seen in Fig. 3(b), because the original channel doping is very low. We call these phenomena impact ionization induced back-interface accumulation.

IV. Conclusion

We have demonstrated that negative back-gate bias is able to reduce threshold voltage sensitivity of fully depleted devices to −4 mV/nm. However, the back-gate should not be biased beyond the back-interface accumulation point because this would cause larger threshold voltage roll-off at high drain bias.

References

[1] G. G. Shahidi *et al.*, "A room temperature 0.1 μm CMOS on SOI," in *Dig. of Tech. Papers, IEEE VLSI Technol. Symp.*, 1993, pp. 27–28.

[2] C.-T. Lee and K. K. Young, "Submicrometer near-intrinsic thin film SOI complementary MOSFET's," *IEEE Trans. Electron Devices,* vol. 36, pp. 2537–2547, 1989.

[3] M. Sherony, L. Su, J. Chung, and D. Antoniadis, "Minimization of threshold voltage variation in SOI MOSFET's," in *IEEE Int. SOI Conf.*, 1994.

[4] J.-K. Choi and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFET's," *IEEE Trans. Electron Devices,* vol. 38, pp. 1384–1391, 1991.

Zero-Temperature-Coefficient Biasing Point of Partially Depleted SOI MOSFET's

Ashraf A. Osman, Mohamed A. Osman, Numan S. Dogan, and Mohamed A. Imam

***Abstract*— Experimental and analytical results of the front gate bias (V_{GS}) and the drain current (I_{DS}) with the drain voltage (V_{DS}) of partially depleted (PD) SOI MOSFET at the Zero-Temperature-Coefficient (ZTC) point over a very wide temperature ranges (25–300°C) are presented. Two distinct ZTC points are identified, one in the linear region and the other is in the saturation region. Additionally, the analysis takes into consideration the body effects, and mobility degradation with applied front gate bias. The analysis results are in excellent agreement with the experimental results.**

I. INTRODUCTION

Recently, there has been a growing interest in designing circuits that operate reliably at high temperatures. It is desirable to drive circuits designed for high temperature applications at a point where the drain current shows zero or very small variation with temperature. This criterion ensures that circuit parameters such as the offset voltage drift are less sensitive to the device matching tolerance. The Zero Temperature-coefficient (ZTC) point has been identified for bulk CMOS by Shoucair [1] and Prijic and coworkers [2] in both the linear and the saturation regions for temperatures between 27 and 200°C. Although, the SOI MOSFET technology is one of the most promising candidates for high temperature applications due to its attractive features of low leakage currents, reduced short channel effects, steeper subthreshold slopes, and suppression of the latch-up phenomenon [3], [4], very little work has been done to investigate the ZTC point for this technology. Groeseneken and coworkers [3] and Jeon and coworkers [4] demonstrated the existence of the ZTC point experimentally for thin and thick-film SOI MOSFET's, respectively. However, no analytical formulation to identify this point has been developed.

Until recently interest in SOI for scaled IC applications was focused on the fully depleted (FD) technology because of the previously mentioned reasons. However, recent work by Fossum and coworkers [5] exploited the merits of the PD SOI technology of the good control of the threshold voltage which is very useful in deep-submicrometer SOI CMOS design, and reduced self heating due to the increase of heat evacuation area compared to the FD [6]. The PD SOI suffers from kink effect which is problematic in analog circuit design. However, one way to eliminate this effect is to use source to body contacts which will keep the body to source junction reversed biased as discussed by Ver Ploeg and coworkers [7]. In this paper, we present an analytical and experimental investigation of the ZTC bias point (V_{GS}(ZTC)) of the (PD) SOI MOSFET in linear region and saturation regions. The analysis takes into account the temperature dependence model parameters such as threshold voltage, mobility, and the body effects. The analytical predictions are in very close agreement with experimental results in both operating regions.

Manuscript received June 13, 1994; revised May 10, 1995. The review of this brief was arranged by Associate Editor K. Shenai. This work was supported by the National Science Foundation through the NSF/Industry Center for the Design of Analog/Digital Integrated Circuits.

A. A. Osman, M. A. Osman, and N. S. Dogan are with the School of Electrical and Computer Engineering, Washington State University, Pullman, WA 99165-2752 USA.

M. A. Imam is with Micron Semiconductor, Inc., Boise, ID 83706-9698 USA.

IEEE Log Number 9413289.

II. ZTC POINT ANALYSIS

The drain current for PD SOI MOSFET has been reported by Lim and Fossum [8] as

$$I_{DS}(T) = \frac{W}{L}\mu_s(T)C_{ox}\times \left[(V_{GS}-V_{th}(T))V_{DS} - \frac{(1+\alpha(T))}{2}V_{DS}^2\right] \quad (1)$$

$$I_{DS}(T) = \frac{W}{2L}\mu_s(T)C_{ox}\frac{(V_{GS}-V_{th}(T))^2}{(1+\alpha(T))} \quad (2)$$

for the linear and saturation regions, respectively, without the explicit temperature dependence indicated in parenthesis. In (1) and (2), T, W, L, C_{ox}, and α are the temperature, channel width, length, the front gate oxide capacitance, and the body effect parameter, respectively. V_{GS} and V_{th} are the gate and threshold voltage while μ_s represent the carrier mobility which is modeled by [9]:

$$\mu_s(T) = \frac{\mu_o(T)}{1+\theta(T)[V_{GS}-V_{th}(T)]}. \quad (3)$$

The parameter $\theta(T)$ accounts for the degradation of the mobility with the applied transverse electric field. The parameter μ_o(T) is the low field-mobility which has temperature dependence of the form $\mu_o(300)(\frac{300}{T})^{k_1}$. The constant k_1 ideally is 1.5; however, several different values between ($1.5 \leq k_1 \leq 2.42$) have been reported [2]. In this work a value of 1.52 is found to provide the best fit.

The Zero-Temperature-Coefficient (ZTC) bias point is defined as the bias at which the drain current exhibits zero variation with temperature ($\frac{dI_{DS}(T)}{dT} = 0$). Using (1) and (2), and the ZTC point defintion, the gate bias at the ZTC point can be described by

$$V_{GS} = V_{th} + \frac{-B+\sqrt{B^2+4AC}}{2A}. \quad (4)$$

where A, B, and C are determined according to whether the ZTC point in the linear or saturation region. The approach used in the above equations is similar to that discussed by Shoucair [1] and Prijic [2] for bulk CMOS. In the linear region, the variables A, B, and C in (4) are found as

$$\begin{aligned} A =& \frac{k_1}{T}\theta(T) - \frac{d\theta(T)}{dT} \\ B =& \frac{k_1}{T}(1 - \frac{V_{DS}\theta(T)}{2}(1+\alpha(T))) \\ &+ (1+\alpha(T))V_{DS}\frac{d\theta(T)}{dT} + \theta(T)\frac{dV_{th}(T)}{dT} \\ &+ \theta(T)(\frac{dV_{th}(T)}{dT} + \frac{1}{2}\frac{d\alpha(T)}{dT}V_{DS}) \\ C =& \frac{k_1}{T}V_{DS}(1+\alpha(T)) + V_{DS}\theta(T)(1+\alpha(T))\frac{dV_{th}(T)}{dT} \\ &- (\frac{dV_{th}(T)}{dT} + \frac{d\alpha(T)}{2dT}V_{DS}). \end{aligned} \quad (5)$$

0018–9383/95$04.00 © 1995 IEEE