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CONDUCTANCE FLUCTUATIONS IN ULTRA-SHORT-CHANNEL Si MOSFETs

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Conductance fluctuations with gate voltage near threshold are observed at temperatures up to 10 K in metal-oxide-semiconductor field-effect transistors (MOSFETs) with wide (44 μm) but short ($\leqq 0.15\,\mu$m) channels. The reproducible variations are consistent with the universal conductance fluctuations predicted by Lee and Stone.

LEE AND STONE [1] have predicted that all disordered conductors will display universal fluctuations in their conductance from one sample to another, one value of the Fermi energy to another or one value of magnetic field to another. At zero temperature, the fluctuations are predicted to be of order e^2/h, independent of the size, shape or composition of the conductor.

The universal fluctuations have been observed in metal wires and rings [2] and in GaAs quantum-wells [3] and Si MOSFETs [4] that are long and narrow. The full e^2/h magnitude of the fluctuations is only seen if the length L and the width W of a two-dimensional sample are short compared to the inelastic diffusion length L_{in}, that is, when the conductance experiment is equivalent to a measurement of the transmission of electrons through the disordered sample. For samples with L and W larger than L_{in} the fluctuations are predicted to be the incoherent superposition of the fluctuations from the subsections with dimensions L_{in}^2. Of course, these blocks add differently in series and parallel. The resulting prediction for the fluctuations is

$$\Delta G = \frac{e^2}{h}\left(\frac{W}{L_{in}}\right)^{1/2}\left(\frac{L_{in}}{L}\right)^{3/2}. \tag{1}$$

This prediction was tested in elegant experiments by Skocpol *et al.* [5] using multiprobe Si MOSFETs fabricated using electron-beam lithography. Relying on the empirical relation

$$L_{in} = 15G\frac{h}{e^2}T^{-1/2}, \tag{2}$$

where G is the conductance per square and with T in K and L_{in} in nm, they found that equation (1) predicts the magnitude of the fluctuations for devices with widths in the range $40\,\text{nm} \leqq W \leqq 200\,\text{nm}$ and lengths in the range $150\,\text{nm} \leqq L \leqq 705\,\text{nm}$.

In an effort to study short-channel devices, we have fabricated MOSFETs that are short and wide. However, these devices also show fluctuations of the conductance consistent with the predictions of Lee and Stone [1].

N-channel MOSFETs with channel lengths ranging from 60 nm to 5 μm and widths of 44 μm were fabricated on a single (1 0 0) Si substrate. The fabrication technique, described previously, involves a combination of X-ray and optical lithographies [6, 7]. The channel length was determined by comparing the electrical properties of devices with various lengths [7, 8]. A rough estimate of the length was also obtained from Shubnikov–de Haas oscillations [9]. The MOSFETs have a 10 nm thick gate oxide and a channel doping of B at $5 \times 10^{17}\,\text{cm}^{-3}$. The electron mobility in the channel is 330 cm^2/V-s at 300 K and 2200 cm^2/V-s at 4.2 K, as determined from drain current (I_{DS}) vs gate-to-source voltage (V_{GS}) curves at low drain-source (V_{DS}) bias.

Figure 1 displays I_{DS} as a function of V_{GS} at various temperatures between 4.2 and 15 K for a 110 nm-channel MOSFET. For a given device, the fluctuations, which are clearly seen below ~ 10 K, are completely reproducible. However, the specific pattern of the fluctuations is peculiar to a given device. All devices with lengths in the range 90–150 nm display the fluctuations at 4.2 K, but long-channel devices (5 μm) do not. Figure 2 shows that the fluctuations become smaller with increasing V_{DS}. This may be simply a result of electron heating.

At 4.2 K the magnitude of the fluctuations is $\sim 5 \times 10^{-4}$ S, about ten times larger than e^2/h. This is in good agreement with the prediction of equation (1)

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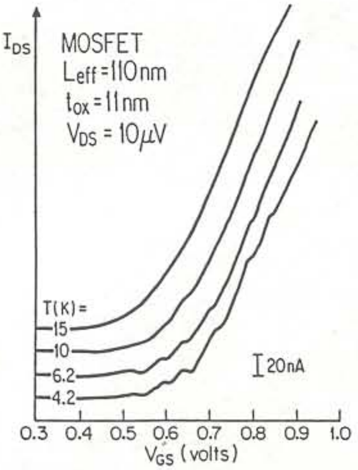

Fig. 1. Drain current of a 110-nm-channel-length MOSFET vs gate voltage at different temperatures. L_{eff} is the effective length as measured by comparison with longer devices, t_{ox} is the oxide thickness.

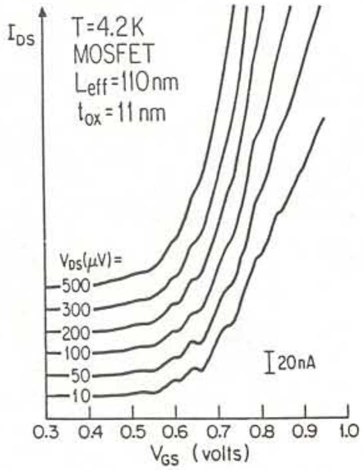

Fig. 2. Drain current of a 110-nm-channel-length MOSFET vs gate voltage at different drain-to-source (V_{DS}) voltages, at 4.2 K.

if we take $L_{in} \simeq L$. Since $W/L = 400$ the fluctuations would be 20 times larger than e^2/h because of the incoherent addition of 400 blocks of size $\sim L^2$.

There is additional evidence which suggests that this interpretation may be correct. At temperatures high enough that $L_{in} < L$ the fluctuations should decrease in size with increasing T because of the term $(L_{in}/L)^{3/2}$ in equation (1). But for temperatures where $L_{in} > L$, the fluctuations should actually increase with T because of the term $(W/L_{in})^{1/2}$. Figure 1 shows that the fluctuations do not change in size from 4 to 6 K indicating that L_{in} may approach L in this temperature range.

The interpretation of the data as evidence for the universal fluctuations is, by no means, unambiguous, however. For example, the empirical relation, equation (2), predicts an inelastic length much shorter than L for the low conductance region near threshold in which the fluctuations are most easily seen. Furthermore, there are peculiar non-linearities in the dependence of I_{DS} on V_{DS} which have not yet been thoroughly explored.

It is clear that magnetoresistance and lower temperature measurements are necessary before we can be sure that the fluctuations seen in Figs. 1 and 2 are fully consistent with the theoretical predictions. If they prove to be so this will be the first observation of the universal conductance fluctuations in devices which are short and wide.

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