

A room-temperature silicon single-electron metal–oxide–semiconductor memory with nanoscale floating-gate and ultranarrow channel

Lingjie Guo, Effendi Leobandung, and Stephen Y. Chou^{a)}

Department of Electrical Engineering, NanoStructure Laboratory, University of Minnesota, Minneapolis, Minnesota 55455

(Received 4 September 1996; accepted for publication 5 December 1996)

We have demonstrated a room-temperature silicon single-electron transistor memory that consists of (i) a narrow channel metal-oxide–semiconductor field-effect transistor with a width (~ 10 nm) smaller than the Debye screening length of single electron; and (ii) a nanoscale polysilicon dot ($\sim 7 \times 7$ nm) as the floating gate embedded between the channel and the control gate. We have observed that storing *one* electron on the floating gate can significantly screen the channel from the potential on the control gate, leading to a discrete shift in the threshold voltage, a staircase relationship between the charging voltage and the threshold shift, and a self-limiting charging process. © 1997 American Institute of Physics. [S0003-6951(97)00907-8]

Floating-gate metal–oxide–semiconductor (MOS) memories based on single-electron effect are very attractive, due to the possibility of a quantized threshold voltage shift, quantized charging voltage to create the shift, small device size, and fast charging time. However, fabrication of such devices demands cutting-edge nanotechnology. To relax fabrication requirement, the single-electron MOS memories (SEMMs) fabricated previously have nonconventional structures, such as a channel made of polysilicon or a floating gate consisting of many isolated silicon nanocrystals, but these devices suffer fluctuation in the device's dimension and performance.^{1,2} For example, the nature of the polysilicon channel SEMM prevents a precise control of the actual transistor channel width, the floating-gate size, and tunnel barrier thickness.¹ In the multinanocrystal floating-gate device, the size of the silicon nanocrystals have a broad distribution.² All of these statistical variations lead to a large fluctuation in the threshold voltage shift and in the charging voltage, therefore, they are unsuitable to large scale integration.

Here we present a single electron MOS memory having a narrow channel and a nanoscale floating gate with a well-controlled dimension. We report that the charging of a single electron to the floating gate will lead to, at room temperature, a quantized threshold voltage shift, a discrete charging voltage, and a self-limiting charging process.

As depicted in Fig. 1, there are two key features of our SEMM. (1) The width of silicon metal-oxide–semiconductor field-effect transistor (MOSFET) channel is narrower than the Debye screening length of a single electron; and (2) the floating gate is a nanoscale square (hence, called dot) to significantly increase single-electron charging energy as well as the quantization energy. Otherwise, the device is similar to an ordinary floating-gate MOS memory. The narrow channel ensures that storing a single electron on the floating gate is sufficient to screen the entire channel (i.e., the full channel width) from the potential on the control gate, leading to a significant threshold voltage shift. A small floating gate is used to significantly increase electron quantum energy (due to small size) and electron charging energy (due to small capacitance), hence, the threshold voltage shift and the

charging voltage become discrete and well separated at room temperature. Note that the control gate in our device is very long, but the device's threshold is determined by the section where the floating gate is located.

In fabrication, the narrow silicon channels with an initial channel thickness of 35 nm and an initial width varying from 25 to 120 nm were fabricated on silicon on insulator (SOI) using electron beam lithography and reactive ion etching (RIE). Next, square-shaped floating gates made of polysilicon were deposited and patterned using a second level e-beam lithography and RIE. The gate has a size almost the same as the channel width and an initial thickness of 11 nm. Then a 18 nm oxide was thermally grown, which would consume silicon, reducing the thickness of the polysilicon dot by about 9 nm, and the lateral size of the dot and the silicon channel width by about 18 nm. A plasma-enhanced chemical–vapor deposition oxide of 22 nm thick was deposited giving the total control oxide of 40 nm. A 3 μm -long polysilicon gate that covers the small floating gate and part of the narrow channel was deposited and patterned. After making final contacts, the devices were sintered to reduce the interface states. Many fabrications described here are similar to our previous work.^{3–5}

Note that in our devices, no tunnel oxide was intentionally added between the channel and polysilicon floating gate. The reason is twofold: (1) to allow fast charging and (2) to minimize the potential difference between the channel and the floating dot during the charging process, so that the Coulomb blockade effect can regulate the number of electrons

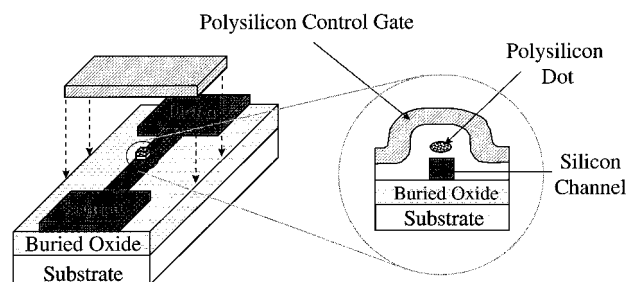


FIG. 1. Schematic of a single-electron MOS memory that has a narrow silicon channel and a nanoscale polysilicon dot as the floating gate. The cross-section view illustrates the floating gate and the channel region.

^{a)}Electronic mail: chou@ee.umn.edu

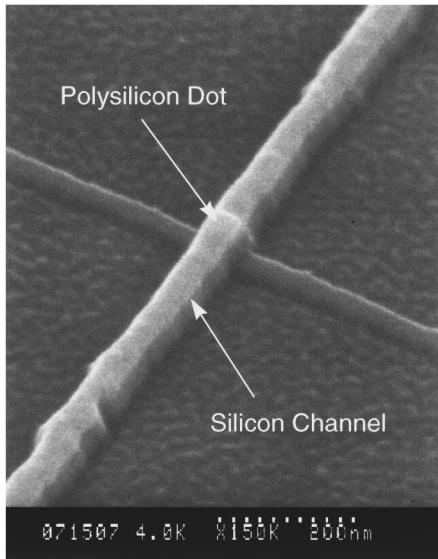


FIG. 2. Scanning electron micrograph of the narrow silicon channel and the polysilicon dot on top before size reduction by thermal oxidation. The width of the channel and the size of the dot are both 50 nm. The lines in buried oxide came from the second-level e-beam lithography and has no effect on device behavior.

that can be stored on the floating dot gate for a given charging voltage. In these devices, the potential barrier still exists between the channel and the floating gate, because of the grain boundary and a thin native oxide.

Figure 2 is a scanning electron micrograph (SEM) showing the polysilicon dot defined on top of the narrow silicon channel. For easy alignment, a line instead of a small square was exposed in the second level e-beam lithography, which creates the lines in the buried oxide but does not affect the electrical characteristics of the device.

The devices were characterized at room temperature using a two-step process. First, a voltage pulse positive relative to the grounded source was applied to the control gate and

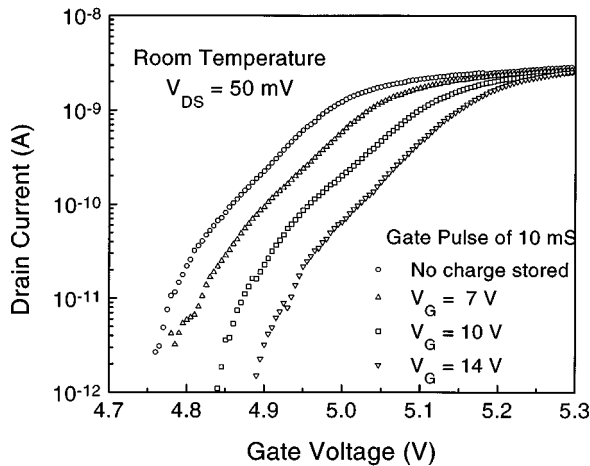


FIG. 3. Room temperature $I-V$ characteristics of a SEMM device before and after the charges being stored onto the floating dot. The threshold voltage (defined as the gate voltage at which the drain current reaches 100 pA) shift is quantized with $\Delta V_{th} \approx 55$ mV. The trace with (○) symbol represents the case where no charge is being stored in the dot, and the other three traces show the results after positive gate pulses had been applied with progressively larger magnitude.

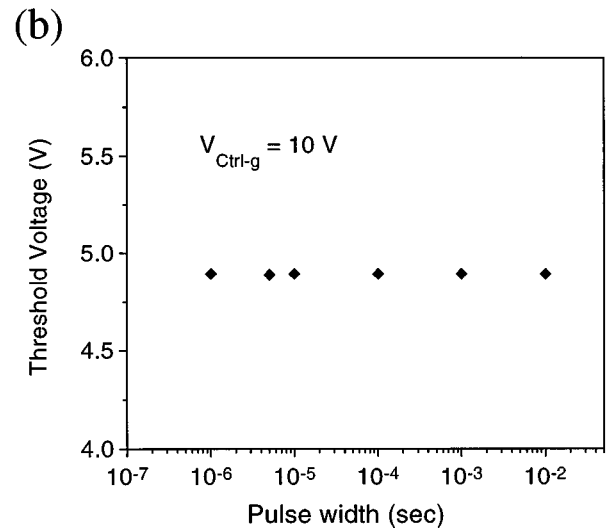
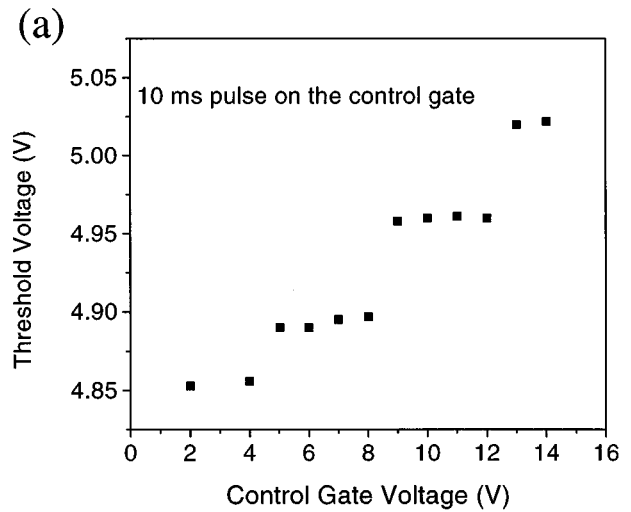


FIG. 4. (a) Threshold voltage as a function of the charging voltage on the control gate, showing a staircase relation with ~ 4 V for each stair. (b) Threshold voltage as a function of the charging time, while the charging voltage is fixed at 10 V.

the drain voltage was maintained at 50 mV. This would cause the electrons to tunnel from the channel to the floating gate. Then the drain current of the transistor was measured as a function of the gate voltage ($I-V$) with a 50 mV source-drain voltage, where the threshold voltage (V_{th}) shift was obtained. A simple switching circuit was used to allow the measurement of the $I-V$ characteristics to be taken within 1 s after the charging process was completed.

A SEMM that has a ~ 10 nm wide channel and a floating gate of a ~ 7 nm \times 7 nm square and 2 nm thick, the smallest in our fabrication, was characterized at room temperature under different charging voltages. The device dimension was estimated from SEM measurement and the oxidation rate. However, self-limiting oxidation might occur;⁶ in that case, the device could be slightly larger. Figure 3 shows the $I-V$ characteristics of the device after the control gate was charged by a different charging voltage from 2 to 14 V. Despite a continuous charging voltage, the threshold of the device always shifts a discrete increment of about 55 mV; and each threshold shift corresponds to a charging voltage interval of ~ 4 V. As shown in Fig. 4(a), there is a staircase

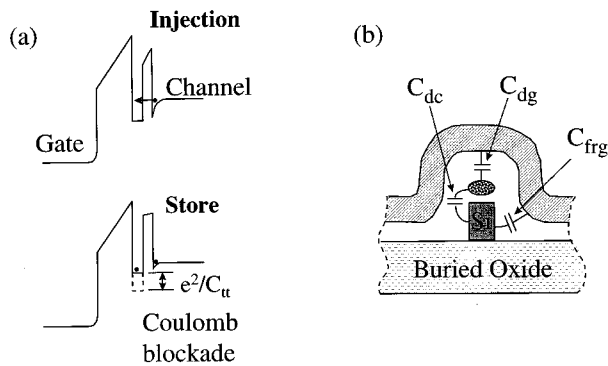


FIG. 5. (a) Schematic band diagram before and after an electron injection onto the dot. A single electron stored in the dot can raise its potential by e/C_u , blocking the other electrons in the channel from coming in. (b) Schematic cross section of the device showing the capacitive coupling between various elements.

relation between the threshold voltage shift and the charging voltage. Moreover, for a given charging voltage, the threshold shift is self-limiting, the threshold voltage shift is independent of the charging time, as shown in Fig. 4(b).

It should be pointed out since there is no intentional tunnel oxide, the charge stored at the floating gate can be held for an average of 5 s after the control-gate potential was set back to the ground, and after about 5 s the threshold voltage of the device returned to its original value (the first $I-V$ on the left in Fig. 3).

The behavior of the device can be explained by the single-electron charging effect. First, since there is little oxide between the channel and the floating gate, the charging voltage primarily drops between the control gate and the floating gate. To add one electron onto the floating gate requires an increment in the charging voltage of the e/C_{dg} , where C_{dg} is the capacitance between the control gate and floating gate [Fig. 5(b)]. The capacitance C_{dg} for the 7 nm \times 7 nm floating gate and a 40 nm control oxide is 4.4×10^{-20} F, giving a single-electron charging voltage of 3.6 V, consistent with the experimental value of 4 V.

Second, the shift in the SEMM's threshold voltage due to one electron stored in the floating gate is given by $\Delta V_{th} \approx e/(C_{dg} + C_{frg})$.¹ Here C_{frg} is added to account for the fact that the control gate wraps around the channel, therefore, the channel is only partially screened by the floating gate. For a conventional floating gate MOS memory, $C_{frg} = 0$, and ΔV_{th} is reduced to the usual form $\Delta V_{th} \approx e/C_{dg}$. In our devices, C_{frg} is many orders of magnitude larger than C_{dg} . The C_{frg} can be estimated from single-electron Debye screen length (~ 70 nm) and the channel thickness (26 nm). For the control oxide thickness of 40 nm and the area of (70 \times 26 nm), the C_{frg} is 2.5 aF and e/C_{frg} is 64 mV, which is again consistent with the experiment.

Third, the self-limiting charging process can be explained by three factors [Fig. 5(a)]. (1) the energy-level spacing in the floating gate, which must be overcome to charge an electron into the floating gate, is large compared with $k_B T$. For a 7-nm-by-7-nm silicon square embedded in SiO₂, the energy spacing due to quantum confinement is ~ 50 meV and the Coulomb charging energy is ~ 30 meV (assuming the oxide between the dot and channel is 1 nm thick);⁸ (2) since the barrier layer is thin, the voltage drop between the channel and the floating gate is very small; and (3) once one electron is added in the floating gate, the potential of the floating gate will raise, further reducing the voltage drop between the channel and the gate and preventing another electron from charging into the floating gate. Therefore, for a fixed charging voltage, the charging process is self-regulated and stops once the floating gate is charged with a fixed number of electrons, leading to a threshold shift independent of charging time and a staircase relation between the charging voltage and the threshold shift.

Now we would like to discuss a number of other issues. First, the discrete threshold shift is not due to the interfacial traps. The threshold shift due to the traps will not give the multiple equally spaced threshold shift and will have a charging process time dependent.⁷ And second, despite an extremely small floating gate and a very low channel doping concentration, the device did not exhibit short channel effects. This is because the inversion layer induced by the control gate effectively acts as an ultrashallow source and drain for the device, making the short channel effect negligible.

In summary, we have demonstrated the first single-electron memory in crystalline silicon MOSFET that has only one floating polysilicon dot as the charge storage node. The quantized shift in threshold voltage, quantized charging voltage, and self-regulated charging process has been observed at room temperature, which is attributed to the single-electron effect.

This work was partially supported by DARPA, ONR, ARO, and NSF.

¹K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE Trans. Electron Devices **41**, 1628 (1994).

²S. Tiwari, F. Rana, H. Hanai, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).

³P. B. Fischer and S. Y. Chou, Appl. Phys. Lett. **62**, 2989 (1993).

⁴P. B. Fischer and S. Y. Chou, J. Vac. Sci. Technol. B **11**, 2524 (1993).

⁵E. Leobandung, L. Guo, and S. Y. Chou, J. Vac. Sci. Technol. B **13**, 2865 (1995).

⁶H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, Appl. Phys. Lett. **64**, 1383 (1994).

⁷See, for example, J. R. Davis, *Instabilities in MOS Devices* (Gordon and Breach, New York, 1980).

⁸The capacitance between the floating gate and the channel was also taken into account using the image charge method.