Lateral resonant tunneling field-effect transistor

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A lateral resonant tunneling field-effect transistor (RTFET) is proposed. The RTFET has three closely spaced, but independent gate electrodes. The two outer gates create lateral double potential barriers in the channel, and control the barrier heights. The inner gate controls the potential of the quantum well between the barriers. These gates are capacitively coupled to the barriers and well; therefore, very small gate currents and high input impedences result. Modeling and computer simulations show that when the potential of the quantum well is scanned, the RTFET should have a better peak-to-valley ratio, narrower current peak widths, and more uniform distribution of peak and valley currents than that of a resonant tunneling diode with the same barriers and well. The independent control of the barrier heights allows us to adjust continuously the peak-to-valley ratio, amplitude, and position of current peaks. Furthermore, using an additional back gate, the peak-to-valley ratio and amplitude of peak current can also be adjusted by changing the carrier concentration next to the double barriers.

Resonant tunneling (RT) transistors are very attractive for their potential applications in ultrahigh speed circuits. Several double-barrier RT bipolar transistors and field-effect transistors (FET's) have been proposed. Most of these transistors can be divided into two classes. In the first class, a double-barrier RT structure is built in a transistor, and acts as a diode in series with the rest of the device; therefore, the potential in the quantum well cannot be adjusted independently. Examples of this kind of devices are the devices in which a double-barrier RT structure is (a) inside of the base,[1] (b) between the emitter and the base,[2] (c) in series with the source,[3] and (d) in series with the drain.[4] The other class of RT transistors are those in which a base electrode is used to contact the quantum well directly in order to control independently the well potential.[5,6] This kind of device is believed to have advantages over the first kind, such as more controllable RT peaks, a better peak-to-valley ratio, and narrower peak width; however, large base current in these devices can destroy the device operation.

As lithography and other semiconductor device fabrication technologies continue to improve, it becomes possible to fabricate lateral microstructures of sizes on the order of 10 nm. With such technology, lateral surface quantization can be realized. In this letter, we propose a novel lateral resonant tunneling FET (RTFET), in which the well potential as well as the barrier heights can be adjusted independently and continuously by using three gate electrodes. These gates are coupled capacitively to the well and barriers; therefore, very small gate current and high input impedence result. This device offers many unique advantages that other RT transistors do not have.

As shown in Fig. 1 (a), the proposed lateral RTFET consists of GaAs and AlGaAs modulation-doped layers, a source and a drain similar in structure to a modulation-doped FET, but with three independent fine finger gates close to each other. The outer gates are used for creating two potential barriers and the inner gate is used for controlling the potential of the quantum well. The energy diagram of this device is shown in Fig. 1 (b).

In the operation of the device, a two-dimensional electron gas forms in GaAs under the AlGaAs, just as in a conventional modulation-doped FET, and a potential is applied between the source and drain. The two outer gates modulate the channel potential in such way that a lateral double-barrier potential is formed, and the inner gate moves the well potential up and down. When the electron inelastic scattering length is longer than the active length of the device, electrons at the source side may tunnel through the lateral surface double barrier to the drain side. The drain current reaches its peak when the resonant tunneling condition is satisfied. The outer gates can control the barrier heights, and therefore can be used to adjust resonant tunneling condi-

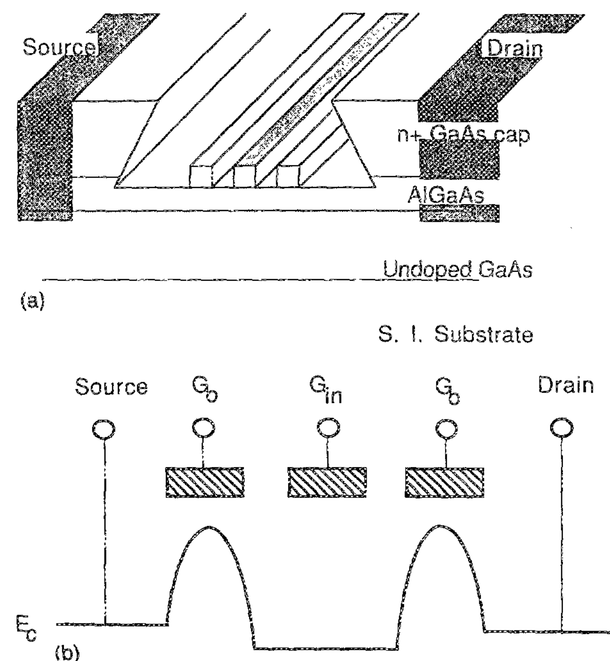

FIG. 1. (a) Schematic and (b) the energy-band diagram of a lateral resonant tunneling FET (RTFET).

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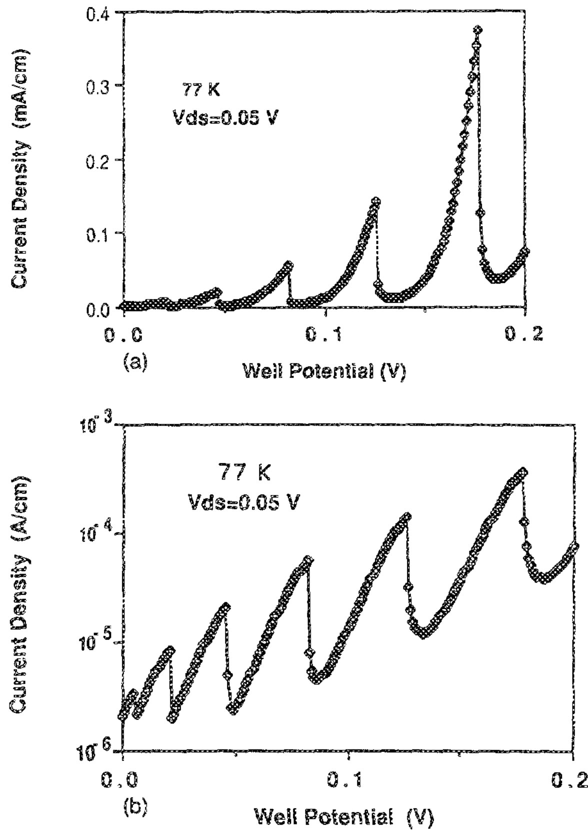

FIG. 2. (a) Linear and (b) the log plots of tunneling current vs the well potential for a lateral RTFET, assuming that each parabolic barrier is 10 nm thick and 0.23 eV in barrier height, the well is 30 nm wide, and the Fermi level is 4.4 meV.

tions. If a back gate is used, the carrier concentration next to the double barrier can be adjusted continuously. Clearly, the lateral RTFET can offer three new freedoms in the device operation: the independent and continuous tuning of (i) the quantum well, (ii) the barrier height, and (iii) the carrier concentration (so the Fermi level).

We modeled and simulated the current-voltage (I-V) characteristics of the device. We assume, as shown in Fig. 1 (b), that each finger gate is 10 nm wide and 10 nm apart, and that the potential under the two outer gates is parabolic and has a barrier height 0.23 eV. We divide the potential of each barrier into seven segments and assume that the potential in each segment is constant. Since electrons induced in GaAs have only two degrees of freedom, a two-dimensional electron supply function is used.[7] The tunneling current density at a given source-and-drain bias, V_{DS}, is given by

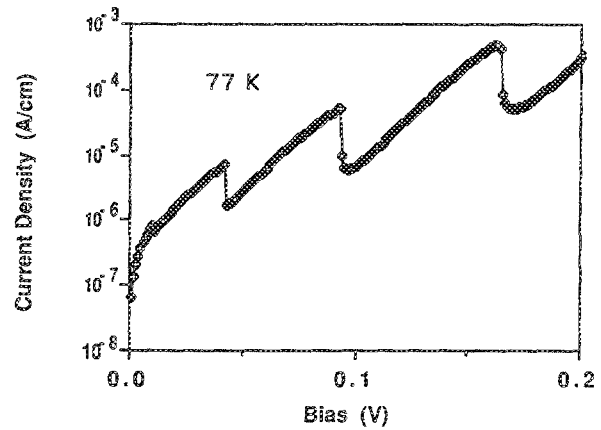

FIG. 3. I-V characteristic of a RT diode with the same barriers and well as those of the RTFET shown in Fig. 2.

$$J^2 = \frac{q}{\pi h} \int dE_l |T|^2 \int dk_y [f(E) - f(E + qV_{DS})],$$

where $|T|^2$ is the electron tunneling probability, h is the Planck constant, $f(E)$ is the Fermi–Dirac function, E_l is the electron energy in the transport direction, and $E = E_l + E_x + E_y$ in which E_x is quantized. In the simulation, we assume that only the ground state of E_x is involved,[8] and do not consider the effects of accumulation, depletion, and scattering.

We simulated the I-V characteristics of the device at 77 K, assuming 2×10^{11} cm^{-2} electrons in the channel. Figure 2 (a) shows a linear plot of drain current density of the device versus the well potential controlled by the inner gate bias, when V_{DS} is 0.05 V and the well potential is scanned from 0 to 0.2 V. Five RT peaks are clearly seen. Figure 2 (b) shows the log plot of the tunneling current, and shows six peaks. The first peak is too small, compared to the sixth peak, to be seen on a linear scale. The multiple peaks are due to the fact that the well width is rather wide, so that there are several quasi-eigenstates in the well. For a diode with the same double-barrier quantum well structure, only four peaks are observed when the source-and-drain voltage is scanned from 0 to 0.2 V, as shown in Fig. 3. Table I shows the voltage at which the peaks occur, the peak-to-valley (PTV) ratio, peak current, valley current, and peak width at half-maximum for the RT FET and diode. We can see that the well potential for the current peaks in the lateral RTFET is half of the bias for the corresponding peaks in the diode. This is expected, because with symmetrical barriers, only half as much voltage is needed to pull down an energy level from inside the well as

TABLE I. Peak position, PTV ratio, peak current, valley current, and peak full width at half-maximum (FWHM) for the RTFET and RT diode.

	1st Peak		2nd Peak		3rd Peak		4th Peak	
	FET	Diode	FET	Diode	FET	Diode	FET	Diode
Peak position (meV)	5	10	21	42	46	93	82	163
PTV ratio	1.5	1.3	4.5	4.2	8.7	8.6	12.3	10.2
Peak I (μA/cm)	3.4	0.84	9	7.1	21	52	56	500
Valley I (μA/cm)	2.2	0.65	2	1.7	2.4	6.1	4.5	48
FWHM (meV)	···	···	8	12	9	13	10	14

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from outside. The peak-to-valley ratio in the lateral RTFET is slightly better than that of the diode. In addition, the peak and valley currents in the lateral RTFET are more uniform than those in the diode. The better PTV ratio and more uniform current peaks are related to the fact that the symmetry of two barriers can be better preserved in a RTFET operated at a fixed low source-and-drain bias, than in a diode.

Figure 4 shows the *I-V* characteristics of a RTFET, with the same structure and carrier concentration as the device shown in Fig. 2, except that the barrier height is raised to 0.35 eV using the outer gates. Comparing with *I-V* characteristics in Fig. 2, we found that under the same biasing conditions, with the higher barrier height, the peak current decreases, the PTV ratio increases, and the peak width remains almost unchanged. The increase of the PTV ratio due to the increase of the barrier height becomes larger for higher peak number; for example, for the fifth peak, the PTV ratio increases by a factor of 6, when the barrier height is increased from 0.23 to 0.35 eV. Figure 4 also shows that the peak positions shift to higher voltages when the barrier height becomes higher. The shift increases with the peak number; there is almost no peak position shift at the first peak, but a 20 meV shift at the 6th peak. We expect the shift of the peak position in a real device to be larger than what we simulated here, because in a real device the well bottom will be bow shaped instead of flat. From the above discussion, we can see that the outer gates provide a novel opportunity to adjust continuously the PTV ratio, amplitude, and position of current peaks. Obviously, it is also possible to bias the two outer gates separately to make the two barrier heights different. This kind of operation is, sometimes, advantageous.

We would like to point out that using a back gate, the carrier concentration next to the barriers and therefore the Fermi level can be tuned. This tuning offers another way to adjust the PTV ratio and amplitude of current peak. The details of this effect will be discussed elsewhere.[9]

We should point out that the active length of the device can be longer than that assumed here, as long as it is comparable to the electron inelastic scattering length. Thick barriers can reduce the tunneling current density; on the other hand, however, the current density can be increased by lowering the barrier height.

Finally, we should point out that the potential variation created by the three finger gates decreases roughly by a factor of $\exp(2\pi z/d)$, as the gate-to-channel distance, z, increases, where d is the separation between the centers of two outer gates.[10] For example, if $d = 60$ nm, the damping factor is ~ 5 for a gate-to-channel distance of 15 nm. Therefore, in order to create an adequate double-barrier potential, the AlGaAs should be as thin as possible. On the other hand, the AlGaAs should be thick enough to avoid large gate tunneling current.

In summary, the proposed lateral RTFET is a novel multiple-gate tunneling device. Its well potential, barrier heights, and carrier concentration can be adjusted independently and continuously, without having large gate currents. Using the inner gate to adjust the well potential, a resonance condition can be achieved without applying a large source-and-drain bias. As a result, the RTFET has a better peak-to-valley ratio, and a narrower peak width than a RT diode with the same structure. Using the two outer gates, the barrier heights, and therefore, the PTV ratio, amplitude, and position of the current peak can be adjusted continuously. Finally, using a back gate, the peak-to-valley ratio and amplitude of current peak can also be adjusted by changing the carrier concentration. Because of these unique advantages, the lateral RTFET should have a high potential in high-speed electronics applications, and should be a powerful vehicle for studying the resonant tunneling.

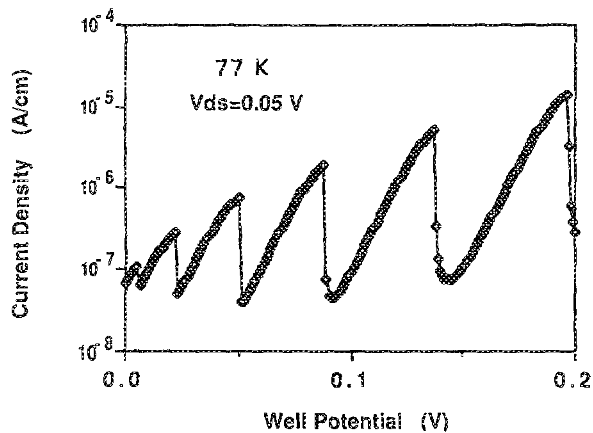

FIG. 4. Tunneling current vs the well potential for a lateral RTFET, assuming every device parameter is the same as that given in Fig. 2, except that the barrier height is 0.35 eV.

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