

# Nanoscale silicon field effect transistors fabricated using imprint lithography

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We report the fabrication and characterization of nanoscale silicon field effect transistors using nanoimprint lithography. With this lithographic technique and dry etching, we have patterned a variety of nanoscale transistor features in silicon, including 100 nm wire channels, 250-nm-diam quantum dots, and ring structures with 100 nm ring width, over a 2×2 cm lithography field with good uniformity. Compared with devices fabricated by the conventional electron-beam lithography, we did not observe any degradation in the device characteristics. The successful fabrication of the semiconductor nanodevices represents a step forward to make nanoimprint lithography a viable technique for the mass production of semiconductor devices. © 1997 American Institute of Physics. [S0003-6951(97)01039-5]

Nanoimprint lithography (NIL), a new lithography paradigm, promises to fabricate sub-10 nm structures with high throughput and low cost.<sup>1,2</sup> However, NIL has not been used to fabricate semiconductor devices, so the effects of NIL on the device performance, such as the effects of high pressure, have not been examined. In this letter, we report for the first time the fabrication of nanoscale silicon transistors using nanoimprint lithography, and examine the effects of NIL on device performance.

Nanoimprint lithography creates nanostructures in a resist by deformation of the resist shape with embossing, rather than by modification of the resist chemical structures with radiation or self-assembly. During NIL, a mold with nanometer scale features is first pressed into a thin layer of specially prepared polymer—polymethyl methacrylate (PMMA) that is coated on the substrate. This process creates a thickness contrast pattern in the polymer. After the mold is removed, an anisotropic etching process is used to transfer the pattern through the entire resist layer by removing the residual polymer in the compressed areas, completing the imprint lithography.

The transistors were fabricated on a silicon-on-insulator (SOI) wafer using a three level lithography process. In the first level, both the transistors' active areas containing nanoscale channel features and the alignment marks were patterned using imprint lithography. In the second and third levels, the gates and the final metal contacts were patterned using conventional photolithography. The starting SOI wafer was made using separation by implanted oxygen (SIMOX). The top (100) *p*-type silicon layer had a boron doping of  $3 \times 10^{15} \text{ cm}^{-3}$ , and was thinned to 70 nm thick. After growing a 30 nm thick sacrificial oxide layer to protect the silicon during the imprint lithography, a 200-nm-thick PMMA resist layer was spun on. The PMMA polymer was specially prepared to have good mold releasing properties.

The mold was formed in the thermally grown SiO<sub>2</sub> layer

on a silicon substrate. The mold has patterns for both the active areas of the transistors and the alignment marks for the subsequent photolithography steps [Fig. 1(a)]. The nanoscale channel features in the active area were defined by using electron beam lithography, while the large  $15 \mu\text{m} \times 12 \mu\text{m}$  mesa for the source-drain region of the transistors and alignment marks were defined by photolithography and lift-off. These patterns were transferred into the SiO<sub>2</sub> layer using reactive ion etching (RIE). The final SiO<sub>2</sub> mold had intrusion features 110 nm deep.

In imprinting [Fig. 1(a)], both the mold and PMMA were heated to 175 °C, well above the glass transition tem-

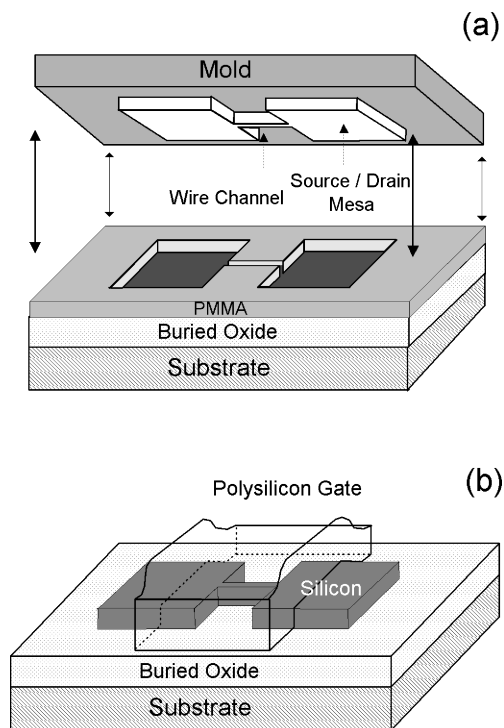


FIG. 1. (a) Imprint lithography based on compression molding to create thickness contrast pattern in PMMA resist carried on the wafer substrate. (For clarity, the feature sizes are not drawn to scale). (b) Schematic of the wire channel transistor defined by nanoimprint lithography in SOI.

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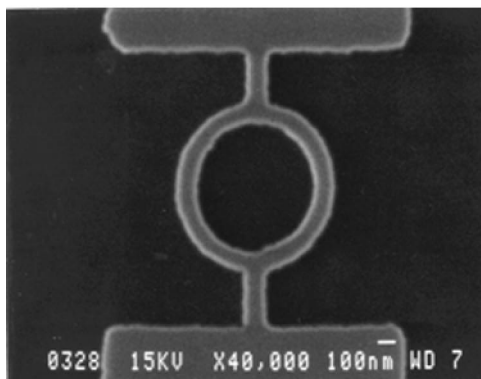
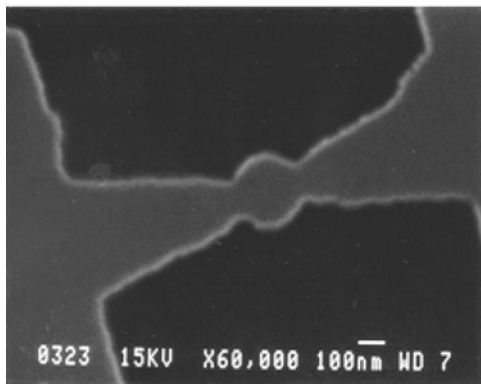
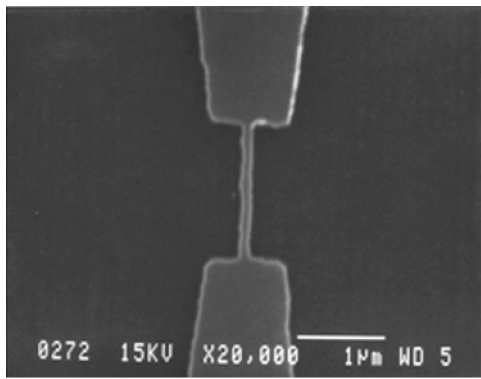


FIG. 2. Nanoscale features in top silicon layer of SOI defined by nanoimprint lithography, lift-off, and RIE: (a) wire channel, (b) quantum dot channel, and (c) ring channel.

perature of the PMMA (105 °C) where the polymer becomes a viscous fluid. The mold was then pressed into the PMMA resist using a pressure of  $4.5 \times 10^6$  Pa to create a thickness contrast in the PMMA. The mold was separated from the PMMA resist after the temperature cooled to below the PMMA's glass transition temperature, thus preserving the thickness contrast in the PMMA. The residual thin resist in the compressed region was removed by anisotropic oxygen RIE. The patterned PMMA was used as a template for a 20 nm Cr lift-off. The Cr pattern was then used as a RIE mask to transfer the pattern into SOI. First, fluorine-based RIE etched away the 30 nm sacrificial oxide. Then chlorine-based RIE further transferred the pattern into the 70-nm-thick silicon layer. The Cr mask was then removed using a common Cr etchant and the sacrificial oxide was removed by wet etch. Figure 2(a) shows a 100 nm wire channel metal-oxide semiconductor field effect transistor (MOSFET), Fig. 2(b) a 250 nm quantum dot, and Fig. 2(c) a 100-nm-wide ring structure

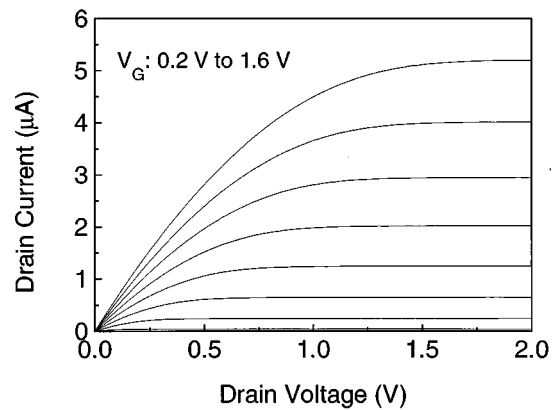


FIG. 3. Current-voltage ( $I$ - $V$ ) characteristics of a wire channel MOSFET at room temperature.

in the silicon layer. These features have the same shape and size as those in the mold, indicating that the nanoimprint has high fidelity during pattern transfer. In addition, we have achieved good pattern uniformity over the entire 2 cm  $\times$  2 cm imprint lithography field. Detailed studies of transfer fidelity and pattern uniformity, as well as mold durability were discussed elsewhere.<sup>3</sup>

The rest of the device fabrication, similar to what we have reported previously in the fabrication of the silicon quantum dot transistors,<sup>4</sup> is briefly described here. After the active device area was defined using NIL and transferred using RIE into the silicon layer of SOI, a 30 nm gate oxide was grown at 1000 °C for 20 min, which also annealed the RIE damage. The width of the wire channel and the size of the quantum dot were also reduced during gate oxidation. Next, polycrystalline silicon was deposited and photolithography was used to define the polysilicon gate that covers the entire channel region of the transistors [Fig. 1(b)]. Then an ion implantation was performed to form the self-aligned source and drain, followed by a second photolithography to define the final metallization contacts and to complete the process.

The room temperature characteristics (drain current versus drain bias) of the 100 nm wire channel MOSFET with 2  $\mu$ m channel length [similar to Fig. 2(a)] is shown in Fig. 3. The device is well behaved with a threshold voltage of 0.2 V and a subthreshold slope of 90 mV/dec. The quantum dot devices were measured in a Heliox cryostat at a temperature of 0.5 K. Strong conductance oscillations were observed when sweeping the gate voltage (Fig. 4). These oscillations are due to the Coulomb blockade effect of electrons in the confined silicon quantum dot.<sup>5</sup> The charging energy, estimated to be 2 meV, is much larger than the thermal energy at 0.5 K, so the energy levels inside the silicon quantum dot become discretized. As a result, discrete peaks are shown in conductance as a function of gate voltage. As compared with the devices fabricated by conventional electron beam lithography, we did not observe any noticeable difference in the device behavior.<sup>4</sup> We are currently investigating the silicon ring devices, and the results will be discussed elsewhere.

Finally, we should point out that the pressure used in NIL is about three orders of magnitude smaller than the yield strength of silicon (which is  $\sim 3.2 \times 10^9$  Pa). Therefore,

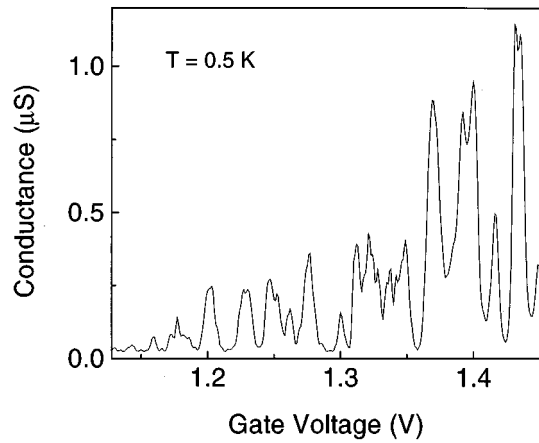


FIG. 4. Conductance as a function of gate voltage for quantum dot transistor measured at 0.5 K.

structural damage of silicon substrate during NIL is not expected.

In summary, we have fabricated the first semiconductor nanotransistors using NIL for the first time. The high pres-

sure and RIE process in NIL does not produce observable effects on the device characteristics. This investigation represents a step forward to make nanoimprint lithography a viable technique for the mass manufacturing of semiconductor devices.

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<sup>5</sup>See, for example, *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).