Wire-channel and wrap-around-gate metal–oxide–semiconductor field-effect transistors with a significant reduction of short channel effects

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Metal–oxide–semiconductor field-effect transistors (MOSFETs) with a wire-channel and wrap-around-gate (WW) structure were fabricated using electron beam lithography and reactive ion etching. The smallest devices have a 35 nm channel width, a 50 nm channel thickness, and a 70 nm channel length. Measurements showed that as the channel width of WW MOSFETs decreased from 75 to 35 nm short channel effects were significantly reduced: the subthreshold slope decreased from 356 to 80 mV/dec and the drain-induced barrier lowering decreased from 988 to 129 mV. Furthermore, the reduction of channel width increases the drive current per unit channel width. A multichannel WW MOSFET with a high current driving capability is discussed. © *1997 American Vacuum Society.* [S0734-211X(97)16806-8]

I. INTRODUCTION

When the size of conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) is reduced to the deep submicron regime, the transistors usually suffer severe short channel effects (SCEs). One of the effects is a large subthreshold slope, which leads to a large leakage current. Another effect is a large drain-induced barrier lowering (DIBL), which causes an undesirable threshold voltage shift as the drain voltage changes. Double-gate and silicon on insulator (SOI) DELTA MOSFETs have previously been proposed to suppress the SCEs.[1–3] In the double-gate structure, a top gate and a bottom gate sandwich a thin silicon layer, giving better gate control over the channel potential than a conventional MOSFET. The SOI DELTA structure is essentially a vertical version of the double-gate structure, where the silicon channel has a narrow wall shape with two gates at both sides of the wall. Using these structures, near long channel behavior has been achieved in a transistor of 0.15 μm channel length.[3]

However, to further reduce the SCEs, both the channel width and the channel thickness need to be reduced. This will allow the gate to wrap around the channel and control the channel potential from all four surfaces, which leads to an optimum structure of reducing SCEs—a wire-channel wrap-around-gate (WW) structure, shown in Fig. 1. This structure has been theoretically studied by Miyano *et al.*,[4] who suggested that a smaller channel cross section should yield better subthreshold characteristics. Recently, the work done by Auth and Plummer[5] also predicted that a WW structure can scale down the channel length 30% more than the double-gate structure. The advantage of the WW structure also can be easily understood by the three-dimensional (3D) Poisson equation:

$$\frac{\partial^2\Phi}{\partial x^2}=\frac{eN_A}{\epsilon_{\mathrm{Si}}}-\frac{\partial^2\Phi}{\partial y^2}-\frac{\partial^2\Phi}{\partial z^2}, \tag{1}$$

where Φ is the electron potential and N_A is the concentration of acceptor atoms inside the channel. Since SCEs can be reduced by increasing the height of the potential barrier between the source and the drain [Fig. 1(a)], which is equivalent to increasing $(\partial^2\Phi/\partial x^2)$, it is traditionally accomplished by increasing the channel doping concentration (N_A). In double-gate and SOI DELTA structures, SCEs are reduced by increasing either $-(\partial^2\Phi/\partial y^2)$ or $-(\partial^2\Phi/\partial z^2)$ but not both. However, in the WW structure, optimum control of SECs can be achieved by increasing both $-(\partial^2\Phi/\partial y^2)$ and $-(\partial^2\Phi/\partial z^2)$. In this article, we present an experimental study of WW MOSFETs. We have observed a significant reduction of SCEs as the channel width is narrowed. A subthreshold slope of 90 mV/dec has been achieved in a 70 nm channel length MOSFET with a 35 nm channel width and a 50 nm channel thickness. Moreover, a narrow channel width also increases the drive current per unit channel width.

II. DEVICE FABRICATION

The WW MOSFETs were fabricated on a separation by implanted oxygen (SIMOX) SOI wafer with an 85-nm-thick top silicon layer [Fig. 2(a)]. The first level electron beam lithography (EBL) and chlorine-based reactive ion etching (RIE) were used to define the wire channel, the source and the drain contact pads [Fig. 2(b)]. Then, a rounding-off oxide was grown to reduce the sharpness of the wire edges,[6] followed by boron channel implantation to reach a final channel doping of 5×10^{17} cm^{-3} [Fig. 2(c)]. The rounding-off oxide was removed by HF. The undercut due to the HF etching makes the silicon wire free standing, suspended between the source and the drain contact pads [Fig. 2(d)]. Then a 11-nm-thick gate oxide was grown and an undoped polysilicon gate of 226 nm thickness was deposited using low pressure chemical vapor deposition (LPCVD) [Fig. 2(e)]. Since the film deposited by LPCVD conforms to the sample topology, the polysilicon gate wraps around the channel. Next, the

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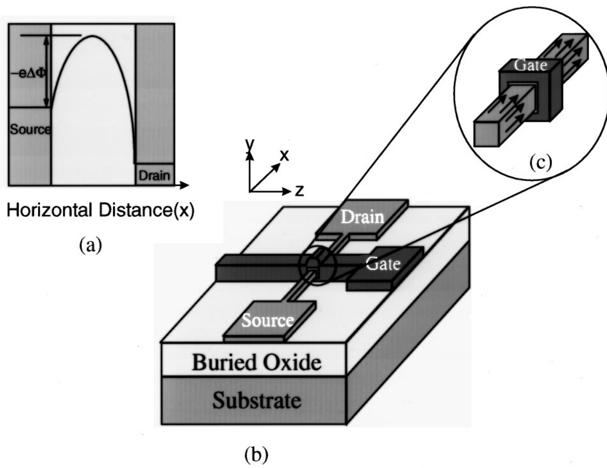

FIG. 1. WW MOSFET. (a) Electron potential profile between source and drain; (b) schematic of WW MOSFET; (c) in the WW structure, current flows along four surfaces of the channel.

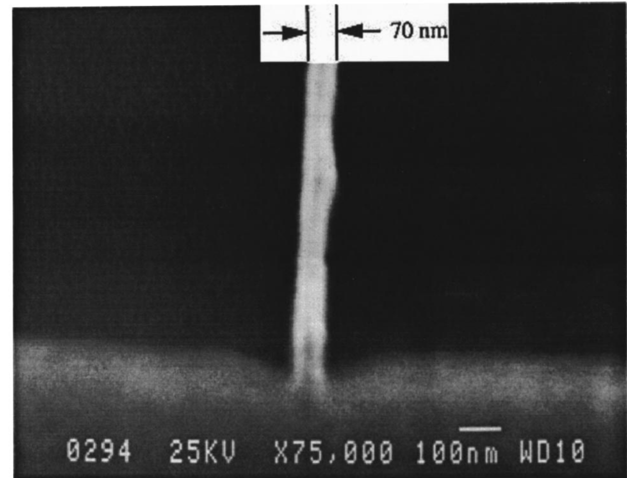

FIG. 3. SEM picture of a silicon wire channel fabricated by EBL (before oxidation).

second EBL and RIE were used to pattern the gate, followed by a self-aligned arsenic implantation of the source and the drain, and a 1000 °C rapid thermal annealing (RTA) process [Fig. 2(f)]. After contact metallization, all the devices were sintered in a hydrogen and nitrogen forming gas at 425 °C for 30 min. For fabrication simplicity, instead of varying the channel cross section, only the channel width was varied while the final channel thickness was fixed at 50 nm.

Figure 3 shows a scanning electron microscopy (SEM) picture of a silicon wire channel fabricated using EBL before oxidation. The wire width was 70 nm, but was reduced to 35 nm after the two oxidation processes.

The key parameters of the devices are as follows. The gate oxide is 11 nm on the top and bottom surfaces of the channel, and is estimated to be 14 nm at the two sidewalls; the channel thickness is 50 nm; the channel width varies from 35 to 75 nm, and the channel length varies from 70 to 730 nm.

III. DEVICE CHARACTERISTICS

Figure 4 shows the $I-V$ characteristics of a device with 35 nm channel width and 70 nm channel length. At 1.55 V drain bias, the subthreshold slope is only 90 mV/dec. The drain output conductance is also small for the 70 nm channel length. Considering the fact that the gate oxide of this device is rather thick (11 nm), the device behavior is very remarkable.

Figure 5 shows how the subthreshold slope and DIBL depend on the channel width. The subthreshold slope of 120 nm channel length devices decreases from 356 to 80 mV/dec

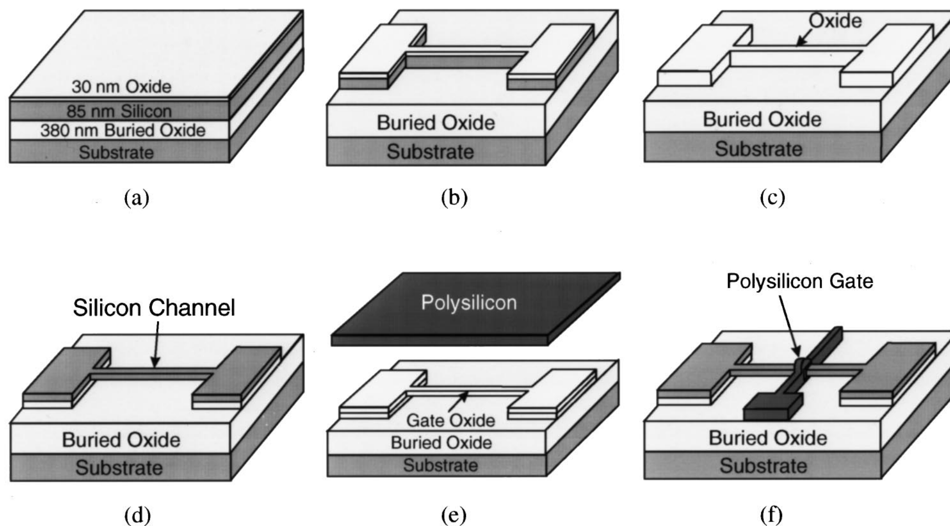

FIG. 2. WW MOSFET fabrication process: (a) starting SOI wafer; (b) channel definition; (c) rounding-off oxide growth and channel implantation; (d) removal of rounding-off oxide; (e) gate oxidation and polysilicon gate deposition; (f) gate definition and source/drain implantation.

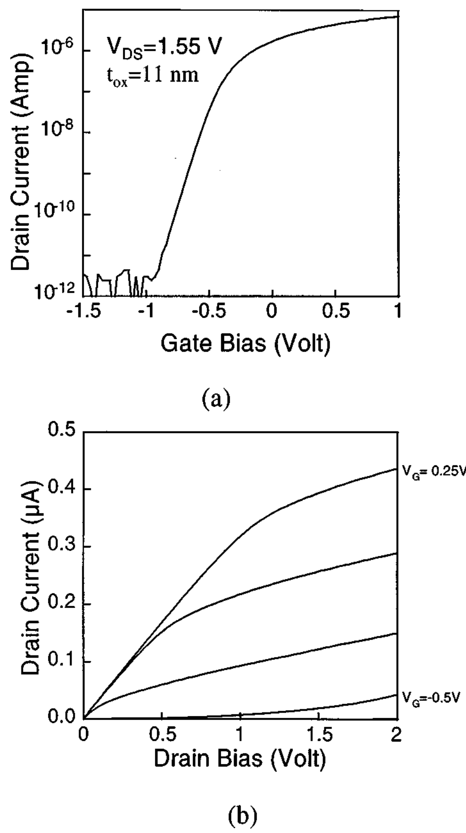

FIG. 4. WW MOSFET with 35 nm channel width and 70 nm channel length: (a) subthreshold characteristics; (b) drain current as a function of drain voltage with a gate bias step of 0.25 V.

when the channel width is reduced from 75 to 35 nm. The improvement is almost a factor of 5, implying that to achieve the same leakage current, the narrow channel MOSFET needs only one-fifth the gate switching voltage required for the wider device. A smaller gate switching voltage implies a smaller power supply and less power consumption. The DIBL is also dramatically reduced as the channel is narrowed. The DIBL is represented by the difference of the threshold voltage at drain biases of 0.05 and 1.55 V. At 75

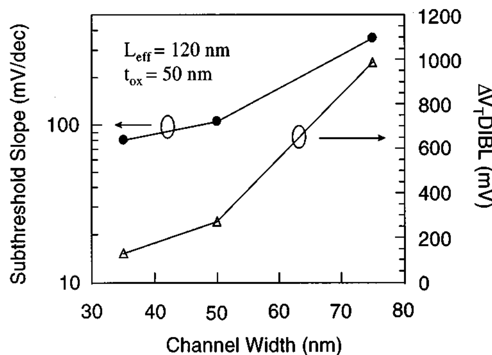

FIG. 5. Dependence of SCEs on channel width.

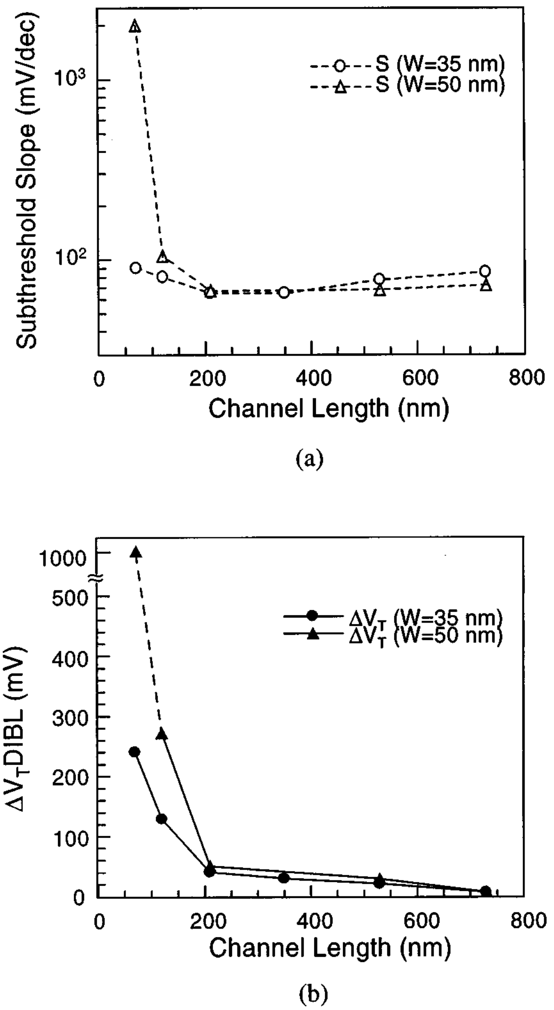

FIG. 6. Effects of channel width on the behavior of devices with different channel lengths: (a) subthreshold slope and (b) DIBL.

nm width, the DIBL is 988 mV. But at 35 nm, the DIBL is only 129 mV. The difference is more than sevenfold.

We have also studied how the channel width affects the behavior of MOSFETs with different channel lengths. Both Figs. 6(a) and 6(b) show that, when the channel length is longer than 200 nm, the effect of channel width is very small. However, when the channel length is less than 200 nm, the devices with 35 nm channel width have significantly smaller subthreshold slopes than those with 50 nm channel width [Fig. 6(a)]. At a 70 nm gate length, the device with a 50 nm channel width has a subthreshold slope of about 2000 mV/dec and can hardly be turned off. On the other hand, the device with a 35 nm channel width has a subthreshold slope of only 90 mV/dec. The DIBLs are also much smaller in the narrower devices than in the wider devices when the channel length is less than 200 nm [Fig. 6(b)]. At 70 nm channel length, for a 35-nm-wide device, the DIBL is 240 mV; for a 50-nm-wide device, the DIBL is almost 1000 mV.

Both Fig. 5 and 6 clearly show that in the WW structure SCEs can be significantly reduced by narrowing the channel

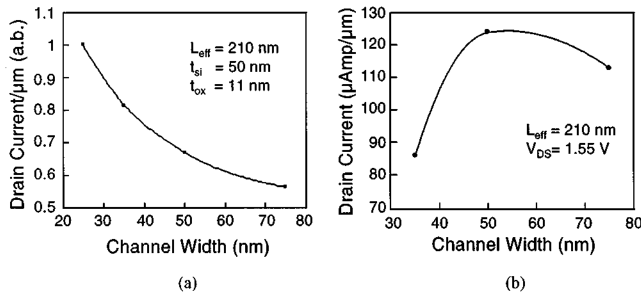

FIG. 7. Drive current per unit channel width as a function of channel width: (a) simulation and (b) experimental results.

width due to better gate control over the channel potential.

Another advantage of the WW structure is that it can increase the current drive per unit channel width. The reason is that in the WW structure current flows along four surfaces of the channel instead of only one as in a conventional MOSFET [Fig. 1(c)]. A simple derivation gives us

$$I_d = K_1 W + K_2 t_{\mathrm{Si}} \Rightarrow i_d \equiv \frac{I_d}{W} = K_1 + \frac{K_2 t_{\mathrm{Si}}}{W}, \tag{2}$$

where W is the channel width, t_{Si} is the channel thickness, and K_1 and K_2 are constants. Equation (2) shows that the current per unit width has a term that is inversely proportional to the channel width. The smaller the channel width, the larger the current per unit width. Simulation using DEVICE3D (from SILVACO International Inc.) shows the same result [Fig. 7(a)].

In our measurements, however, the increase of the drive current per unit width with the reduction of the channel width only occurs when the channel width decreases from 75 to 50 nm [Fig. 7(b)]. When the channel width is further reduced to 35 nm, the drive current per unit width decreases instead of increases. This discrepancy is due to the large source and drain series resistance at a very narrow channel width. The resistance can be reduced by reducing the spacing between the source and the drain contact pads.

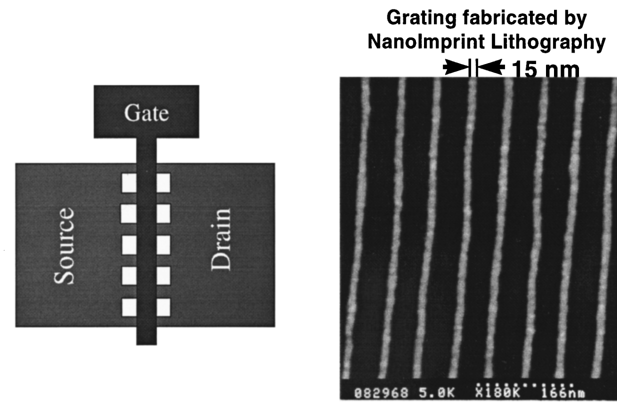

FIG. 8. Proposed multichannel WW MOSFET.

Moreover, in order to maintain the total current driving capability of a WW MOSFET, parallel channels should be used. To alleviate lithography constraints, this can be achieved using nanoimprint lithography, as shown in Fig. 8.[7]

IV. SUMMARY

We have fabricated a WW MOSFET 35 nm in width, 50 nm in thickness, and 70 nm in length. A significant reduction of the SCEs was observed by decreasing the channel width from 75 to 35 nm. The subthreshold slope decreased from 356 to 80 mV/dec and the DIBL decreased from 988 to 129 mV. The WW structure can give a high current drive per unit channel width, and the multichannel WW MOSFET is proposed for future high performance ULSI.

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