Improved organic thin-film transistor performance using novel self-assembled monolayers

M. McDowell and I. G. Hill[a)]
Dalhousie University, Department of Physics, Halifax, Nova Scotia, Canada

J. E. McDermott, S. L. Bernasek, and J. Schwartz
Princeton University, Department of Chemistry, Princeton, New Jersey

(Received 17 November 2005; accepted 3 January 2006; published online 14 February 2006)

Pentacene-based organic thin-film transistors have been fabricated using a phosphonate-linked anthracene self-assembled monolayer as a buffer between the silicon dioxide gate dielectric and the active pentacene channel region. Vast improvements in the subthreshold slope and threshold voltage are observed compared to control devices fabricated without the buffer. Both observations are consistent with a greatly reduced density of charge trapping states at the semiconductor-dielectric interface effected by introduction of the self-assembled monolayer. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2173711]

Organic thin-film transistors (OTFTs) are a promising alternative technology to amorphous silicon devices. Free from traditional high-temperature processing steps, they can be fabricated on a wide variety of low-cost flexible substrates, including polyethylene terephthalate and naphthalate.[1] The combination of low-temperature processing and flexible substrates may enable a large-scale low-cost continuous manufacturing process, resulting in a greatly reduced cost per unit area.

Pentacene OTFTs have performed very similarly to their amorphous silicon counterparts,[2–4] with carrier mobilities in the range of 1 $cm^2/V\,s$ and on-off ratios between 10^6 and 10^8. The major drawbacks of pentacene OTFTs, however, are their poor subthreshold performance and typically large positive threshold voltages. Large subthreshold slopes, on the order of about 5 V/decade, and threshold voltages of a few tens of volts, are typical of OTFTs having a SiO_2 dielectric thickness of 350 nm.[3] These shortcomings have been addressed by the use of an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) at the SiO_2/pentacene interface. This treatment has been shown to improve subthreshold slopes, with values of 0.6 and 1.6 V/decade reported for 200 (Ref. 2) and 350 nm (Ref. 4) dielectric thicknesses, respectively. These values are still far from the theoretical minimum of ≈58 meV/decade $[kT/q\ \ln(10)]$, which is independent of dielectric thickness in the trap-free limit. It is generally accepted that the improved performance observed is the result of the elimination of charge trapping states at the semiconductor/dielectric interface. It has recently been suggested that electron-trapping hydroxyl groups are the cause of both the poor subthreshold performance of polymer and molecular organic thin film transistors (TFTs) and the general absence of *n*-type conduction that has been observed in these devices.[5] The filled electron trap states prevent the Fermi level from moving within the semiconductor gap as the gate potential is changed. In the case of a *p*-type device with a large electron interfacial trap density, this resistance to Fermi level shifting results in a poor subthreshold slope, but does not directly influence the observed hole mobility.

Unfortunately, OTS SAMs are difficult to prepare, in part because OTS reacts violently with water and is unstable in air. Consequently, it is desirable to find a different treatment that gives a stable buffer that is easy to prepare and that results in even better performance than an OTS one. Hanson *et al.*,[6,7] have recently demonstrated a class of SAM, utilizing organophosphonates as the constituent molecules. These SAMs are easily prepared in air, and form well-ordered strongly bound films on oxide surfaces with molecular densities close to those found in single crystals. Organophosphonates were therefore chosen as a class of SAMs that may be suitable for treatment of OTFT gate oxides.

To eliminate trap states using a SAM, it might be desirable to provide a surface onto which the pentacene can be deposited that "looks" as much like a pentacene film as possible. It is also desirable to produce an organic surface with which the pentacene will interact only via van der Waals forces, and not by a stronger chemical interaction that may result in trapping states in the semiconductor gap. It is imperative that the organic SAM has a band gap that is larger than that of the pentacene itself, so that the SAM does not provide inherent trapping states. We chose a SAM presenting an anthracene monolayer surface for further pentacene deposition that is covalently attached to the gate dielectric through a phosphonate linkage. Anthracene and pentacene belong to the family of linear polycyclic aromatic hydrocarbons (see Fig. 1), and the pentacene/anthracene interaction is therefore likely to be similar to the pentacene/pentacene interaction. Furthermore, the highest occupied molecular orbital-lowest unoccupied molecular orbital (HOMO-LUMO) gap of anthracene is significantly larger than that of pentacene due to the much greater delocalization of the π and π^* systems in the larger pentacene molecule. It is therefore reasonable to expect that an anthracene SAM will not

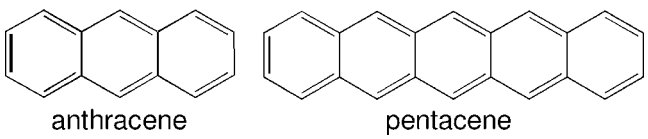

FIG. 1. Anthracene vs pentacene.

[a)]Electronic mail: ian.hill@dal.ca

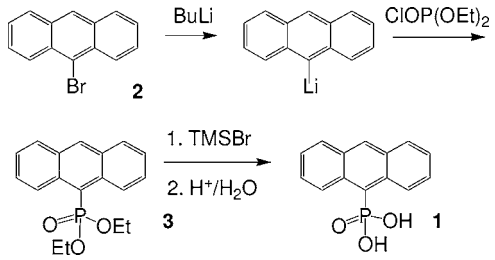

FIG. 2. Synthesis of 9-phosphonoanthracene, **1**.

contribute charge-trapping states within the pentacene HOMO-LUMO gap.

9-Phosphonoanthracene **(1)** was synthesized by metal-halogen exchange from 9-bromoanthracene **(2)** followed by phosphonation with diethyl chlorophosphate and subsequent ester hydrolysis (Fig. 2). 9-Bromoanthracene **(2**, 94%, 1.00 g, 3.90 mmol) was dissolved in 50 mL freshly distilled diethyl ether under argon at −78 °C Butyllithium (1.7 M, 4.59 mL, 7.80 mmol, 2 equiv.) was slowly injected through a rubber stopper via a glass syringe, and the resulting dark orange solution was allowed to stir for 15 min. Diethyl chlorophosphate (97%, 1.13 mL, 7.80 mmol, 2 equiv.) was then added, and the reaction mixture was allowed to stir for 2 h at −78 °C, and then 8 h at room temperature. The resulting yellow suspension was filtered to remove LiCl, and the solvent was evaporated at reduced pressure. The recovered solid was purified by chromatography on a silica column (20% ethyl acetate/hexane eluent) affording yellow 9-diethylphosphonoanthracene **(3**, 0.540 g, 1.71 mmol, 44%) For **3**, 1H NMR (CDCl3, 400 MHz): 9.39 (d) 2H; 8.62 (s) 1H; 8.02 (d) 2H; 7.62 (t) 2H; 7.50 (t) 2H; 4.26 (m) 2H; 4.04 (m) 2H; 1.28 (t) 6H. 9-Diethylphosphonoanthracene **(3**, 0.200 g, 0.636 mmol) was suspended in 10 mL dry methylene chloride under argon to which bromotrimethylsilane (0.247 mL, 1.90 mmol, 3 equiv.) was added. After stirring overnight, the solvent was evaporated, the solid was dissolved in 2 mL acetonitrile, and 5 mL 1% aqueous HCl was added. The acetonitrile was removed by rotary evaporation, yielding a precipitate of **1**. Addition of 10 mL 5% aqueous potassium hydroxide redissolved **1**. Filtration and reacidification precipitated yellow crystals of 9-phosphonoanthracene, which were collected on a filter and dried under a vacuum (0.135 g, 0.522 mmol, 82% yield). For **1**, 1H NMR (CDCl3, 400 MHz): 9.36 (d) 2H; 8.71 (s) 1H; 8.06 (d) 2H; 7.50 (m) 4H.

Transistors were fabricated on heavily doped Si wafers, which served as common gate electrodes for all devices. A thermal oxide layer, 100 nm thick, was used as the gate dielectric. The method used to prepare the SAMs has been reported elsewhere.[6] Si substrates were suspended in a 0.025 mM solution of **1** in dry THF and the solvent was allowed to evaporate from the reservoir to until the sample was no longer in contact with it. In this process, the phosphonic acid amphiphile is transferred to the substrate as the meniscus traverses its surface, forming a phosphonic acid SAM that is hydrogen bonded to the oxide surface. The coated substrates were then heated to 130 °C in a tube furnace for 48 h under N_2 to set the monolayer as a phosphonate. The treated Si substrates were next sonicated in 1:1 ethanol:toluene for 20 min, then rinsed successively with ethanol and milliQ® water to remove any residual multilayer. Finally, the samples were blown dry with dry N_2 and stored under nitrogen. This process was repeated in triplicate for each sample to fill in any pinholes that may remain following a single deposition cycle. The quality of the phosphonate SAM was evaluated by imaging with a Digital Instruments Dimension atomic force microscope (AFM) (Fig. 3). The film thickness was found to be approximately 9.5 Å by pinhole section analysis after one deposition, suggesting that the anthracene phosphonate molecules are held virtually perpendicular to the surface. Previous studies on alkyl- and aryl-terminated phosphonate SAMs have shown these pinhole-determined thicknesses to correlate well with those determined by x-ray reflectivity.[6] Following three depositions, no pinholes could be found.

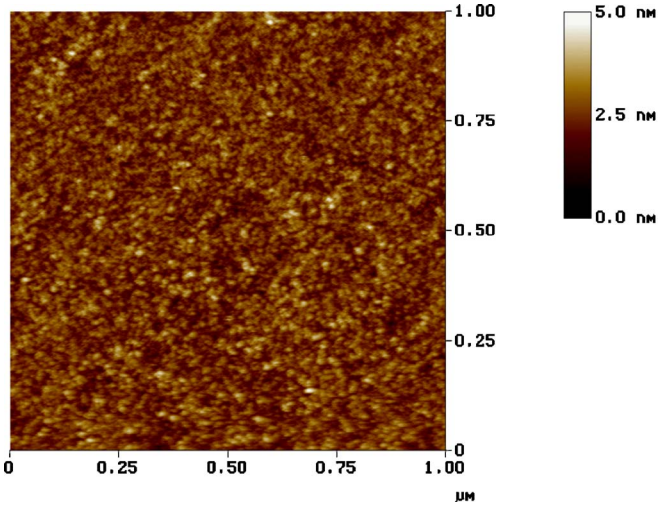

FIG. 3. AFM image (1 μm×1 μm) of a SAM of anthracene-9-phosphonate, prepared from **1** on SiO_2/silicon.

Pentacene crystals were purchased from America Organic Semiconductor, and were used as received, without further purification. 99.999% pure gold was used for the source-drain contacts. Each sample run consisted of two such substrates: One treated with the phosphonate SAM and one control. Prior to being loaded into the vacuum deposition system, SAM and control substrates were cleaned by the same procedure: Boiling for 3 minutes in trichloroethylene, soaking for 3 min in room-temperature acetone, boiling for 3 min in methanol, and blown dry using compressed air. Pentacene was deposited at 0.1–0.2 nm/s by sublimation from a molybdenum boat, with the substrate holder held at 70 °C, as previously determined to be optimum for pentacene deposition on untreated SiO_2 in our system. Gold was deposited from a tungsten wire basket filament at 0.2 nm/s with the sample nominally at room temperature. All depositions were performed in a bell jar evaporation system with a base pressure of $\sim 10^{-6}$ Torr.

Transistors were fabricated in the top-contact geometry, with gold source-drain contacts (50 nm) evaporated on top of the pentacene film (50 nm). Arrays of transistors were patterned by shadow masking of both the pentacene and gold layers. The channel widths of the transistors thus fabricated ranged from 500 to 1500 μm, while the channel lengths ranged from 25 to 250 μm. W/L ratios therefore ranged from 2 to 60. The saturation transfer characteristics of these devices were measured using two Keithley 237 source-measure units with a current resolution of 10 fA. Source electrodes were held at ground potential. Drain electrodes were set at −25 V, with respect to the source (V_{DS}). Gate

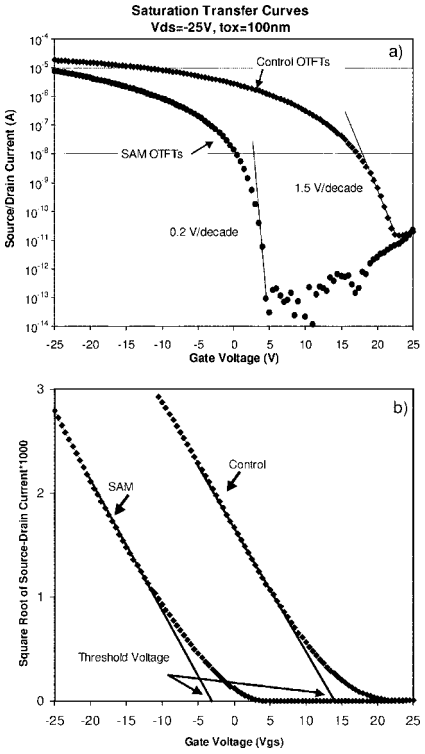

FIG. 4. Saturation transfer curves of TFTs with subthreshold slope indicated. Top panel is a semilog plot, illustrating the subthreshold characteristics of the devices. Bottom panel illustrates the threshold voltage shift observed by plotting the square root of the source-drain current.

potentials (V_{GS}) were swept from +25 V (off) to −25 V (on). The data were analyzed by plotting the square root of the drain current (I_D) as a function of gate voltage. The slope of a fit to the linear portion of this plot, above threshold, yields the field effect hole mobility, while the gate voltage intercept of the fit line determines the threshold voltage. The (inverse) subthreshold slope is determined by a linear fit to the log (I_D) just as the current begins to increase. On-off ratios were determined using the minimum observed drain current in the off region and the maximum current observed in the on region. On the order of ten pairs of control and SAM substrates were studied, each containing fifty transistors. Typical saturation transfer curves for control and SAM devices are presented in Fig. 4.

Hole mobilities of the transistors ranged between 0.3 and 0.8 $cm^2/V\,s$ for both control and SAM treated samples. No statistically significant differences in mobilities were evident between the SAM and control devices. These mobilities are typical for similar devices reported in the literature, but are lower than the best reported mobilities for pentacene devices utilizing a polyvinylphenol-based polymeric dielectric.[8] Subthreshold slopes were consistently 0.2–0.3 V/decade for SAM-modified devices versus 1.5–1.7 V/decade for control devices. Threshold voltages for control devices were typically +13 V, with a strong dependence on channel length, which will be reported in a future manuscript. SAM devices, in contrast, consistently exhibited a threshold voltage of −4.5 V, with a scatter on the order of 100 meV. Note, in Fig. 4, that the near-zero threshold voltage also results in an improved on-off ratio (as high as 10^8), as the off current is approximately two orders of magnitude smaller for the SAM devices than for the control devices, due to lower dielectric leakage currents at lower gate voltages.

The significant improvements in subthreshold slope and threshold voltage measured can be attributed to a decreased charge trap density at the pentacene/dielectric interface. We estimated the areal density of interfacial traps in the control devices using two procedures. The first assumes that the difference in threshold voltage of the SAM and control devices is due to trapped charge on one side of a capacitor, of a capacitance/area equal to C_{ox}. The second estimates an upper limit on the same quantity using the value of the subthreshold slope:[9]

$$\text{Method (1) } N_{\text{trap}} \approx \frac{C_{\text{ox}} \times \Delta V_{\text{th}}}{q},$$

$$\text{Method (2) } N_{\text{trap}}^{\max} \approx \left[\frac{qS\log(e)}{kT} - 1\right]\frac{C_{\text{ox}}}{q},$$

where q is the electronic charge, S is the (reciprocal) subthreshold slope, in V/decade, k is Boltzmann's constant, and C_{ox} is the capacitance/area of the gate dielectric. Using Method 1, we estimate the interfacial trap density in the control devices to be $3.7\times10^{12}\ cm^{-2}$. Using Method 2, we estimate an upper limit of $5.4\times10^{12}\ cm^{-2}$. The consistency of the two estimates strengthens the arguments as to the origin of the threshold voltage shifts and change in subthreshold slopes observed. The subthreshold slope of the SAM devices results in an estimated interfacial trap density of $5.3\times10^{11}\ cm^{-2}$, indicating the degree to which the trap states have been eliminated by the SAM.

In conclusion, we have demonstrated that OTFTs fabricated using oxide gate dielectrics modified with phosphonate-linked SAMs have greatly improved electrical properties compared to those fabricated using bare oxides. Furthermore, these SAMs are far more stable and more easily prepared than the more commonly used trichlorosilane-derived films, and exhibit better electrical characteristics. When prepared on 100 nm thermal SiO_2, SAM/pentacene OTFTs have a near-zero threshold voltage, and a subthreshold slope of 0.2 V/decade, which is only 3.5 times the minimum value allowed by thermodynamics.

This work was supported by the Natural Sciences and Engineering Research Council of Canada (I.H.), the Canada Foundation for Innovation (I.H.), the National Science Foundation (J.S. and S.L.B.), the National Defense Science and Engineering Graduate Fellowship program (J.M.), and CRG Chemical of San Diego, California (I.H. and J.S.).

[1] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, Appl. Phys. Lett. **80**, 1088 (2002).
[2] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Electron Device Lett. **18**, 606 (1997).
[3] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, IEEE Electron Device Lett. **18**, 87 (1997).
[4] M. Shtein, J. Mapel, J. B. Benziger, and S. R. Forrest, Appl. Phys. Lett. **81**, 268 (2002).
[5] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[6] E. L. Hanson, J. Schwartz, B. Nickel, N. Koch, and M. Fatih Danisman, J. Am. Chem. Soc. **125**, 16074 (2003).
[7] E. L. Hanson, J. Guo, N. Koch, J. Schwartz, and S. L. Bernasek, J. Am. Chem. Soc. **127**, 10058 (2005).
[8] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, J. Appl. Phys. **92**, 5259 (2002).
[9] A. Rolland, J. Richard, J.-P. Kleider, and D. Mencaraglia, J. Electrochem. Soc. **140**, 3679 (1993).