Organophosphonate Self-Assembled Monolayers for Gate Dielectric Surface Modification of Pentacene-Based Organic Thin-Film Transistors: A Comparative Study[†]

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Organic thin-film transistors using pentacene as the semiconductor were fabricated on silicon. A series of phosphonate-based self-assembled monolayers (SAMs) was used as a buffer between the silicon dioxide gate dielectric and the active pentacene channel region. Octadecylphosphonate, (quarterthiophene)phosphonate, and (9-anthracene)phosphonate SAMs were examined. Significant improvements in the sub-threshold slope and threshold voltage were observed for each SAM treatment as compared to control devices fabricated without the buffer. These improvements were related to structural motif relationships between the pentacene semiconductor and the SAM constituents. Measured transistor properties were consistent with a reduction in density of charge trapping states at the semiconductor−dielectric interface that was effected by introduction of the self-assembled monolayer.

Introduction

Interest in organic electronic materials derives in part from their low processing costs and the ability to fabricate devices with them on flexible substrates, which may give organics significant advantages over traditional inorganic semiconductor materials. Organic thin-film transistors (OTFTs) first received attention in the 1980s[1] and are of particular interest, given their widespread possible application to switching, amplification, oscillation, signal modulation, or voltage regulation in display backplanes or large integrated circuits.[2]

OTFTs can be fabricated in either the top or the bottom contact geometry, using patterned metal or heavily doped silicon gate electrodes. In laboratory experiments, a heavily doped silicon wafer is often used as a common gate electrode for an entire array of OTFTs. A thin layer of gate dielectric SiO_2 is grown on top of this gate, which serves to insulate the gate from the rest of the transistor.[3] Pentacene is commonly used as the semiconductor in these devices; pentacene-based OTFTs have carrier mobilities in the range of 1 cm^2/V s and on−off ratios between 10^6 and 10^8,[4,5] which may rival the performance of amorphous silicon transistors. There are, however, major drawbacks of pentacene OTFTs, including poor sub-threshold performance and large positive threshold voltages: sub-threshold slopes on the order of about 5 V/decade and threshold voltages of tens of volts are typical for OTFTs using a 350 nm thick SiO_2 dielectric.

Most OTFT devices exhibit hole transport (*p*-type) but not electron transport (*n*-type) behavior. The lack of ambipolar transport is interesting because these materials are not extrinsic semiconductors; they do not require an external dopant, so they should be able to transport electrons as effectively as holes. It has been proposed that surface hydroxyl (OH) groups at the SiO_2 gate dielectric−organic semiconductor interface give rise to electron traps, which prevent *n*-type transport.[6] It may be that these traps result from localized surface dipoles of these OH groups, which are dilute on the SiO_2 surface, and which in turn induce localization effects in the organic semiconductor. Perhaps the organic semiconductors transport holes more effectively than electrons when these OH groups are present because holes are not as susceptible to those specific trapping states as are electrons.[7] Electron trapping states can, however, lead to a degraded performance in standard *p*-type devices, too, so any scheme to improve the performance of either *n*- or *p*-type OTFTs should involve OH group passivation or removal.[7,8]

A powerful technique for the modification of metal or metal oxide surfaces uses self-assembled monolayers (SAMs). SAMs are attractive candidates to treat gate dielectrics in organic electronic devices: they can accommodate a diversity of film constituent molecules, and they thus provide a degree of film property tunability. SAMs can enhance wetting of the (hydrophilic) gate dielectric by an organic semiconductor by presenting a hydrophobic surface on the substrate. Finally, SAMs can be easily fabricated on a variety of substrates by the choice of film constituent head group according to the chemical reactivity requirements of the substrate surface.

In crystalline pentacene, the molecules adopt a herringbone structure in which C−H bonds of one molecule interact with the π-system of a neighbor.[9] Pentacene molecules vapor deposited onto a SiO_2 substrate stand up lengthwise on the surface to maximize this herringbone interaction; because pentacene wetting of the SiO_2 surface is poor, they do not lie down on it. A better surface treatment might be one that not only eliminates surface OH groups but also presents an ordered, wettable surface onto which the pentacene molecules can be deposited, also with some order. Common now in the fabrication of laboratory pentacene-based OTFTs is to bond an interfacial coating derived from octadecyltrichlorosilane (OTS) onto the SiO_2 dielectric prior to depositing the pentacene semiconductor. Alkylsiloxane film formation consumes surface OH groups of

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the SiO_2, but siloxane films often involve extensive cross-linking, and they are typically thick, not surface conforming, and have disordered alkyl chains. The silanized SiO_2 surface is, though, better wet by pentacene following OTS treatment than is untreated SiO_2,[5] and OTFTs using silanization show improved sub-threshold slopes (0.6 and 1.6 V/decade for 200 and 350 nm SiO_2 dielectric thicknesses, respectively) as compared to devices based on untreated SiO_2.[4,10] These values are, however, still far from the theoretical minimum of about 58 mV/decade.[11]

SAMs based on organophosphonates are significantly more durable than siloxane films.[12,13] They are, therefore, perhaps more applicable to real world situations. Unlike siloxane films, phosphonate SAMs are surface conforming and well-ordered, and they can be systematically varied with regard to structure, making possible their application as a template to direct further pentacene growth. We have therefore taken a surface chemistry design approach to transistor function optimization that is based on gate dielectric surface treatment using SAMs of organophosphonates; we have previously reported on one member of this series.[14]

Phosphonate SAM formation involves two steps: first, a SAM of the phosphonic acid is adsorbed by the oxide surface, and it is then converted to the SAM of the phosphonate by heating. In contrast to silanization, where only surface OH groups react directly with film forming constituents, both surface OH and bridging surface oxide groups are activated by this process. A simple procedure,[15,16] dubbed the T-BAG, enables phosphonate SAM formation on a substrate under ambient conditions. Phosphonate SAMs adhere strongly to the substrate surface[17,18] and are ordered, homogeneous,[15] and versatile for subsequent chemical modification.[19,20] They have molecular densities close to those found in single crystals of the film constituents,[15,19] are resistant to removal by moisture and oxidation,[13] and are stable in electronically active environments.[14,16,21] The T-BAG method has been used successfully for a wide variety of oxide-terminated substrates and phosphonic acid structural motifs,[14,16,18] so virtually any phosphonic acid may be deposited onto any gate dielectric oxide material.

Pentacene/bare SiO_2/Si transistors were fabricated (as a control) in top-contact geometry and were evaluated for performance with respect to four transistor characteristics: charge carrier mobility, on/off ratio, sub-threshold slope, and threshold voltage. Optimization of transistor performance was accomplished as follows: (1) an aliphatic SAM of octadecylphosphonate (**1**) was grown on the SiO_2 gate dielectric to improve general surface wetting by the pentacene and to remove surface OHs; (2) a SAM of (quarterthiophene)phosphonate (**2**) was next used, which is aromatic group-terminated but does not closely resemble pentacene (and also removes surface OHs); and (3) an acene group-terminated SAM of (9-anthracene)phosphonate (**3**) was then used, whose structure does closely resemble pentacene so that it might serve as nucleation sites for ordered pentacene crystal deposition (and also eliminates surface OHs).

Experimental Procedures

General Considerations for Transistor Fabrication. Pentacene TFTs were fabricated either on SAM-treated or bare (control) SiO_2 substrates. All used heavily doped Si with a 100 nm thermally grown SiO_2 layer. The dielectric thickness was chosen as a compromise between a thicker one that would reduce electrical shorts through it and a thinner one that would yield reduced operating voltages. All substrates were subjected to the same cleaning procedure: 3 min in boiling trichloroethylene (TCE), 3 min in acetone, 3 min in boiling methanol, and blow dry with compressed air. For each pentacene deposition run, one SAM-treated sample and one control sample were placed side-by-side in a vacuum deposition system (base pressure 5×10^{-6} Torr) so that deposition conditions were identical for the SAM control pair. Pentacene was deposited through a shadow mask to a thickness of 500 Å, at ≈1 Å/s, with substrates heated to approximately 60 °C. Patterning of the pentacene layer was done to reduce leakage currents between adjacent transistors. Gold source and drain electrodes were deposited through a shadow mask to a thickness of 500 Å at approximately 1 Å/s, with the substrate at (nominally) room temperature. Arrays of transistors were fabricated with channel widths ranging from 0.5 to 1.5 mm and channel lengths ranging from 25 to 250 μm, allowing study of transistors with a range of W/L ratios, as shown in the overlaid shadow mask outlines previously described.[14] In general, between 100 and 200 transistors were tested for each type of SAM and for the controls.

SAMs of Octadecylphosphonate (1; ODP) on SiO_2/Si. These were formed by the T-BAG method,[15] in which SiO_2/Si substrates were suspended in a solution of 0.050 mM octadecylphosphonic acid in tetrahydrofuran (THF). SAMs were set by heating at 120 °C for 36 h. SAM film quality was evaluated by measuring the water wetting contact angle ($\Theta = 94°$), AFM (no gaps or multilayer formation), RAIRS ($\nu_{CHasymm} = 2915$ cm^{-1} and $\nu_{CHsym} = 2850$ cm^{-1}), and XPS (C1s = 285.6 eV and P2s = 191.8 eV).[15]

SAMs of (Quarterthiophene)phosphonate (2; 4TP) on SiO_2/Si. These were formed similarly from a solution of (quarterthiophene)phosphonic acid in THF (0.025 mM). The film of the phosphonic acid was converted to a covalently bound phosphonate SAM by heating at 140 °C for 48 h under argon; an argon atmosphere is necessary to prevent oxidation of the quarterthiophene moieties. Characterization of this SAM has been described.[22]

SAMs of (9-Anthracene)phosphonate (3; AP) on SiO_2/Si. These were formed similarly from a 2.5 μM solution of (9-phosphono)anthracene in THF. Optimal concentrations for (9-phosphono)anthracene deposition are 10−100 times lower than for ODPA because of its low solubility in THF and the need to avoid micelle formation. After baking the phosphonic acid-treated substrate at 130 °C for 36 h (under argon to prevent dephosphorylation), a residual multilayer was removed either by solvent rinsing or using a CO_2 snow gun. The SAM film was evaluated by AFM (no gaps or multilayers after three T-BAG procedures; film thickness, by section analysis, 9.5 Å), RAIRS ($\nu_{PO} \approx 1100$ cm^{-1}; no peak for free phosphonic acid), and XPS (P2s = 193 eV).

Results and Discussion

Octadecylsiloxane films have been well-studied for OTFT dielectric surface treatment, and so a SAM of octadecylphosphonate (**1**; ODP) was prepared for direct comparison; it provides a baseline substrate for hydrophobic SAM treatment of SiO_2 without imparting any specific sites for interaction with superdeposited pentacene. In contrast to the siloxane film, SAMs of **1** are surface conforming on SiO_2/Si as determined by AFM.[15] Quartz crystal microgravimetry (QCM) measured surface loadings of **1** to be 0.9 nmol/cm^2 on SiO_2/Si, which translates to a molecular footprint of 18.5 Å^2.[15] This density approaches the packing of crystalline polyethylene[23] and suggests that individual molecules of **1** are tightly packed in the SAM; IR analysis indicates that alkyl chains are well-ordered.[15,24]

SAMs of α-(quarterthiophene)phosphonate (**2**, 4TP) on indium-tin oxide had been studied in our group as anode

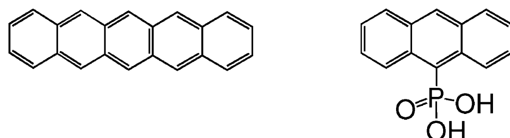

Figure 1. Pentacene (left) and (9-phosphono)anthracene (right).

treatments to improve the performance of organic light emitting diodes (OLEDs).[16,21] The 4TP SAM is also tightly packed (loading of **2** by QCM is 0.66 nmol/cm^2), with a molecular footprint of about 25 Å^2, giving a film density approaching the density of crystalline quarterthiophene;[25] this SAM has been structurally well-characterized.[15] It presents a surface in which thiophene C−H bonds are held nearly perpendicular to the substrate surface; by interactions of these C−H bonds with the π-system of vapor deposited pentacene molecules, the SAM might influence pentacene crystal growth on the substrate.

Our third dielectric surface treatment involved growing pentacene on a SAM of (9-anthracene)phosphonate (**3**); the surface of this SAM resembles a continuous anthracene film. The anthracene compound was chosen for several reasons: (1) the SAM constituents should have a band gap larger than that of the pentacene itself, so that the SAM would not provide inherent trapping states; (2) the SAM and pentacene should have only C−H bond−π-system interactions and not stronger bonding ones that could, themselves, create trapping states in the semiconductor gap; (3) the SAM should present an acene monolayer surface to affect further pentacene deposition; and (4) the SAM constituents should be soluble in media appropriate for ordered monolayer growth. Anthracene and pentacene are structurally related acenes (Figure 1), which might enhance crystalline grain formation in the pentacene overlayer. Furthermore, the highest occupied molecular orbital−lowest unoccupied molecular orbital (HOMO−LUMO gap) of anthracene (3.3 eV) is significantly larger than that of pentacene (1.86 eV) due to the greater delocalization of the π- and π*-systems in the larger pentacene molecule.[26] It was therefore reasonable to expect that an anthracene SAM would not contribute charge-trapping states at energies within the pentacene HOMO−LUMO gap and would present appreciable barriers to both electrons and holes if the pentacene gap was nested within that of the SAM. SAMs of **3** are tightly packed (loading of **3** by QCM is 0.33 nmol/cm^2) with a molecular footprint of 49 Å^2, suggesting a π-stacking morphology of anthracenyl units. SAMs of **3** are surface conforming on SiO_2/Si as determined by AFM, with a film thickness of 9.5 Å, consistent with individual molecules of **3** held normal to the surface.

Hole mobilities of the transistors fabricated using **1**, **2**, **3**, or controls all ranged from 0.3 to 0.8 cm^2/V s. No statistically significant differences in mobilities were evident between SAM and control devices (with no SiO_2/Si surface treatment). These mobilities are typical for similar devices reported in the literature.[27] The pentacene deposition conditions employed (1 Å/s at 60 °C substrate temperature) are optimal for use on bare SiO_2 but not necessarily so for the various SAM samples. Optimizing deposition conditions for the SAM-treated samples might lead to better performance from these transistors, but such optimization was beyond the scope of this study. Nonetheless, improvements in transistor performance were measured for all SAM devices as compared to control ones. For example, uniformity in threshold voltage (V_{Th}) among numerous devices is essential for utilization of transistors in large arrays such as those used to control display pixels; for *p*-channel devices such as these, it is often advantageous for there to be a slightly negative threshold voltage so that the current through the device is nearly zero with a zero gate voltage. An additional factor is the total voltage swing/power required to turn the device on or off, which should be small.

ODP (**1**)-treated devices demonstrated an improvement in threshold voltage uniformity (4 V < V_{Th} < 10 V) versus control devices (−5 V < V_{Th} < 15 V), as well as a decrease in the average threshold voltage (Figure 2A, right). Sub-threshold slopes of 1.5 V/decade were common for the control pentacene on bare silicon dioxide gate dielectric devices, while the ODP-treated gate dielectric transistors demonstrated sub-threshold slopes of 1.1 V/decade (Figure 2A, left).

Transistors fabricated using 4TP (**2**) SAMs on the gate dielectric were tested similarly to ODP-treated transistors, and two striking improvements versus the control were noted. Transistors prepared using **2** had a threshold voltage of −5 V with a range of ±1 V (Figure 2B, right), which is greatly reduced as compared to the control sample. There was also a clear improvement in the sub-threshold slope for 4TP-treated samples as compared to the controls. The 4TP transistors were found uniformly to have a slope of 0.5 V/decade (Figure 2B, left).

Transistors fabricated using AP (**3**) SAMs showed even better performance than those using **2**. AP SAM devices consistently had a threshold voltage of −4.5 V, with scatter on the order of only 100 mV (Figure 2C, right). This small threshold voltage was accompanied by an improved on−off ratio (as high as 10^8); the off current was approximately 2 orders of magnitude smaller for the SAM **3** devices than for the control devices, which is attributed to lower dielectric leakage currents at lower gate voltages. Sub-threshold slopes were consistently 0.2 V/decade for AP SAM-modified devices (Figure 2C, left); these sub-threshold slopes are only about 3 times the minimum value calculated for room temperature.[11] Sub-threshold slopes were about one-third of those reported for octadecyltrichlorosiloxane-treated devices; indeed, sub-threshold slopes for these AP SAM transistors are the lowest values reported to date for this class of OTFT.

The significant improvements in sub-threshold slope and threshold voltage measured for phosphonate-based SAM treatments can be attributed to a decreased charge trap density at the pentacene−dielectric interface. Interfacial trap density for devices using **3** can be estimated from the maximum observed sub-threshold slope[28] and were 0.5−1.6 × 10^{12} cm^{-2}. This value compares favorably with that for transistors using **1** (3.8−4.5 × 10^{12} cm^{-2}), **2** (1.6−3.0 × 10^{12} cm^{-2}), or the control devices (5.2−6.7 × 10^{12} cm^{-2}). All transistor performance data are summarized in Table 1.

To further evaluate the performance of transistors using **3**, ultraviolet photoelectron spectroscopy (UPS) was used to probe valence energy levels at the surface and determine the actual energy level alignment of SAM constituents and pentacene within these devices.[29] This alignment might deviate substantially from that estimated based solely on HOMO−LUMO gap measurements made for pure anthracene and pentacene. To duplicate as closely as possible the OTFT fabrication conditions,[14] heavily doped (*n*-type ≈ 0.001 cm) Si(100) wafers were used as substrates for this experiment. The OTFTs utilized a 1000 Å thermal SiO_2 layer as a gate dielectric, which is unsuitable for UPS studies due to charging effects from such a thick oxide. Instead, an ultrathin layer of approximately 7 Å was grown on the substrates by oxide stripping with HF followed by reoxidation using HNO_3, as reported elsewhere.[30] The SAMs of (9-anthracene)phosphonate were formed on these substrates using the same procedure as was used for the

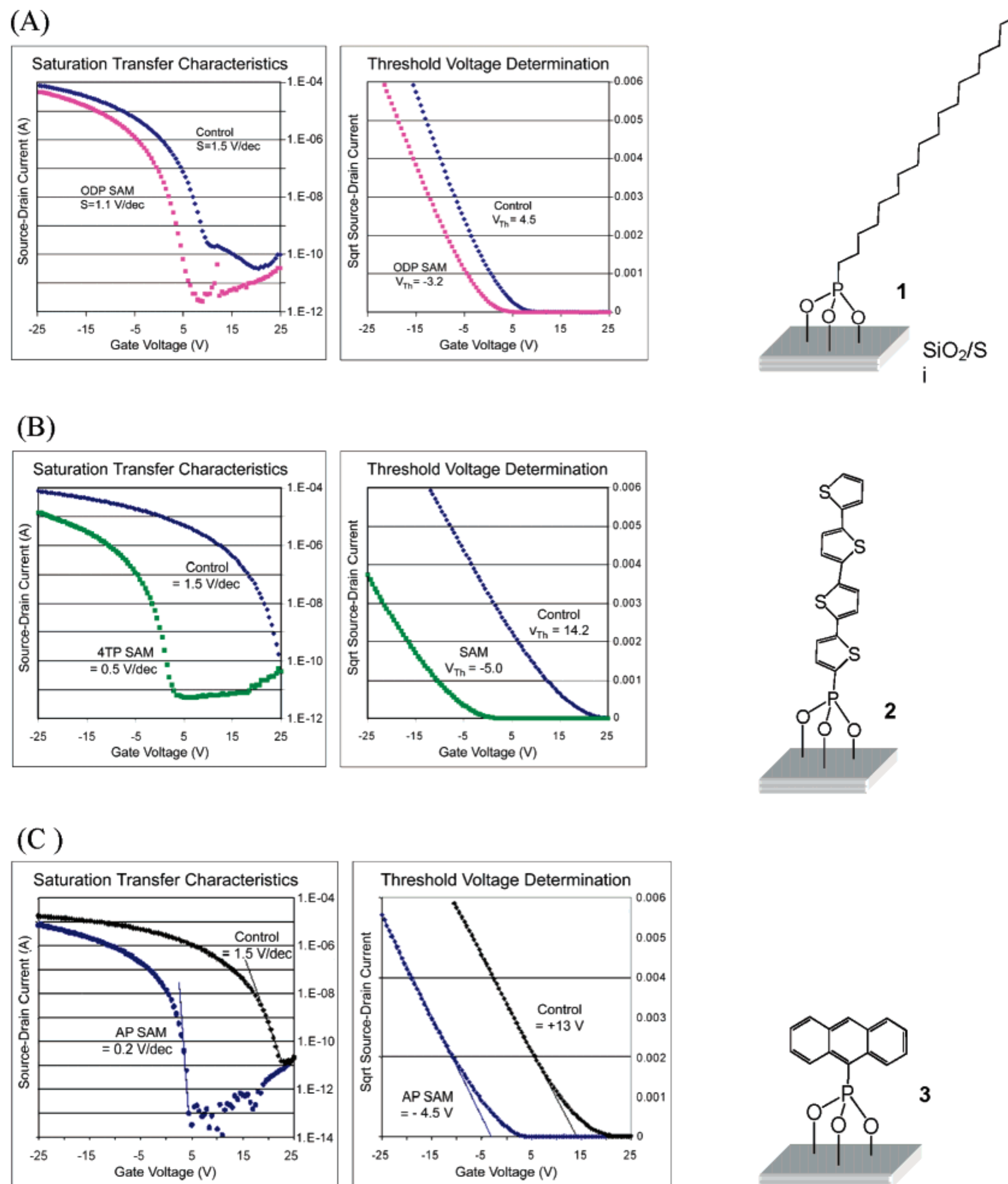

Figure 2. Sub-threshold (left) and threshold performance (right) of SAM-treated and control devices: (A) octadecylphosphonate (**1**); (B) (quarterthiophene)phosphonate (**2**); and (C) (anthracene)phosphonate (**3**).

TABLE 1: Comparative Transistor Performance Data

dielectric surface treatment	threshold range (V)	sub-threshold slope (V/decade)	charge trap density ($\times 10^{12}$ cm^2)
none (control)	0 ± 10	1.5−1.9	5.2−6.7
octadecylphosphonate, **1**	−5 ± 1	1.1−1.3	3.8−4.5
(quarterthiophene)phosphonate, **2**	−5 ± 1	0.5−0.9	1.6−3.0
(9-anthracene)phosphonate, **3**	−6 ± 1	0.2−0.5	0.5−1.6

functional transistors.[15] Pentacene was deposited incrementally on top of the SAMs at 0.1 Å/s.

UPS spectra were collected from the bare SiO_2 control samples, SAM coated samples, and at pentacene overlayer total thicknesses of 2, 4, 8, 16, 32, and 64 Å. The UPS spectrum of a multilayer of (9-phosphono)anthracene was recorded, and the ionization energy (IE), defined by the low binding energy edge of the UPS HOMO feature, was determined to be 6.1 ± 0.1 eV.[31] UPS spectra for the bare **3** and incrementally deposited pentacene were also measured. The evolution of the onset of photoemission (vacuum level) as a function of pentacene thickness is shown in the left panel of Figure 3, while the evolution of the density of states in the vicinity of the pentacene HOMO is shown in the right panel. The pentacene HOMO and other low binding energy states are clearly visible, even at a nominal coverage of 2 Å. As the monolayer is completed, the peak narrows, and its position remains constant with increasing overlayer thickness. The IE of the pentacene film is 5.0 ± 0.1 eV, in agreement with previous reports.[32,33]

The alignment of energy levels in the four regions of the sample, Si, SiO_2, SAM, and pentacene, was then calculated (Figure 4).[31] To estimate the LUMO offset between pentacene and SAM, care must be exercised. Traditionally, optical absorption HOMO−LUMO gaps have been used to estimate the position of the electron transport LUMO level. The optical gap is smaller than the transport gap by an amount equal to the exciton binding energy, which can be large in these materials.[29] Adiabatic energy gaps were used to ensure consistency in the

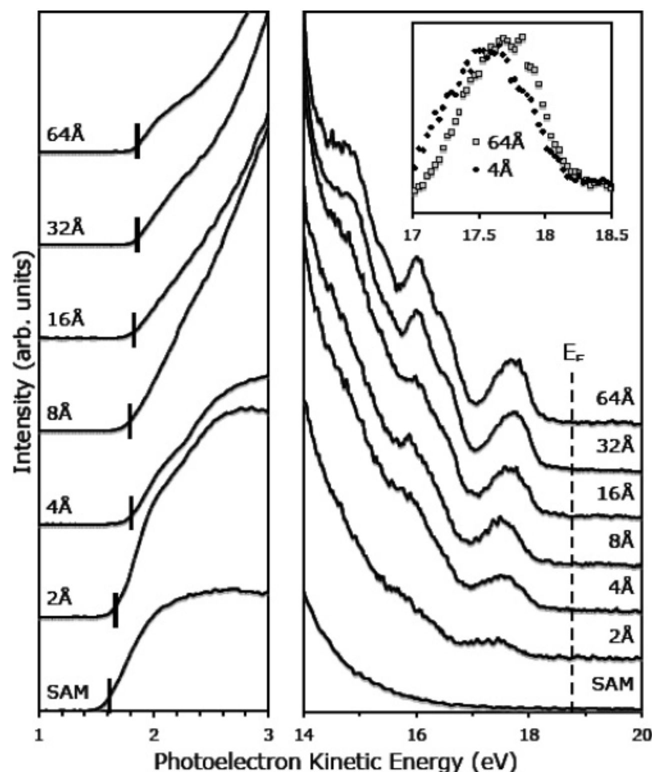

Figure 3. Evolution of the valence density of states and the onset of photoemission for incremental deposition of pentacene on SAM **3**.

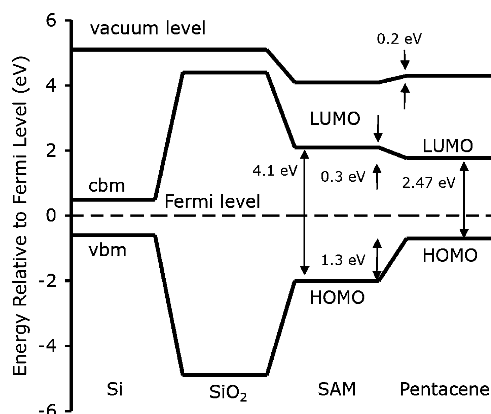

Figure 4. Frontier energy level alignment of the Si substrate, SiO_2 dielectric, SAM of **3**, and pentacene overlayer.

estimated LUMO positions of both molecules.[34] A pentacene transport gap of 2.47 eV and a (9-phosphono)anthracene transport gap of 4.1 eV were used to construct Figure 4.[29,34]

Conclusion

In contrast to the well-known strategy of using multilayered silanization to coat gate dielectrics in OTFTs, we find that the surface chemical and physical properties of these dielectrics can be manipulated systematically using ordered, self-assembled monolayers of organophosphonates. Fabrication using SAMs of simple, straight aliphatic chain octadecylphosphonate gave devices that were superior to untreated control devices and were comparable to devices using octadecylsilane derivatives. The structural tunability of phosphonate SAMs through choice of molecular constituent allowed for the design, synthesis, deposition, and characterization of a new (anthracene)phosphonate self-assembled monolayer-based transistor. This device showed dramatic improvement over others using octadecylsilane, other phoshonates, or controls and also demonstrated the best transistor characteristics, to our knowledge, to date, for a pentacene on a silicon/silicon dioxide transistor. These devices had substantially reduced trap states, on/off ratios of 10^8, subthreshold slopes of 0.2 V/decade (only 3 times the calculated minimum), and substantially uniform threshold voltages of −4.5 V across a large number of devices. It is possible that, with the use of thinner gate dielectrics and by the optimization of pentacene deposition conditions, even more substantial improvements in OTFT device behavior can be realized using phosphonate SAMs.

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