reconstructed using the disparity of the first matched point found to its left.

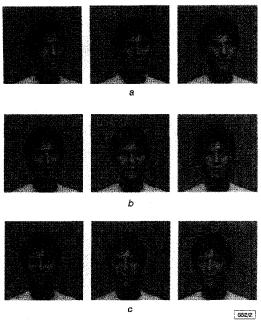


Fig. 2 MAN intermediate views for $\alpha = 0.0, 0.15, 0.25; 0.35, 0.5, 0.65;$ and 0.75, 0.85, 1.0

 $a \alpha = 0.0, 0.15, 0.25$ $b \alpha = 0.35, 0.5, 0.65$ $c \alpha = 0.75, 0.85, 1.0$

In addition, a simple check is carried out on unmatched points to verify that they would still be visible in an IV position. For each unmatched point in the left image, with co-ordinates (x, y), d_1 is the disparity of the first matched point found to its left, while d_2 is the disparity of first matched point found to its right, with coordinates (x_2, y) . If $(x+\alpha d_1) < (x_2+\alpha d_2)$, this point is still visible at this IV position and eqn. 2 is applied; otherwise, it is occluded. Analogously, for each unmatched point in the right image, with co-ordinates (x, y), d_3 is the disparity of the first matched point found to its left, with co-ordinates (x_3, y) , while d_4 is the disparity of the first matched point found to its right. If $(x_3 + \alpha d_3) < (x + (1 - \alpha d_3))$ α) d_a), this point is still visible at this IV position and eqn. 3 is applied; otherwise, it is occluded.

$$I_{IV}(x + \alpha d_1, y) = I_L(x, y) \tag{2}$$

$$I_{IV}(x + (1 - \alpha)d_4, y) = I_R(x, y)$$
 (3)

Finally, the intensity values for the intermediate view positions that have not been reconstructed by the above process are obtained using a bilinear interpolator.

Experimental results and conclusions: Stereo image pair MAN [4] is used to test the algorithm. It was captured using a parallel camera setup. Fig. 2 shows the original left ($\alpha = 0.0$) and right views ($\alpha =$ 1.0) as well as synthesised views for different values of α .

The algorithm provides high-quality scene reconstruction, with very realistic synthesis. This is corroborated by the very gradual displacements present in the intermediate views, that starts as one image of the stereo pair and slowly, as a function of the parameter α, 'warps' towards the other. Consequently, the resulting synthesis does not look like a mere mapping of the intermediate view intensities over the co-ordinates of one of the original stereo images, which creates an unnatural appearance of the image 'spinning' around an axis of rotation.

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M.M. Perez, C.L. Pagliari and T.J. Dennis (Department of Electronic Systems Engineering, University of Essex, Colchester, CO4 3SQ, United

E-mail: {mdmper, clpagl, tim}@essex.ac.uk

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Four-channel wavelength selector monolithically integrated on InP

R. Mestric, M. Renaud, F. Pommereau, B. Martin, F. Gaborit, G. Lacoste, C. Janz, D. Leclerc and

D. Ottenwalder

A four-channel wavelength selector with 200 GHz channel spacing monolithically integrated on InP is reported. Record low fibre-tofibre insertion loss of 1.5dB was obtained at a bias current of only 30mA. BER performance at 2.5Gbit/s has also been investigated.

Introduction: Selective filters with very fast switching times are very attractive devices for the routing and switching of optical packets in WDM networks [1]. Such filters can be realised by combining two phased-array wavelength demultiplexers and optical gates, as illustrated in Fig. 1 with the so-called wavelength selector. The first demultiplexer spatially separates the incoming wavelength channels, which are then amplified or attenuated by optical amplifiers. A second identical phased-array multiplexes the signals from each amplifier into a single output port. The filter is digitally controlled: each specific wavelength is filtered by injection current control of the corresponding amplifier. Consequently, the wavelength selector is more simply controlled than tunable filters, such as acousto-Optic or Fabry-Perot filters, the passbands of which have to be tuned in order to change channels. Moreover, the wavelength selector provides access to several channels simultaneously, and its switching speed is limited only by the rise and fall times of the optical amplifiers, which are typically <1 ns.

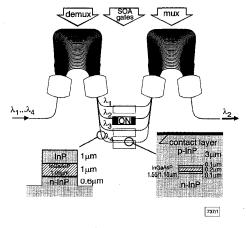


Fig. 1 Schematic diagram of wavelength selector, showing structures of active and passive sections

Wavelength selectors have already been reported [2, 3]. The first device [2], monolithically integrated on InP, suffered from high propagation loss in passive waveguides due to the choice of the integration technology. A lossless wavelength selector based on the hybrid integration of silica phased-array wavelength demultiplexers and semiconductor optical amplifiers on a PLC platform was reported [3]. However, the device is physically large and integration complexity increases with the number of channels. The realisation of robust active-passive integration technology, suited to a variety of complex devices, remains a key technological challenge for the fabrication of compact low-cost devices. Here, we show the potential of the monolithic integration of deep ridge passive waveguides and BRS active waveguides through the realisation of a high-performance compact wavelength selector.

Device structure: The structure of our wavelength selector is depicted in Fig. 1. For the integration of the demultiplexers and SOAs on the same InP substrate, we have chosen a butt-joint coupling technique, which offers a large degree of freedom in the design of the waveguide structures. A deeply-etched structure was used for the phased-array wavelength demultiplexers. It consists of a 1 μ m thick quaternary layer ($\lambda_g = 1.05 \mu$ m) with 1 μ m thick undoped InP layer on top. The width of the waveguide is 2.5 μ m for zero birefringence, and the etched depth is 2.6µm. One advantage of this structure is that the etch depth does not have to be precisely controlled to ensure polarisation independence. We have already demonstrated high-performance polarisation-insensitive phased-array wavelength demultiplexers with this deep ridge structure [4].

The SOA consists of a separate confinement heterostructure (λ_{φ} = 1.18 \mum, 0.1 \mum thick) with a low tensile-strained bulk active layer (0.2µm thick) [5]. The introduction of tensile strain in the active layer provides polarisation-independent gain for a nominal waveguide width of 1.2 µm. It should be noted that while an increased SOA width hardly affects the gain polarisation dependence, a reduction in width will have a greater effect.

A four-channel wavelength selector has been fabricated with two identical 200GHz frequency channel spacing phased-array wavelength demultiplexers containing 40 waveguides in the grating and having a free spectral range (FSR) of 22nm. The four SOAs are 750 µm long and are spaced by 150 µm. The chip dimensions are 3.2mm $\times 1.7$ mm.

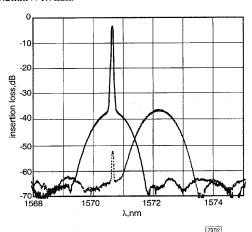


Fig. 2 Output spectrum of wavelength selector for channel 1 (λ = 1570.7nm) when SOA 1 or SOA 2 are biased with 30mA

- SOA 1 ---- SOA 2

Experimental results: First, the channel spacing and the FSR of the wavelength selector were checked by analysing the amplified spontaneous emission (ASE) of the SOAs filtered by the demultiplexers with an optical spectrum analyser (OSA). The expected values were obtained. The peak gain for all the SOAs was ~1580nm at 30mA (CW) bias current. For higher bias current, we observed a lasing peak in the middle of the gain profile due to residual reflectivity at the butt-joint.

Next, we injected a signal from a tunable laser into the wavelength selector and examined the optical output; coupling was achieved using lensed fibres. The signal was set to a wavelength corresponding to one of the four channels of the wavelength selector, i.e. 1570.7, 1572.3, 1573.9 or 1575.5 nm. When the corresponding SOA was biased with 30mA (CW) current, the fibre-to-fibre insertion loss of the wavelength selector was ~3dB for -4dB input power. When a different SOA was biased without changing the signal wavelength, the signal level was suppressed by 50dB, as shown in Fig. 2.

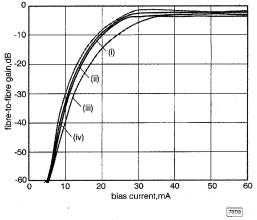


Fig. 3 Fibre-to-fibre gain of four channels of wavelength selector

(iii) channel 3

(i) channel 1 (iv) channel 4 (ii) channel 2

Fig. 3 shows the gain against current characteristics of the wavelength selector for all the SOAs. In this experiment, only one amplifier is biased at a time. The polarisation of the input signal is adjusted in order to maximise the gain. We can see that the fibreto-fibre gain of the wavelength selector is limited to -1.5dB for the best channel and -3.5dB for the worst due to the lasing effect described above. For bias currents higher than 30mA, the SOAs are clamped and the gain is constant. The polarisation dependence of the device is close to 5dB, but the maximum gain for the four SOAs was measured for the same polarisation. Most of this polarisation dependence is attributed to the SOAs, the etched widths of which are somewhat smaller than the design value (~0.2µm).

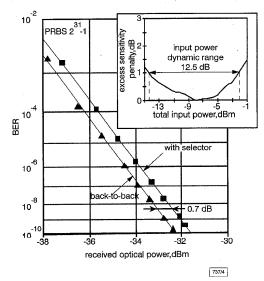


Fig. 4 BER performance of wavelength selector at 2.5 Gbit/s for input power of -8dBm, and excess sensitivity penalty against input power

No post-selector optical filtering is used Inset: excess sensitivity penalty against input power

In a last experiment, we measured the bit error rate (BER) performance of the wavelength selector at 2.5Gbit/s with a PRBS of 231-1. For experimental convenience, we measured the BER for the fourth channel at 1553.6nm (one FSR below the gain peak)

for 30mA (CW) bias current. The on-fibre modulated input power was -8dBm. From Fig. 4, we see that the sensitivity penalty is 0.7dB at 10-9 BER after insertion of the wavelength selector, compared to back-to-back transmission, when no post-selector optical filtering is used. The input power dynamic range for an excess sensitivity penalty of 1 dB is 12.5dB.

Conclusion: We have fabricated a four-channel compact wavelength selector monolithically integrated on InP with 200GHz channel spacing, 50dB on-off ratio and minimum 1.5dB insertion loss for only 30mA bias current. A sensitivity penalty of only 0.7dB for 10-9 BER at 2.5Gbit/s was measured, with a dynamic range of 12.5dB for an excess sensitivity penalty of 1dB. These first results, to our knowledge the best reported so far for a monolithically integrated wavelength selector, make this device very promising for high-speed packet switching applications in optical networks.

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R. Mestric, M. Renaud, F. Pommereau, B. Martin, F. Gaborit, G. Lacoste, C. Janz, D. Leclerc and D. Ottenwalder (OPTO+, Groupement d'Intérêt Economique, Alcatel Corporate Research Centre, Route de Nozay, F-91460 Marcoussis, France)

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Division algorithm over $GF(2^m)$

E.M. Popovici and P. Fitzpatrick

A new division algorithm over $GF(2^m)$ is presented. The serial-in, parallel-out structure is independent of the defining polynomial of the field, and uses operands represented in canonical basis. Because of its regularity and simplified control structure, the resulting divider is hardware efficient and suitable for VLSI implementation.

Introduction: Galois field arithmetic has received a great deal of attention because of applications in error control coding and cryptography [1, 2]. While multiplication has been the subject of a number of papers [2-4], and the conventional technique for inversion is Euclid's algorithm (or table lookup), division in canonical basis is still relatively poorly studied. In this Letter, a fast division algorithm is proposed for $GF(2^m)$, requiring 2m clock cycles. Both inputs and outputs are represented in canonical basis so no basis conversion is required; hence it is readily matched to any input or output system. Owing to its simplicity, the design for large m is easy to realise. Also, the algorithm is independent of the irreducible polynomial used to define the field. Our algorithm may be extended to division in the field $GF(p^m)$ for any prime p.

Division in $GF(2^m)$: Let p(x) be an irreducible polynomial of degree m with coefficients in GF(2). Then we may identify $GF(2^m)$ with the set of polynomials of degree at most m-1 with coeffi-

cients in GF(2) under the operations of addition and multiplication modulo p(x). Let $a, b \in GF(2^m)$, $a \ne 0$ and consider the problem of determining the quotient $u = b/a \in GF(2^m)$. The equation ua - b = 0 in $GF(2^m)$ is equivalent to the polynomial equation ua - b = vp where, with δ denoting degree, $\delta(ua - b) \le m - 1 + \delta(a)$. It follows that the congruence $ua + vp \equiv b \mod x^i$ an equation when $t = m + \delta(a) - 1$. The idea of the algorithm is to build up to this equation by successively solving the congruences $ua + vp \equiv b \mod x^i$, $i = 0, \dots, t$, for the pair (u, v). We initiate with the set of three pairs $(u_i, v_1) = (1, 0)$, $(u_2, v_2) = (0, 1)$, $(u_3, v_3) = (0, 0)$. At step i we compute the discrepancies d_1, d_2, d_3 according to the formulas

$$u_1a + v_1p \equiv d_1x^i \mod x^{i+1}$$
$$u_2a + v_2p \equiv d_2x^i \mod x^{i+1}$$
$$u_3a + v_3p + b \equiv d_3x^i \mod x^{i+1}$$

Now define (u_1, v_1) to be smaller than (u_2, v_2) if

$$\delta(u_1) \le \delta(v_2) + 1 \tag{1}$$

otherwise (u_2, v_2) is smaller than (u_1, v_1) . Let k denote the index of the smaller of (u_1, v_1) , (u_2, v_2) and let \bar{k} denote the index of the larger. Observing that it is not possible for both d_1 and d_2 to be zero, new pairs (u_1, v_1) , (u_2, v_2) , (u_3, v_3) are constructed as follows: if $d_k = 0$ then

$$\begin{cases} (u_k,v_k) = (u_k,v_k) \\ (u_3,v_3) = (u_3,v_3) + d_3(u_{\bar{k}},v_{\bar{k}}) \\ (u_{\bar{k}},v_{\bar{k}}) = x(u_{\bar{k}},v_{\bar{k}}) \end{cases}$$

if $d_k = 1$ then

$$\begin{cases} (u_{\bar{k}}, v_{\bar{k}}) = (u_{\bar{k}}, v_{\bar{k}}) + d_{\bar{k}}(u_k, v_k) \\ (u_3, v_3) = (u_3, v_3) + d_3(u_k, v_k) \\ (u_k, v_k) = x(u_k, v_k) \end{cases}$$

Here, the addition of pairs and multiplication by scalars and by x are defined componentwise in the obvious fashion. The flowchart is presented in Fig. 1.

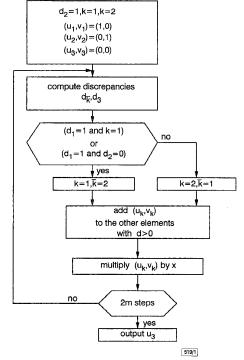


Fig. 1 Division algorithm flowchart

Implementation: As stated previously, the number of clock cycles for performing the division is 2m. The architecture for serial-in, parallel-out implementation of the algorithm is presented in Fig. 2.