A highly integrated 32-SOA gates optoelectronic module suitable for IP multi-terabit optical packet routers

N. Sahri, D. Prieto, S. Silvestre, D. Keller, F. Pommereau, M. Renaud, O. Rofidal*, A. Dupas*, F. Dorgeuille*, and D. Chiaroni*

OPTO+, Groupement díIntérêt Economique
**Alcatel CIT*
Alcatel Research & Innovation
Route de Nozay, 91460 Marcoussis Cedex, France
Nabil.Sahri@alcatel.fr

Abstract: For the first time, the realization and the performance of a compact optoelectronic 32-SOA module including their drivers is reported. Preliminary experiments in an optical packet switching matrix for IP multi-terabit router is also reported.

1. Introduction

The internet demand, in constant increase, pushes constructors to propose solutions to provide capacity and flexibility for the future network. Optical packet switching techniques could provide both aspects. For several years, constructors have studied optical switching matrices [1,2] adapted to these needs. The SOA technology, by providing the required specifications (high On/Off, sub-nanosecond switching times and enough maturity) has been rapidly identified as a key technology for such applications.

For an industrial approach however, integration, packaging technique and cost-effectiveness become key issues. The SOA gate array approach is very attractive, as it provides modular building blocks which could be easily implemented in large-scale optical space-switches. Such devices have been fabricated and assembled either in conventional standard butterfly package [3] or flip-chip mounted on a silicon planar lightwave circuit and associated with an optical passive circuit [4], both including high speed electronic drivers.

We report here, for the first time to our knowledge, on the realization of a high performance, cost-effective and compact optoelectronic module including 32-SOA gates and their associated high-speed drivers. A lot of attention was paid to the optimization of the power consumption. Technologies implemented and performance are reviewed and preliminary experiments based on such a module in an optical matrix for multi-terabit routers is also reported.

2. Module characteristics

The fabricated module is presented in Fig.1. It consists of three main parts : The SOA-array sub-modules (SM), the printed circuit board (PCB) supporting the drivers and realizing the electrical interconnections and the housing, including the thermoelectric coolers (TEC). Each SM includes an array of 4 SOA gates flip-chip mounted on a silicon submount [5] with V-grooves. The flip-chip is done passively by self-alignment process using 3D structures. The SOAs are pigtailed in a collective manner using lensed fiber ribbons ensuring coupling losses < 5 dB per facet and terminated with small-form-factor MU connectors chosen for optimum compactness. Electrical access to the SOAs is done using an alumina transmission line attached to the SM housing. Bonding wires connect the SM transmission lines to the drivers placed as close as possible to these latter to avoid degrading the driver output signal. The driver ICs are directly mounted on the PCB which carries the electrical signals to and from outside the module. Another function ensured by the PCB is to evacuate the heat generated by the ICs through an inserted thermal drain. This latter is adequately put in contact during the assembly with an external radiator attached to the housing base. This approach was proven to be sufficient to evacuate the heat generated by the electronic chips and to avoid having their back side temperature increase to a damage level. The SOA temperature is kept constant by placing each SM on a dedicated TEC. The optimization of heat evacuation was done by using high thermal dissipation materials associated to a clever design. Thus the overall module power consumption (TEC and drivers) is less than 3W (7W) at an external temperature of 35 C (55 C), in a module operation where two SOA gates are active simultaneously.

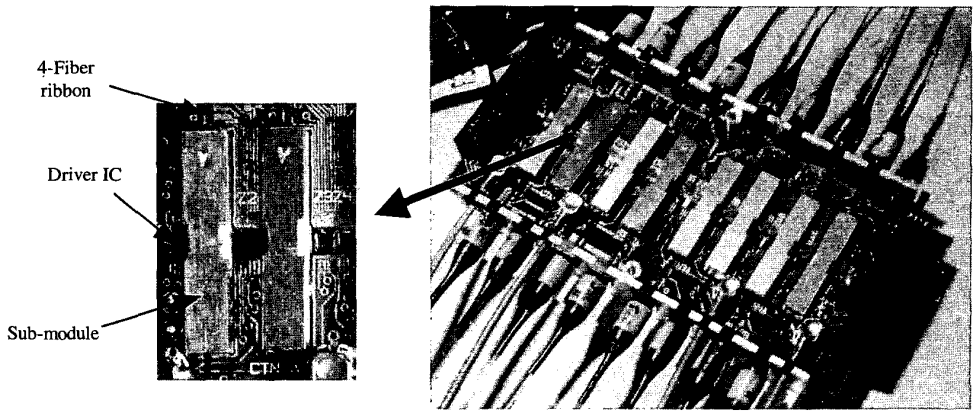

Figure 1: 32-SOA gate module. The size is 100 x 50 x18 mm^3.

The electronic drivers are key elements for the switching operation of the module. The ICs were fabricated in a commercial foundry using a GaAs p-HEMT process. They are responsible for the regeneration and the synchronization of a command signal with respect to a clock input. The performances obtained from these chips are : high output current (~200 mA) and a switching time < 5 ns necessary to ensure packet switching. This time is an order of magnitude longer than previously reported one [3] because of the major constrain introduced by the low power consumption requirement. Thus the drivers logical function was designed using a Direct-Coupled Field effect transistor Logic circuitry (DCFL) (< 5 mW for a 13 transistors D-Flip-flop). The output current is adjustable between 0 to 300 mA for each SOA gate at the will of the user so as to equalize the optical power throughout the different channels in the system. The driver design ensured perfect matching to the SOA without the necessity of any additional passive elements. The electrical crosstalk on the PCB was kept below -35 dB.

Static characteristics of a large number (> 100) of packaged SOAs at 200 mA are, among others, a fiber-to-fiber gain Gff of 20 dB ± 2 dB and a noise figure NF of 10 dB ± 0.8 dB. But the major results obtained with these SOAs are their polarization insensitivity with a value of 0.4 dB ± 0.5 dB and the homogeneity of the output power 7 dBm ± 0.5 dBm (Fig. 2). The optical On/Off ratios within the fabricated modules are > 45 dB.

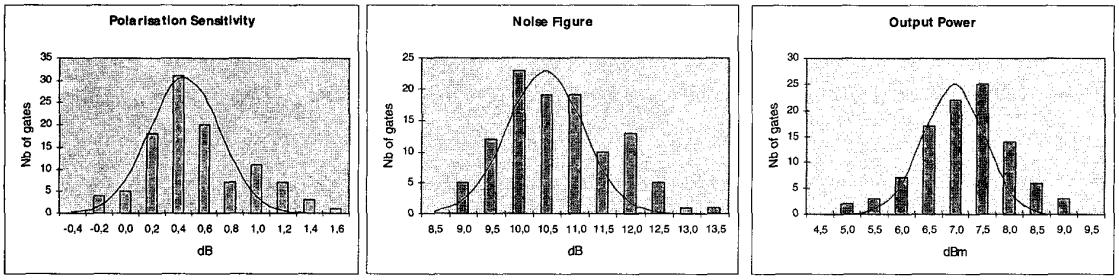

Figure 2: Static characteristics of the SOA.

Figure 3 shows typical dynamic responses of packaged SOAs before and after output-power equalization by the driver. The 0-100% optical switching time is of the order of few nanoseconds. The flatness of these responses is mainly due to the stability of the driver current which is enhanced by the fact that the SOAs are operated under saturation regime.

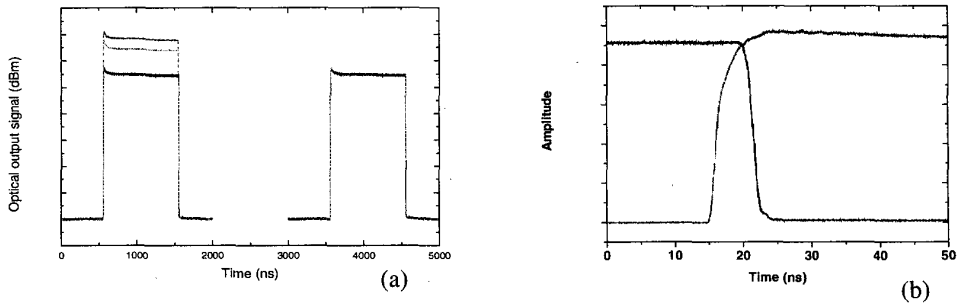

Figure 3. Equalization of the optical power by the driver of three different channels (a). Optical responses rise and fall times (b).

3. Test of an SOA module in an optical matrix environment

To test the SOA module in a system environment, a board (366X460X66 mm3) capable to integrate four 32 SOA modules has been designed and realized. A path of an optical matrix (as proposed for multi-terabit packet router [1]) has been experienced (figure 4a) where SOAs have been exploited as high speed optical gates in WDM regime.

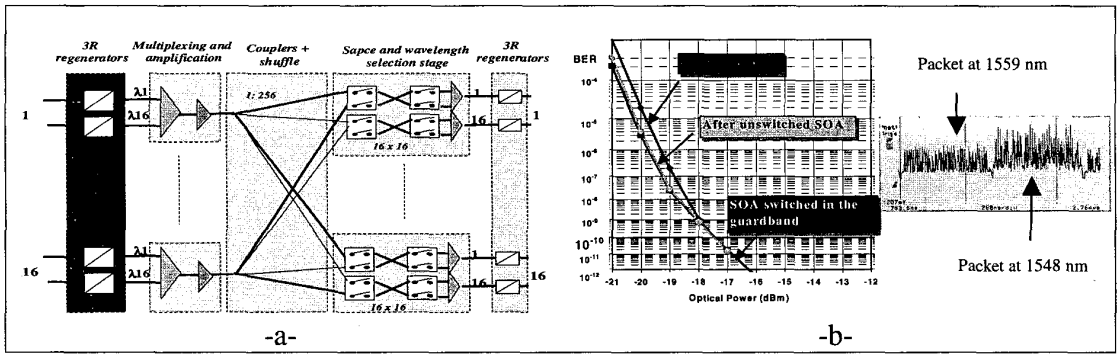

Figure 4: a-Test of a path through an optical matrix of a multi-terabit packet router (a).
10 Gbit/s BER curves through an unswitched and switched SOA, signal visualization before the output 3R regenerator (b).

After amplification and broadcasting, the packets were switched in the space stage (to select the input port) and in the wavelength selection stage (to select the wavelength). The optical packets with a length close to 0.9µs were switched within their guard-bands (~50ns). BER curves measured at 10 Gbit/s with a receiver sensitivity of ñ17.5 dBm at 10^{-10} (figure 4b) showed a negligible sensitivity penalty in a switching regime. This experience fully validate the module for the building of such kind of matrices.

4. Conclusion

In this paper we have presented a 32 SOA module fully equipped and including the electronic drivers. Switching speed, low power consumption, small form factor together with mass production techniques make the developed approach an attractive solution to build future multi-Terabit IP routers. This module has been successfully validated in a multi-terabit optical matrix exhibiting less than 1 dB penalty at 10Gbit/s. The integrated 32 SOA module represents a fundamental step in the next introduction of optical packet switching systems adapted to this Internet world.

[1] D. Chiaroni *et al,* " Towards 10Tbit/s optical packet routers for backboneî , ECOC 2000, Munich, Germany, Sept. 3-7, 2000

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[5] M. Renaud et al., "SOA-based Optical Network Components", invited paper to be published at ECTC'2001, Lake Buena Vista, FL, May 29-June 1, 2001.