Title: Adress Decode Logic

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Diagram:

- U1A
- U1B
- U3A
- U3B
- U3C
- U7A
- PHI2

Connections:

- A15 connected to U1A
- A14 connected to U1A
- PHI2 connected to U3A
- U3A outputs connected to U1B
- U3B outputs connected to U3C
- U3C outputs connected to U7A
- U7A connected to FAKE CE 3
- U1B connected to FAKE CE 2
- U1A connected to FAKE CE 1

Diagram Layout:

- Input pins are labeled A15, A14, A13, PHI2
- Output pins are labeled FAKE CE 1, FAKE CE 2, PHI2