Rockwell

R650X and R651X MICROPROCESSORS (CPU)

DESCRIPTION

The 8-bit R6500 microprocessor devices are produced with N-channel, silicon gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips—the semiconductor threshold is cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides single chip microcomputers, memory and peripheral devices—as well as low-cost design aids and documentation.

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The R650X and R651X family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz, 2 MHz and 3 MHz) and temperature (commercial and industrial) versions.

ORDERING INFORMATION

Part Number: R65XX_ _ _

- Temperature Range (T_L to T_H):
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No letter = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- Model Designator:
  - XX = 02, 03, 04, . . . 15

FEATURES

- N-channel, silicon gate, depletion load technology
- 8-bit parallel processing
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt request
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz, 2 MHz, and 3 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  - —External single clock input
  - —Crystal time base input
- Commercial and industrial temperature versions
- Pipeline architecture
- Single +5V supply

R6500 CPU FAMILY MEMBERS

Microprocessors with Internal Two Phase Clock Generator

Model	No. Pins	Addressable Memory
R6502	40	64K Bytes
R6503	28	4K Bytes
R6504	28	8K Bytes
R6505	28	4K Bytes
R6506	28	4K Bytes
R6507	28	8K Bytes

Microprocessors with External Two Phase Clock Input

Model	No. Pins	Addressable Memory
R6512	40	64K Bytes
R6513	28	4K Bytes
R6514	28	8K Bytes
R6515	28	4K Bytes

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Data Sheet Order No. D39
Rev. 6, February 1984

INTERFACE SIGNAL DESCRIPTIONS

CLOCKS (Ø1, Ø2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level. The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

ADDRESS BUS (A0–A15, R6502)

The address line outputs access data in memory device locations or cells, access data in I/O device registers and/or effect logical operations in I/O or controller devices depending on system design. The addressing range is determined by the number of address lines available on the particular CPU device. The R6502 and R6512 can address 64K bytes with a 16-bit address bus (A0-A15); the R6504, R6507, and the R6514 can address 8K bytes with a 13-bit address bus (A0-A12); and the R6503, R6505, R6506, R6513, and R6515 can address 4K bytes with a 12-bit address bus (A0-A11). These outputs are TTL-compatible and are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0–D7)

The data lines (D0-D7) form an 8-bit bidirectional data bus which transfers data between the CPU and memory or peripheral devices. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

DATA BUS ENABLE (DBE, R6512 ONLY)

The TTL-compatible DBE input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE is driven by the phase two (Ø2) clock, thus allowing data output from microprocessor only during Ø2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

READY (RDY)

The Ready input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (Ø1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (Ø2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as Direct Memory Access (DMA).

INTERRUPT REQUEST ($\overline{IRQ}$)

The TTL level active-low $\overline{IRQ}$ input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Processor Status Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts can occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative going edge on the $\overline{NMI}$ input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during Ø2 (phase 2) and will begin the appropriate interrupt routine on the Ø1 (phase 1) following the completion of the current instruction.

SET OVERFLOW FLAG ($\overline{SO}$)

A negative going edge on the $\overline{SO}$ input sets the overflow bit in the Processor Status Register. This signal is sampled on the trailing edge of Ø1 and must be externally synchronized.

SYNC

The SYNC output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

RESET ($\overline{RES}$)

The active low $\overline{RES}$ resets, or starts, the microprocessor from a power down or restart condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

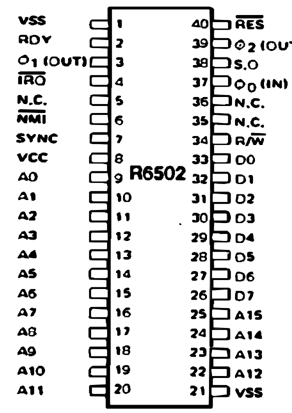
After a system initialization time of six clock cycles, the mask interrupt flag is set and the microprocessor loads the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signals become valid.

2

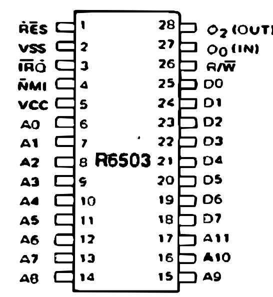
R6502 FEATURES

- 64K addressable bytes of memory (A0–A15)
- $\overline{IRQ}$ interrupt
- On-chip clock
  TTL-level single phase input
  RC time base input
  crystal time base input
- SYNC signal
  (can be used for single instruction execution)
- RDY signal
  (can be used to halt or single cycle execution)
- Two phase output clock for timing of support chips
- $\overline{NMI}$ interrupt
- 40-pin DIP



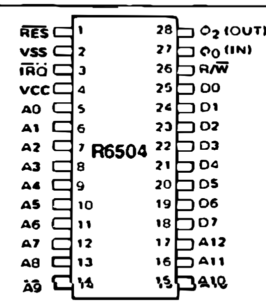
R6503 FEATURES

- 4K addressable bytes of memory (A0–A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



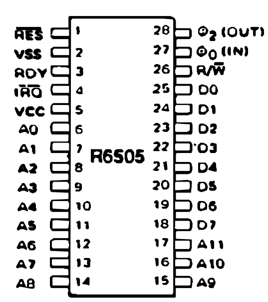
R6504 FEATURES

- 8K addressable bytes of memory (A0–A12)
- On-chip clock
- $\overline{IRQ}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



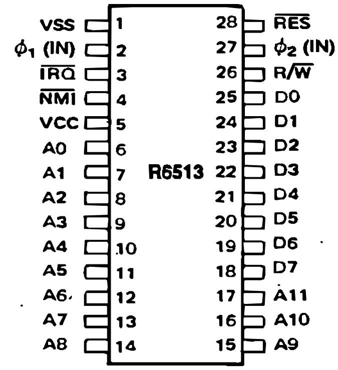
R6505 FEATURES

- 4K addressable bytes of memory (A0–A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP



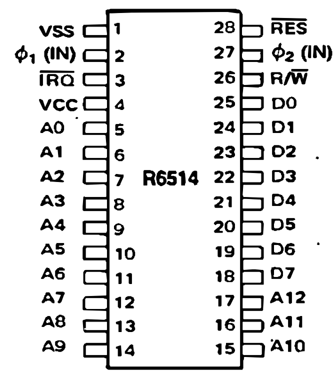
R6513 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



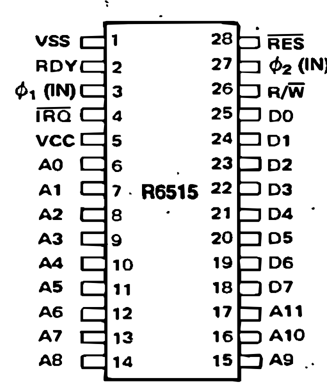
R6514 FEATURES

- 8K addressable bytes of memory (A0-A12)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- 8-bit bidirectional data bus



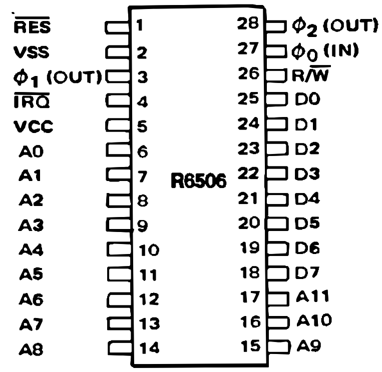
R6515 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- RDY signal
- 8-bit bidirectional data bus



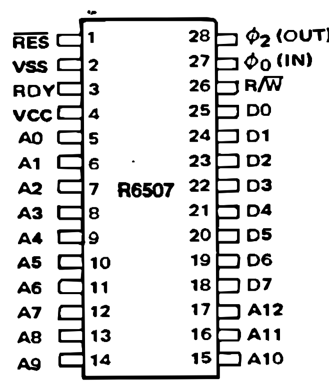
R6506 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- Two phase output clock for timing of support chips
- 8-bit bidirectional data bus
- 28-pin DIP



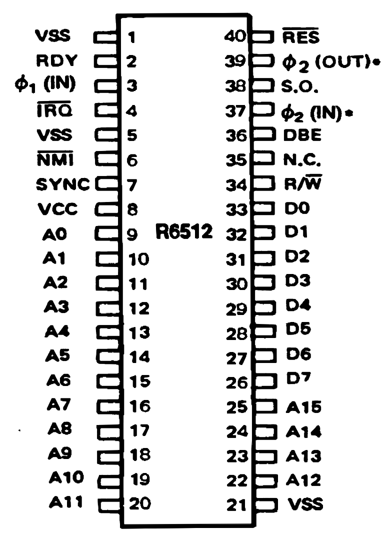
R6507 FEATURES

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP



R6512 FEATURES

- 64K addressable bytes of memory (A0-A15)
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- SYNC signal
- Two phase clock input
- Data Bus Enable
- 40-pin DIP



*Pins 37 and 39 are connected internally

FUNCTIONAL DESCRIPTION

The internal organization of all R6500 CPUs is identical except for some variations in clock interface, the number of address output lines, and some unique input/output lines between versions.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instuction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

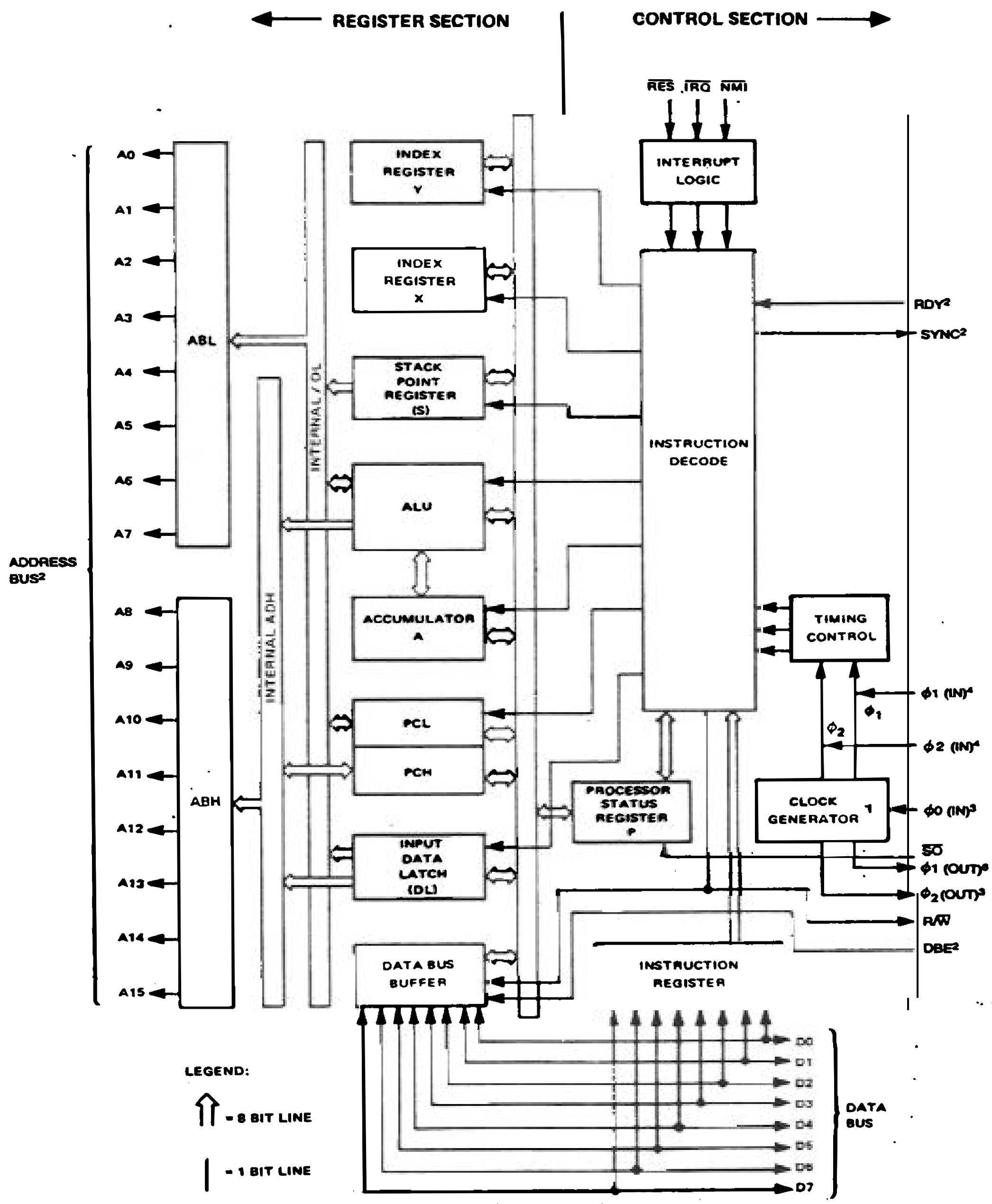
When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$) and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU.



NOTE

1. CLOCK GENERATOR IS NOT INCLUDED ON R6512, R6513, R6514 AND R6515.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE CPUs.
3. R6502, R6503, R6504, R6505, R6506 AND R6507.
4. R6512, R6513, R6514 AND R6515.
5. R6512 ONLY.
6. R6502 ONLY.

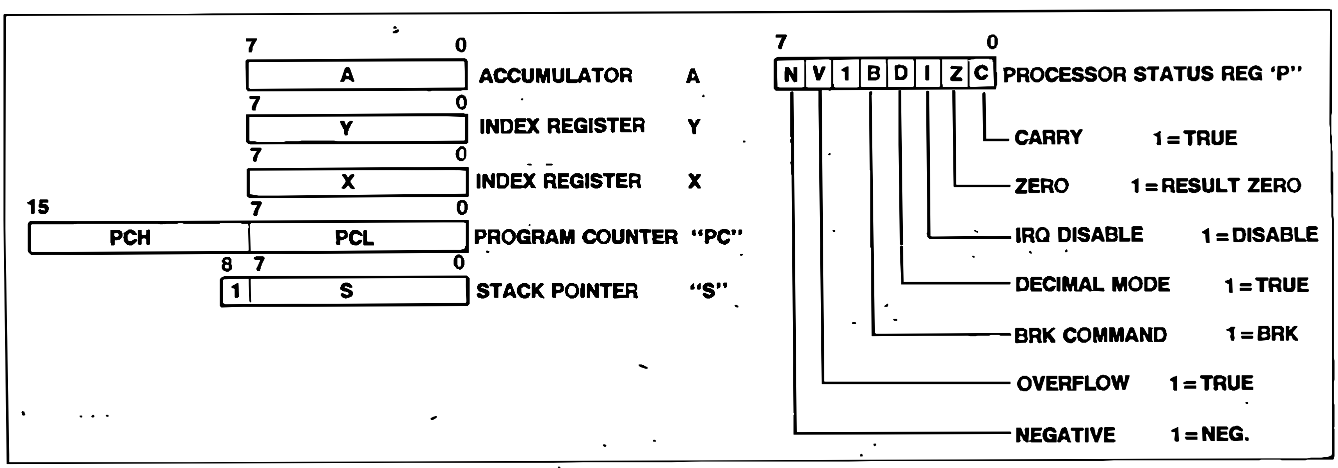
R650X and R651X Internal Architecture

INSTRUCTION SET

The R6500 CPU has 56 instruction types which are enhanced by up to 13 addressing modes for each instruction. The accumulator, index registers, Program Counter, Stack Pointer and Processor Status Register are illustrated below.

Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
		LDA	Load Accumulator with Memory
BCC	Branch on Carry Clear	LDX	Load Index X with Memory
BCS	Branch on Carry Set	LDY	Load Index Y with Memory
BEQ	Branch on Result Zero	LSR	Shift One Bit Right (Memory or Accumulator)
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	NOP	No Operation
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	ORA	"OR" Memory with Accumulator
BRK	Force Break		
BVC	Branch on Overflow Clear	PHA	Push Accumulator on Stack
BVS	Branch on Overflow Set	PHP	Push Processor Status on Stack
		PLA	Pull Accumulator from Stack
CLC	Clear Carry Flag	PLP	Pull Processor Status from Stack
CLD	Clear Decimal Mode		
CLI	Clear Interrupt Disable Bit	ROL	Rotate One Bit Left (Memory or Accumulator)
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator	RTI	Return from Interrupt
CPX	Compare Memory and Index X	RTS	Return from Subroutine
CPY	Compare Memory and Index Y		
		SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		STA	Store Accumulator in Memory
EOR	"Exclusive-OR" Memory with Accumulator	STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator



Programming Model

ADDRESSING MODES

The R6500 CPU family has 13 addressing modes. In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [Absolute]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING [ZP, X or Y]—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING [ABS, X or Y]—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

2

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [Indirect]—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the Op Codes associated with the R6500 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2					
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	
3	BMI Relative 2 2**	AND (IND), Y 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	
7	BVS Relative 2 2**	ADC (IND), Y 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	
9	BCC Relative 2 2**	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	
F		SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*		

	0	
0	BRK Implied 1 7	—OP Code —Addressing Mode —Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page; add 2 to N if branch occurs to different page.

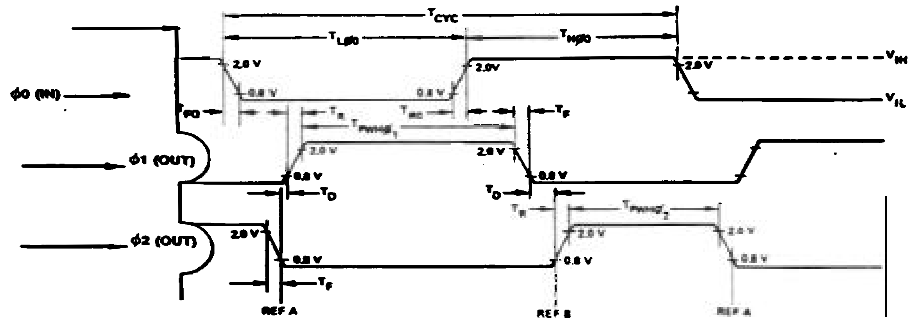
INSTRUCTION SET SUMMARY

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 / N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 … 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							• • • • • • • •	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																															M7 M6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 … 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	← [7 … 0] ← C ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	→ C → [7 … 0] →				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																												96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													[illegible]	[illegible]	[illegible]																									N • • • • • Z •	TYA

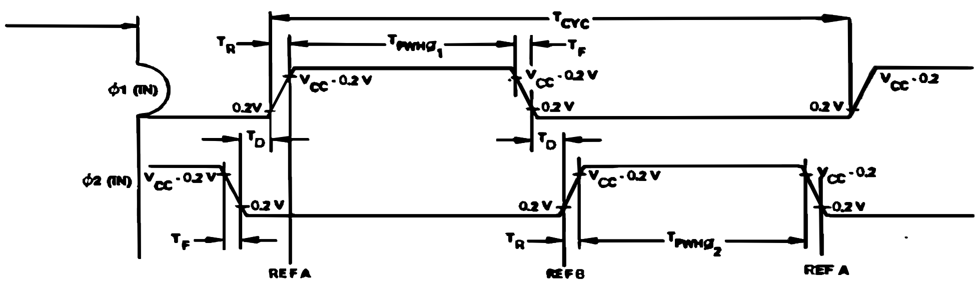
(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M7	MEMORY BIT 7
Y	INDEX Y	−	SUBTRACT	M6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	⊻	EXCLUSIVE OR		

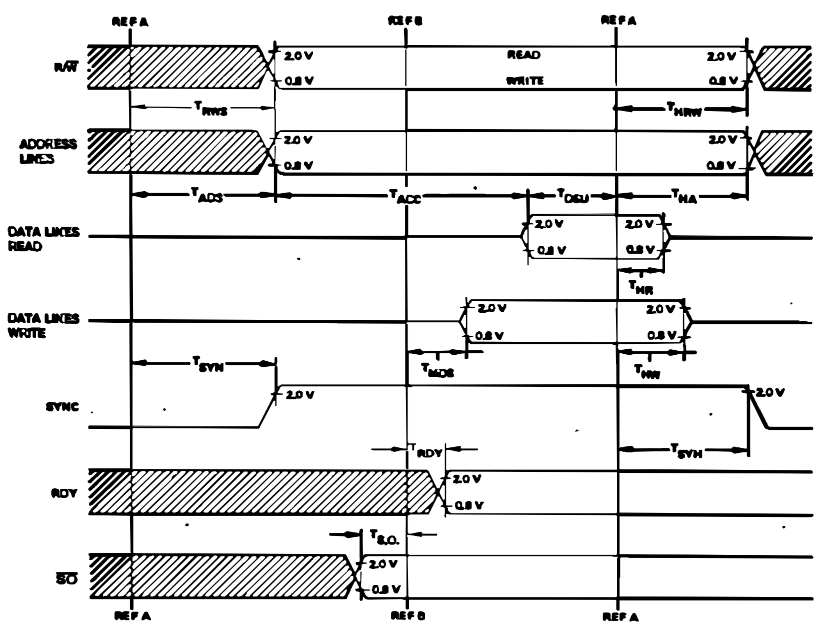
R650X CLOCK TIMING



R651X CLOCK TIMING



R65XX READ WRITE TIMING



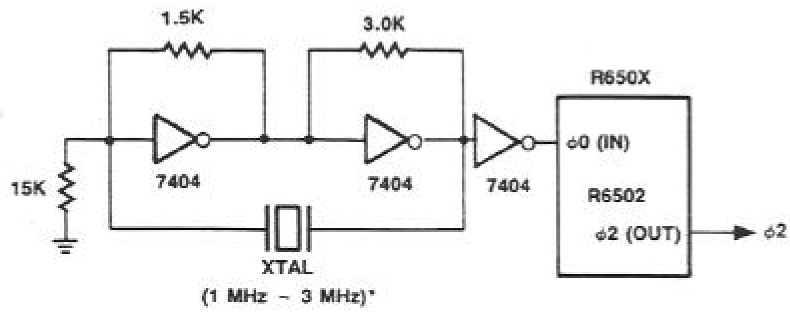
AC CHARACTERISTICS

Characteristic	Symbol	R65XX (1 MHz) Min	R65XX (1 MHz) Max	R65XXA (2 MHz) Min	R65XXA (2 MHz) Max	R65XXB (3 MHz) Min	R65XXB (3 MHz) Max	Unit
R650X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
ø0 (IN) Low Pulse Width	$T_{L\phi 0}$	480	—	240	—	160	—	ns
ø0 (IN) High Pulse Width	$T_{H\phi 0}$	460	—	240	—	160	—	ns
ø0 (IN) Rise and Fall Time[1, 2]	T_{R0}, T_{F0}	—	10	—	10	—	10	ns
ø1 (OUT) High Pulse Width	$T_{PWH\phi 1}$	460	—	235	—	155	—	ns
ø2 (OUT) High Pulse Width	$T_{PWH\phi 2}$	460	—	240	—	160	—	ns
Delay Between ø1 (OUT) and ø2 (OUT)	T_D	0	—	0	—	0	—	ns
ø1 (OUT), ø2 (OUT) Rise and Fall Time[1, 2]	T_R, T_F	—	25	—	25	—	15	ns
R651X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
ø1 (IN) High Pulse Width	T_{PWH01}	430	—	215	—	150	—	ns
ø2 (IN) High Pulse Width	T_{PWH02}	470	—	235	—	160	—	ns
Delay Between ø1 and ø2	T_D	0	—	0	—	0	—	ns
ø1 (IN), ø2 (IN) Rise and Fall Time[1, 3]	T_R, T_F	—	25	—	20	—	15	ns
R65XX READ/WRITE TIMING								
R/W̄ Setup Time	T_{RWS}	—	225	—	140	—	110	ns
R/W̄ Hold Time	T_{HRW}	30	—	30	—	15	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	ns
Address Hold Time	T_{HA}	30	—	30	—	15	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	—	175	—	100	—	85	ns
Write Data Hold Time	T_{HW}	30	—	30	—	15	—	ns
SYNC Hold Time	T_{SYH}	30	—	30	—	15	—	ns
RDY Setup Time	T_{RDY}	100	—	50	—	35	—	ns
S̄Ō Setup Time	T_{SO}	100	—	50	—	35	—	ns
SYNC Setup Time	T_{SYN}	—	225	—	140	—	110	ns

Notes:
1. Loads: All output except clocks = 1 TTL + 130 pF. Clock outputs = 1 TTL + 30 pF.
2. Measured between 0.8 and 2.0 points on waveform load.
3. Measured between 10% and 90% points on waveforms.
4. *RDY must never switch states within R_{RDY} to end of ø2.

2

RECOMMENDED TIME BASE GENERATION FOR R6502



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to 70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[5]	Max.	Unit[1]	Test Conditions
Input High Voltage Logic, φ0 (IN) φ1 (IN), φ2 (IN)	V_{IH}	 2.0 V_{CC} −0.3	 — —	 V_{CC} V_{CC} + 0.25	V	
Input Low Voltage Logic, φ0 (IN) φ1 (IN), φ2 (IN)	V_{IL}	 −0.3 −0.3	 — —	 0.8 0.4	V	
Input Leakage Current Logic (Excl. RDY, S.O.) φ1 (IN), φ2 (IN) φ0 (IN)	I_{IN}	 — — —	 — — —	 2.5 100 10	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for Three State Off D0-D7	I_{TSI}	 —	 —	 10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage SYNC, D0-D7, A0-A15, R/$\overline{W}$, φ1 (OUT), φ2 (OUT)	V_{OH}	 +2.4	 —	 —	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage SYNC, D0-D7, A0-A15, R/$\overline{W}$, φ1 (OUT), φ2 (OUT)	V_{OL}			 +0.4	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
Power Dissipation 1 and 2 MHz 3 MHz	P_D	 — —	 450 500	 700 800	mW	
Capacitance Logic D0-D7 A0-A15, R/$\overline{W}$, SYNC φ0 (IN) φ1 (IN) φ2 (IN)	C C_{IN} C_{OUT} $C_{φ0(IN)}$ $C_{φ1}$ $C_{φ2}$	 — — — — — —	 — — — — 30 50	 10 15 12 15 50 80	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistor.
4. φ1 (IN) and φ2 (IN) apply to R6512, 13, 14, and 15; φ0 (IN) applies to R6502, 03, 04, 05, 06 and 07.
5. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.