EE 470: Configurable Computing
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Equal B216
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Lectures:
Currently TTh 1:30-2:50, but we will work to find consensus on another possible time.
Office Hours: TTh 3-4pm or other times by arrangement

Textbook:
There will not be a textbook for the class. Instead, readings will be from company’s technical
specifications and a selection of research papers. Traditionally, I’ve tried to have a course reader from
Pequod for the class, but over time, more and more documents in this area are available electronically via
the web, so I am likely to dispense with the reader this time and simply have a web page with links to most
of the relevant papers.

Course Objectives:
By the end of the course, you will be able to:

- Create basic designs with programmable devices
- Describe the internals of commonly-available FPGA devices and the design tradeoffs involved in their
  architectures.
- Discuss the costs and benefits of designing with gate-level programmable parts (e.g. FPGAs) versus
  instruction-level programmable parts (e.g. microprocessors)
- Evaluate application characteristics to determine their suitability to configurable hardware
  implementations
- Design an application-specific accelerator using FPGAs
- Identify the key contributions of a research paper and evaluate the experimental methodologies used in
  evaluating proposed ideas.

Course Structure:
The course will have 5 main parts as listed below:

- 2/1-2/15: Traditional and FPGA-based computing Architectures
  - Overview of FPGA architectures
  - Internals of an FPGA
  - Case studies with Xilinx and Altera parts
  - Some review of computer architecture: memory architectures and I/O bus models
  - Basics of parallel computing, cache consistency, etc.
- 2/15-2/24: Intro to CAD Techniques
  - Typical CAD toolflows
  - Design tradeoffs and algorithm choices for synthesis, routing, etc.
- 2/29-3/14: Configurable Hardware Systems
- Chimaera, Garp, DPGA, Brass, PRISC, RAW, and many many more
  - Nimble, PRISC, DeepC, and others
- 4/13-4/27: Applications experiences
  - Graph problems, Boolean satisfiability, signal processing, ATR, and others

In addition to covering research material etc. some classes will be devoted to questions or thorny issues that may have come up as you work on your projects. These will be determined on an as-requested basis, so don’t be shy about asking for them.

Lectures:
This is not likely to be a large class, so I am eager to get some good discussions going. Please be ready to participate. I know it’s a bit unusual at first, but once you get in the habit, I think you’ll agree it’s a lot more fun than if I drone at you for 80 minutes….. If you happen to be having a lousy day/week, feel free to email or speak to me in advance and I won’t call on you that day.

On the course days when we cover research papers, one student will be in charge of thinking up discussion questions and leading a discussion. Hint: thinking up the questions is the easy part….getting your fellow students to discuss things is the tough part. Feel free to start arguments, feed people caffeine, pass out bribes, or whatever else it takes to get a rousing discussion going.

Projects:
I assume that the projects are the main attraction for most of you taking the class. We will do design projects using the Compaq Pamette FPGA cards. They have four FPGAs and some SRAM on them, and they hook into the PCI I/O bus of a standard PC. We have four installed in a basement lab (B115). Here’s a timetable for the projects:

- Feb 22: In-class 5-minute summaries of project proposals. Hand in a 1-page description of what you hope to do.
- Mar 21: In-class 5-minute status reports about what headway you’ve made on the projects. Hand in a 3-5 page summary of your design plans, block diagrams, and current status.
- April 25: Demo Day. Class will meet in B115 for project demos and a party. Flashiest demo & coolest project will be voted on for a prize.
- Dean’s date (May 9): Final project reports due.

Fabulous Class Prizes:
Two prizes will be given out at the end of the semester:

- Best Discussion leader: The student who is named (through a vote of your peers) to have been the best discussion leader of the semester will receive a fabulous prize.
- Best Project: The student (or students) who are named to have done the coolest project will also receive a fabulous prize.

Grade Breakdown: 30% participation, 70% project