Micropower Wireless Sensors

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ABSTRACT

This paper describes circuit architectures and techniques to meet the specialized requirements of energy-autonomous micro-sensor nodes. We address the fundamental components, namely the ADC, DSP, and radio, at the node-level to isolate important optimizations and functions. Using prototyped implementations, low energy and power-aware circuits are presented. These, state-of-the-art techniques demonstrate that practical self-powered nodes are possible.

Keywords: wireless sensor networks, integrated circuits, power-aware circuits, sub-threshold, low-power design.

1 INTRODUCTION

Sensor networks consist of hundreds to thousands of energy-autonomous nodes. The fundamental components, namely an analog-to-digital converter (ADC), a digital signal processor (DSP), and a radio, enable ad-hoc deployment, self-organization, and collaborative sensing/processing. An additional energy subsystem generates a usable power supply from the output of an energy harvesting source, enabling indefinite, self-powered operation from ambient sources [1].

Typical sensor operating scenarios are characterized by short bursts of activity between long idle periods. Research on energy-harvesting mechanisms to date suggests that a reasonable average power budget for a self-powered node is 100μW [2]. Under these circumstances, duty-cycling, where circuits are powered down between active operations, is invaluable, but the overhead of active-idle state transitions must be minimized. Of course, during the brief active periods, efficiency is still critical to meeting the stringent energy limitations. However, since a high throughput is not required, the speed constraint can be removed from this optimization to derive a point of minimum energy operation. Finally, ad-hoc deployment and energy harvesting imply that both the constraints and requirements of the sensor nodes are unpredictable and time varying [3]. It is essential, therefore, that their performance be dynamically scalable to optimize power consumption with respect to desired observation quality.

The following sections present the most effective techniques and prototype results for the ADC, DSP, and radio to enable efficient and energy-scalable sensor nodes.

2 ANALOG-TO-DIGITAL CONVERTER

The 12b, 100kS/s ADC in [4] represents an upper bound in performance required for most micro-sensor applications. Consuming a total of just 25μW, it is the most efficient design demonstrated to date, and its sampling rate can be reduced arbitrarily to yield linear power savings. Additionally, a low power 8b mode enables further power savings when the dynamic environment and energy budget allow for reduced observation quality.

Sensor nodes must detect highly sporadic events and may only be able to sample data once before having to react. Consequently, even though oversampling converters ease the anti-aliasing requirements, Nyquist acquisition is preferred. In this scenario, successive approximation register (SAR) ADCs meet the speed and resolution requirements of micro-sensor applications with the lowest power consumption.

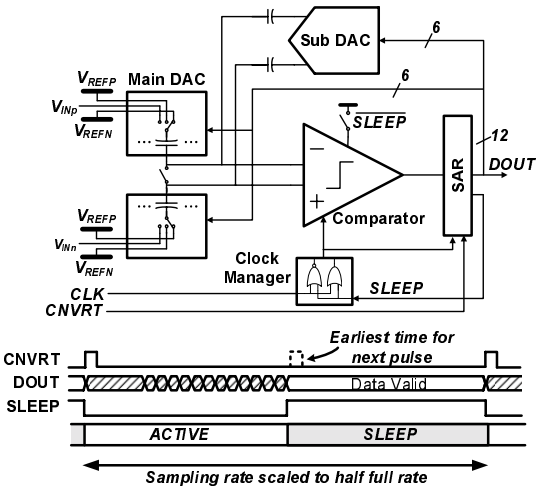


Figure 1: Successive approximation register ADC block diagram.

A block diagram of the ADC in [4] is shown in Fig-

ure 1. This design can operate at low voltages since the comparator doesn't require a large linear range, the state machine (SAR) is digital, and the DAC is passive. As a result, until noise limitations become dominant, the power supply V_{DD} can be reduced to greatly increase efficiency. In particular, analytical models show that the optimum energy-per-conversion (for a constant SNR) occurs at 800mV if the relative contributions of the noise limited and non-noise limited circuits are accurately seeded. In practice, a higher supply, of 1V, was used in [4] to avoid reliability issues with weak-inversion biasing circuits and floating switches.

The only active component in a SAR ADC is the comparator, which can be powered-off with very little overhead. As a result, by clock-gating the digital circuits and power-gating the analog circuits, the total current drawn by the ADC can be reduced to leakage levels. The waveforms in Figure 1 show how sample rate control is implemented in [4]. An input pulse on $CNVRT$ initiates the conversion, and when the ADC is done, it asserts a $SLEEP$ signal to enforce the clock/power-gating. In the shown example, the sampling rate and power consumption are half their maximum values.

The dominant source of power consumption in most 12b SAR ADCs is the comparator. Figure 2 shows a block diagram of the comparator in [4]. The two signal paths are optimized for the gain and noise requirements of the precision mode (i.e. 12b or 8b) and can be selectively de-activated.

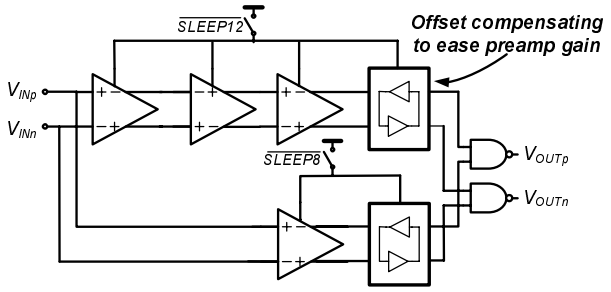
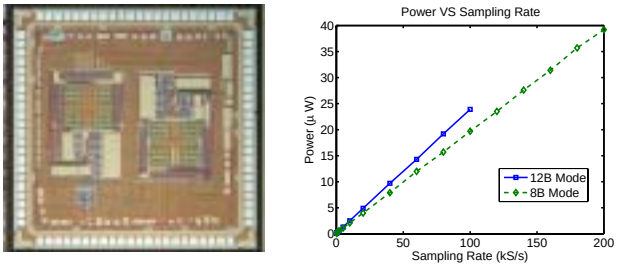


Figure 2: Block diagram of a scalable, energy efficient comparator.

Latches have a superior power-delay product compared with linear amplifiers. However, preamplifiers are required to provide buffering and sufficient signal swing beyond the latch offset. Due to noise limitations, preamplifiers often dominate the power consumption and, thus, should be optimized. In particular, an offset compensating latch can be used to ease the gain requirements of the less efficient linear stages. Feedback biasing, amenable to multi-step conversion, can be used to apply calibration to devices off the latch reset path [4].

The ADC shown in Figure 3(a) has a total power consumption of 25μW (in 12b mode at 100kS/s) [4]. In this design, the digital circuits actually consume slightly more power than the noise limited circuits, suggesting that the low V_{DD} has helped significantly to improve efficiency. Latch calibration has greatly eased the gain requirements of the preamplifiers reducing their power consumption to 5.8μW, an uncharacteristically low portion of the total ADC power.

Figure 3(b) shows that the ADC's power consumption goes down linearly with sampling rate in both 12b mode (where the maximum rate is 100kS/s) and 8b mode (where the maximum rate is 200kS/s). in 12b and 8b mode, the ADC achieves an SNDR of 65dB and 49dB respectively (at its Nyquist rate), and its SFDR is 71dB despite the low supply voltage.



(a) (b)

Figure 3: (a) ADC die photograph (b) Measured power consumption with respect to sampling rate.

3 DIGITAL SIGNAL PROCESSOR

Digital processing and memory circuits rely heavily on duty-cycling, necessitating careful design at architectural and circuit levels.

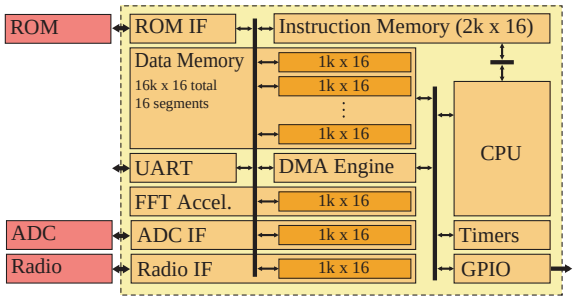


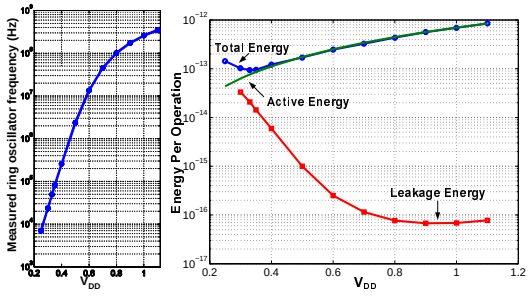
Figure 4: Architecture of an energy-efficient sensor DSP.

Figure 4 shows the architecture of an energy-efficient sensor node processor. It employs a custom CPU and instruction set to minimize the instruction memory footprint. Dedicated blocks for interfacing to the ADC and radio, as well as for performing complex algorithms, such as FFTs, handle common tasks much

more efficiently than CPU software. A DMA engine further reduces CPU load by efficiently moving data between the functional blocks and memory.

In addition to dedicated hardware, ultra-dynamic voltage scaling (UDVS) [5] is an effective technique in which supply voltage and frequency are varied together to optimize energy. A conventional DVS system operates at the lowest V_{DD} where throughput constraints are met. Without speed constraints, a UDVS system further reduces the supply voltage to the sub-threshold region where energy is minimized. The frequency versus V_{DD} characteristic of a UDVS test chip [5] is shown in Figure 5(a).

A minimum energy operating point, V_{DDopt}, exists because of two opposing trends when voltage is reduced. The dynamic energy of a circuit reduces according to CV_{DD}^2, as illustrated in Figure 5(b). However, the leakage energy of idle currents $I_{leak}V_{DD}T_D$ rises exponentially. This is due to an exponential increase in circuit propagation delay T_D caused by the rapid reduction in active currents as V_{DD} decreases. The net result is an optimum supply voltage that often lies below the transistor threshold voltage, V_T. This motivates the design of robust digital circuits capable of operating in the sub-threshold region.



(a) (b)

Figure 5: Effect of V_{DD} scaling on (a) frequency and (b) energy.

Because sub-threshold currents are exponentially dependent on threshold voltage, process variation affecting V_T significantly impacts circuit functionality and performance. To ensure functionality, active currents in a logic gate must be strong enough to overcome parallel leakage paths across process corners. Furthermore, large delay variability, an example of which is shown in Figure 6, must be carefully analyzed during timing verification. A 180mV FFT processor in [6] has shown that static CMOS is generally the most robust against variation in sub-threshold logic.

Memory, however, poses a challenge since the traditional 6T SRAM cell relies on transistor sizing ratios for proper functionality. Ratioed circuits are much more sensitive to variation in sub-threshold because currents vary only linearly with sizing but exponentially with V_T. In particular, random V_T mismatch can

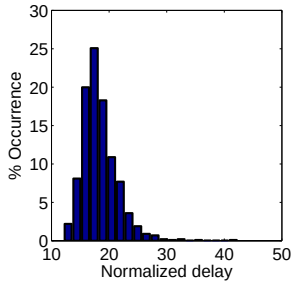
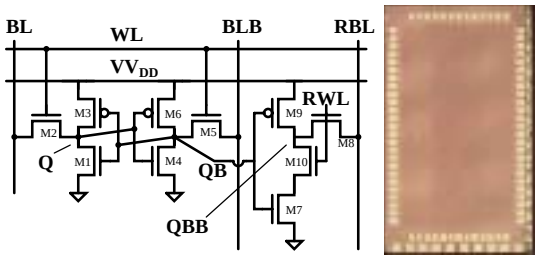


Figure 6: Delay distribution of 8-bit static CMOS adder at 0.3V due to V_T mismatch.

cause a 6T bit-cell to have negative read static noise margin (read SNM), implying the stored data will be destroyed during a read. This imposes a limitation on the minimum operating voltage of the SRAM.



(a) (b)

Figure 7: 10-transistor bit-cell (a) and die photo (b) of a 65nm sub-threshold memory.

The 10T bit-cell in [7] enables aggressive supply voltage scaling, which is especially beneficial since memory typically accounts for a large portion of the total design and consumes significant leakage power. This bit-cell obviates the read SNM problem by using a 4T buffer (M7-M10 in Figure 7(a)) to isolate the storage node during a read access. Furthermore, a robust write is achieved by floating the virtual V_{DD} rail, VV_{DD}, so that the access transistors M2 and M5 can reliably overpower the storage transistors M1, M3, M4, and M6. This bit-cell is incorporated in the 256-kbit, 65nm memory of Figure 7(b), which functions down to 400mV and consumes 3.28μW at a speed of 475kHz.

4 RADIO

Due to their high frequency of operation and wide bandwidth, RF circuits in a radio typically consume milliwatts of power and dominate the power budget of a wireless micro-sensor node. To achieve microwatt average power consumption and optimal energy efficiency, a radio can be duty cycled by operating at a high instantaneous data rate and turning off the radio periodically. To realize an energy efficient duty cycled radio, it is important that the idle to active startup time is minimized.

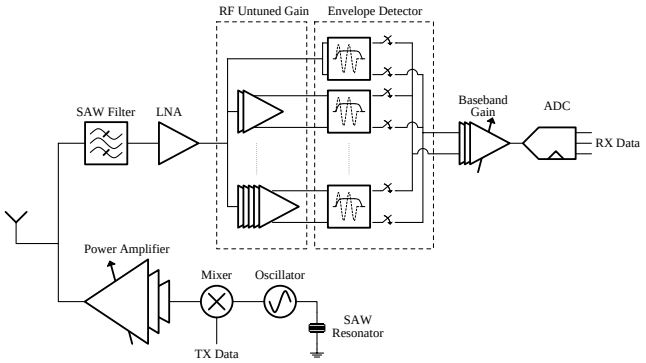


Figure 8: Architecture of proposed transceiver

A key metric for measuring the energy efficiency of the transceiver is *energy per bit*, which is equal to the power consumption of the transmitter or receiver divided by the instantaneous data rate. The radio in [8] achieves energy per bit ratios down to 0.4 nJ/bit in receive mode and 3.8 nJ/bit in transmit mode, the lowest demonstrated ratios in its class of low-power, short range radios. These low ratios, combined with a fast receiver startup time of 2.5 μs, allow for energy efficient operation.

A block diagram of the transceiver is shown in Fig. 8 [8]. The RF front end supports several gain settings, so that the power consumption of the receiver can be reduced in the presence of large input signals. The transmitter supports 7 digitally controlled output power levels to enable power scaling based on node proximity.

The transceiver operates in a single channel centered at 916.5 MHz and employs on-off keying (OOK) modulation. A non-coherent, envelope detection receiver architecture removes the need for a local oscillator and allows for a fast receiver startup time. OOK is well suited for energy efficient short-range wireless links where circuit power consumption is often greater than the transmitted output power [9].

The receiver power consumption scales from 0.5 mW to 2.6 mW, with an associated sensitivity ranging from -37 dBm to -65 dBm at a bit error rate of 10^{-3}. The transmitter supports output power levels from -11.4dBm to -2.2dBm.

5 CONCLUSION

Micro-sensor nodes can self-organize into a collaborative network and operate autonomously, offering a truly disruptive advantage in intelligent observation. This paper offers demonstrated examples of how the characteristics of minimum energy operation, duty-cycling, and scalability can be achieved in the ADC, DSP, and radio circuits. Considerations are required at all levels of design from energy-aware architectures to efficient circuits. A comparator based ADC that can operate at low voltages and be efficiently disabled, allows scalable and low-energy data conversion. Dedicated and scalable digital hardware, along with dynamic voltage scaling into the sub-threshold regime, enable efficient and reconfigurable digital signal processing. Finally, variable sensitivity and simple modulation optimize power consumption and enable agile duty-cycling in the radio.

ACKNOWLEDGMENTS

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