Low Voltage System Design for Highly Energy Constrained Applications

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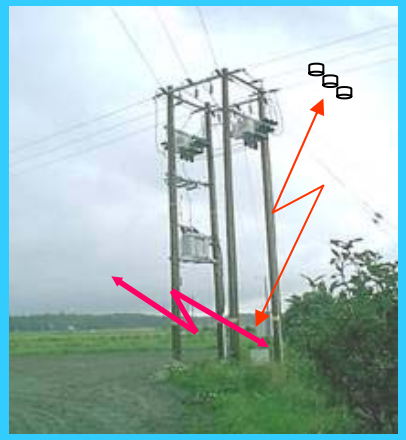
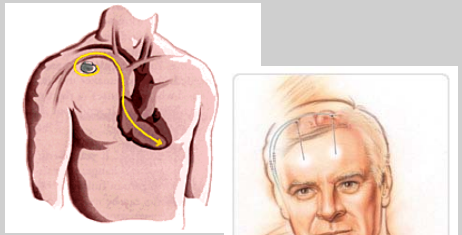
FTFC 2008

Emerging Microsystems

Industrial Plants and Power Monitoring (courtesy ABB)



Implantable Medical Electronics [Medtronic]



Portable Medical Electronics

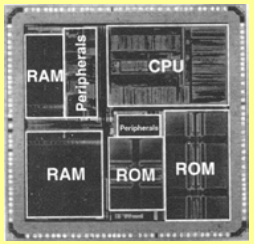
Seizure Onset Detection System [J. Guttag, MIT]

The Energy Problem

7.5 cm³ AA battery

Alkaline: ~10,000J

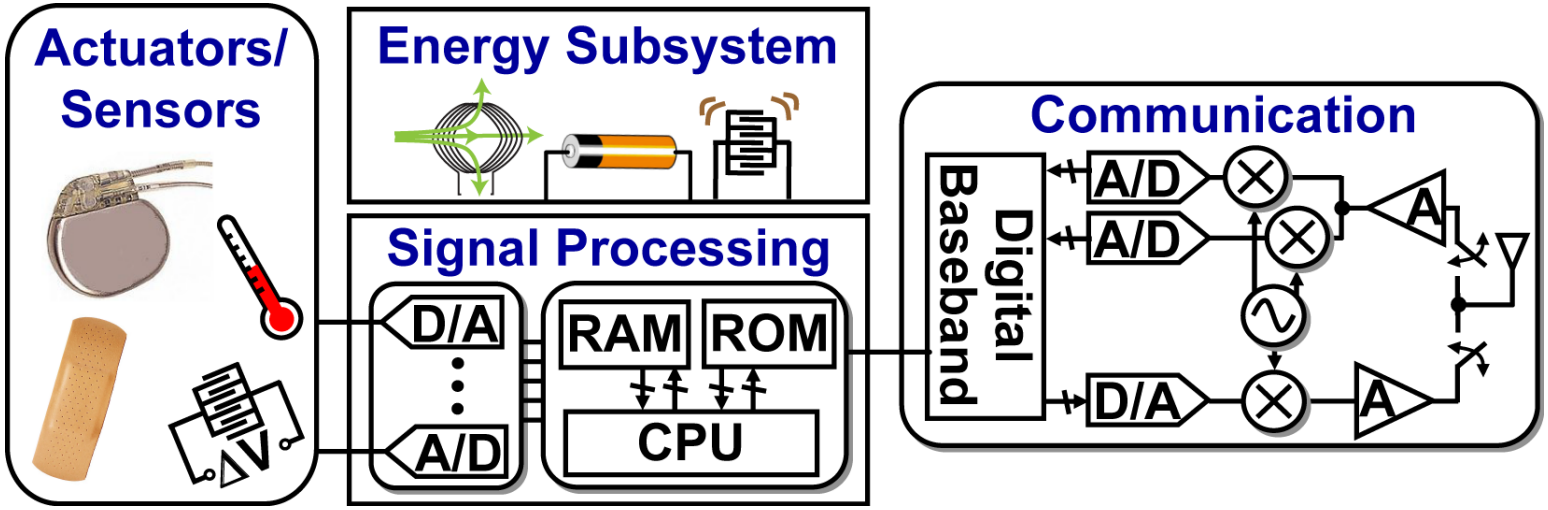
What can One Joule of energy do?



6 Billion Operations on a C55x DSP

Send a 1 Megabyte file over 802.11b

Integrated Sensor Nodes



- Compact Form Factor (mm^3 – cm^3)
- Energy dissipation per function must be minimized
  - Average power < 10μW (for energy scavenging)
- For many embedded applications, computing speed is not critical

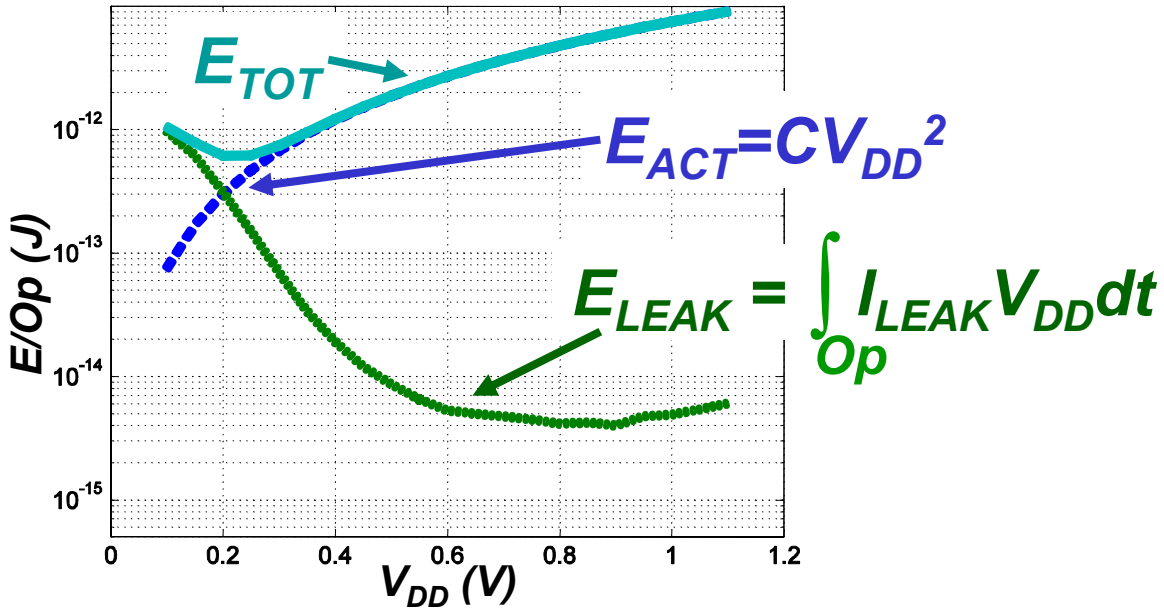
Exploit Application Attributes to Minimize Energy

Outline

- Voltage scaling
  - Advantages, challenges
- Ultra-low-voltage computing
  - Logic
  - SRAM
  - Power delivery and processing
- Low-energy CPUs
- Low-energy ADCs
- Conclusions

Voltage Scaling

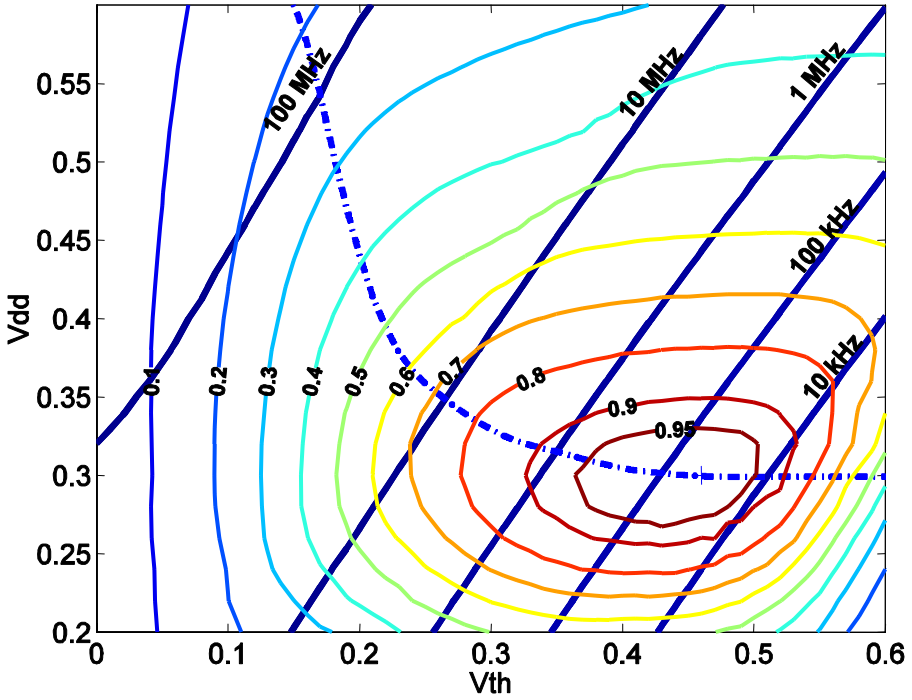
Simulation of 32-b CLA adder



Minimum energy V_{DD} for logic results from opposing active and leakage components

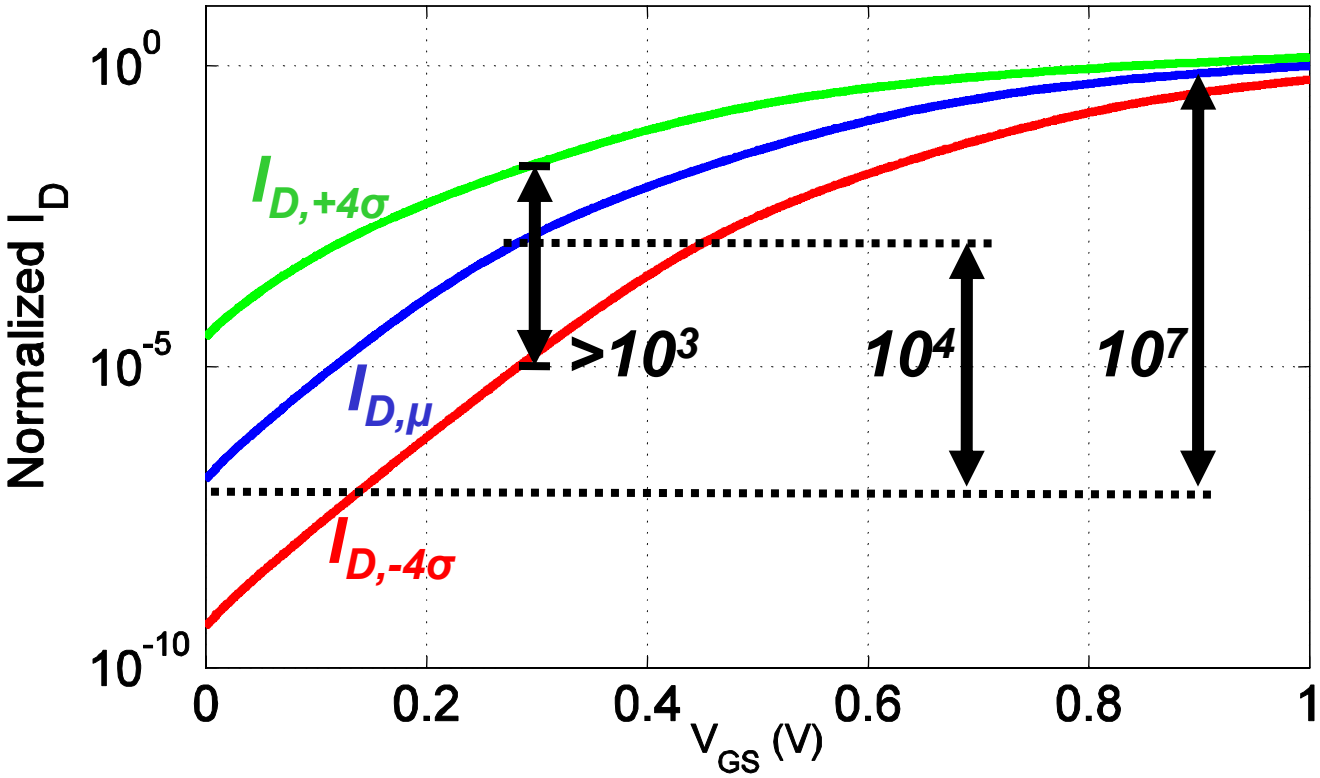
Optimal V_{DD} and V_t

V_{DD} and V_t yield <u>contours</u> of constant energy and performance



Full minimization of energy requires V_{DD} <u>and</u> technology optimization (V_t, slope, etc.)

ULV MOSFET Degradations



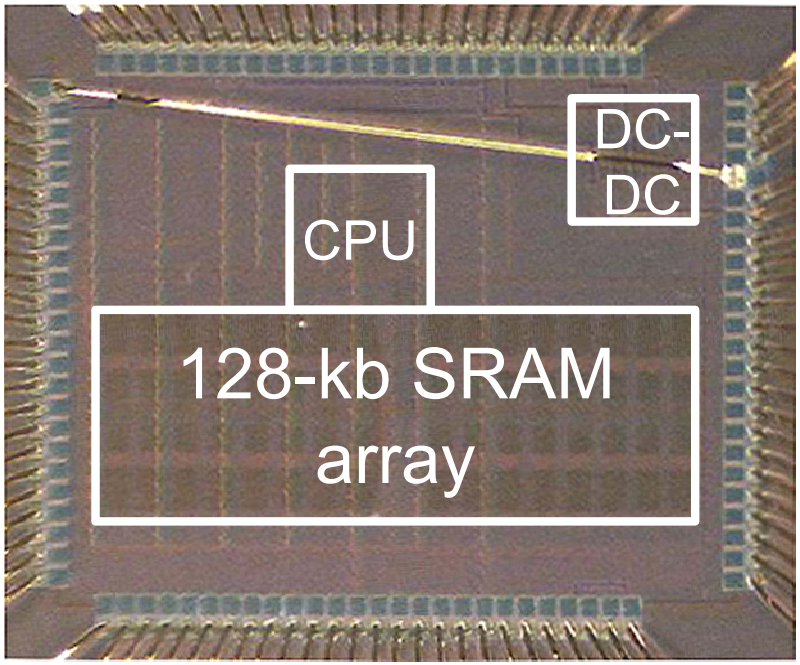
In Sub-V_t:

1) V_t variation exponentially affects strength

2) I_{ON}/I_{OFF} is severely degraded

ULV Computing Platform

Ultra-low-power DSP for bio-medical implants and sensor-nodes



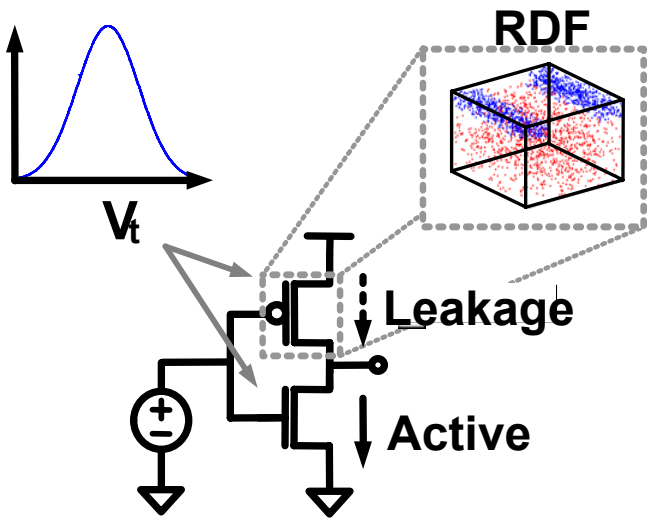
0.3V MSP430 SoC

1) Sub-V_t Logic
2) Sub-V_t SRAM
3) Integrated DC/DC

Specialized techniques target severe variation and current-ratio with minimum overhead

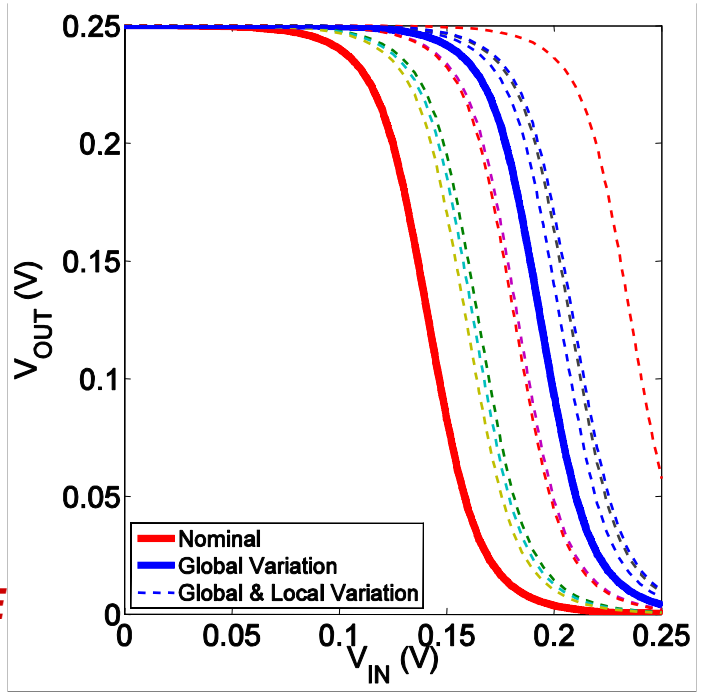
Sub-V_t Logic Level Failure

1) V_t variation

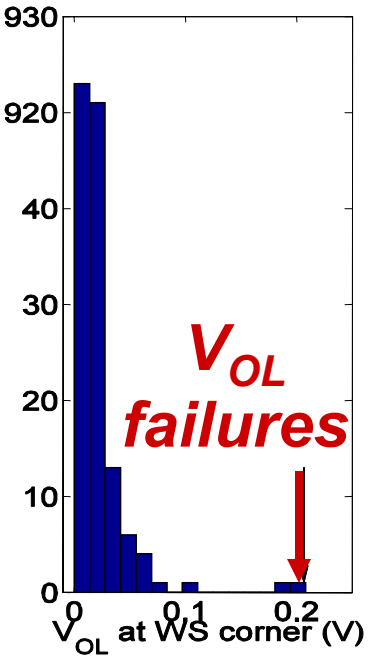


2) $I_{ACTIVE} \approx I_{LEAKAGE}$

Inverter VTC



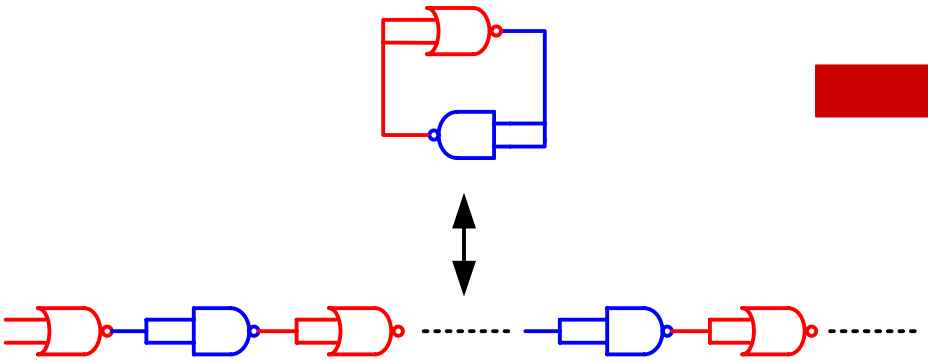
V_{OL} Histogram

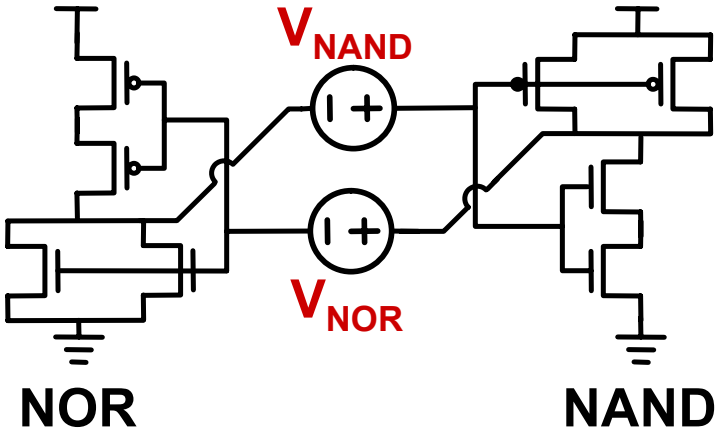


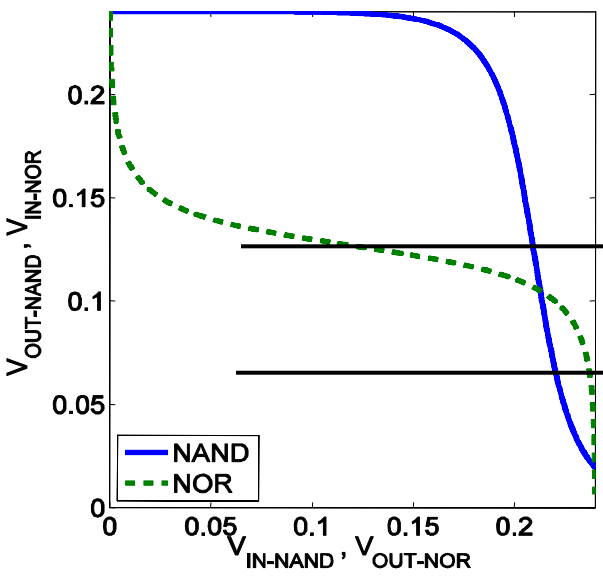
Sub-V_t static CMOS gates exhibit variation in logic levels (V_{OH}, V_{OL})

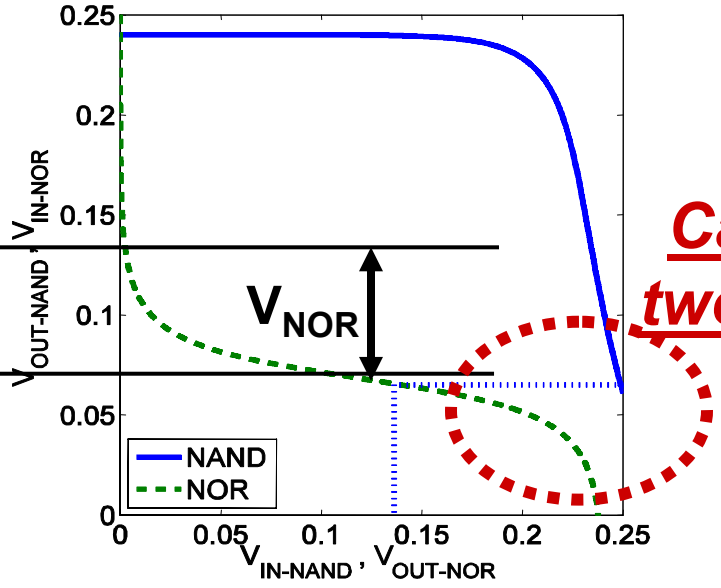
Sub-V_t Library Design

Model worst-case logic path







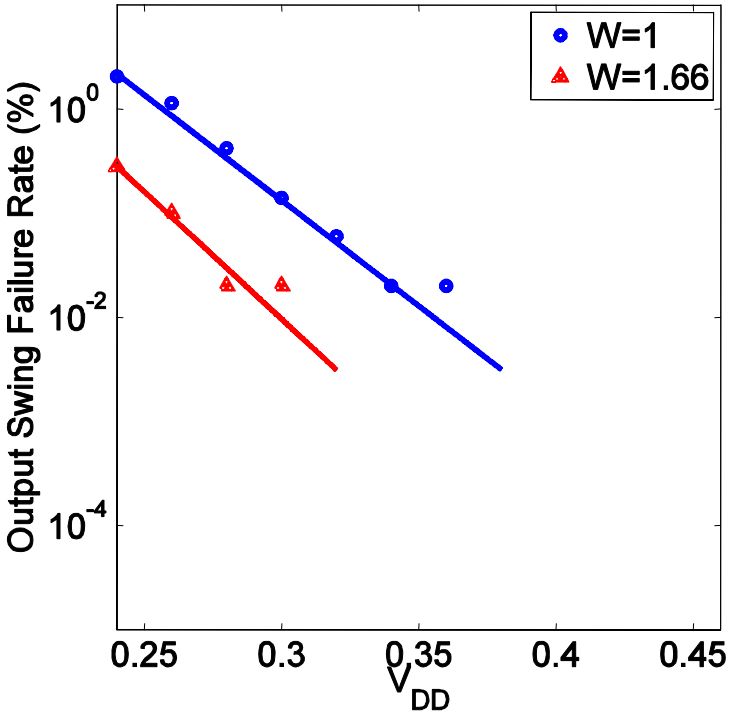


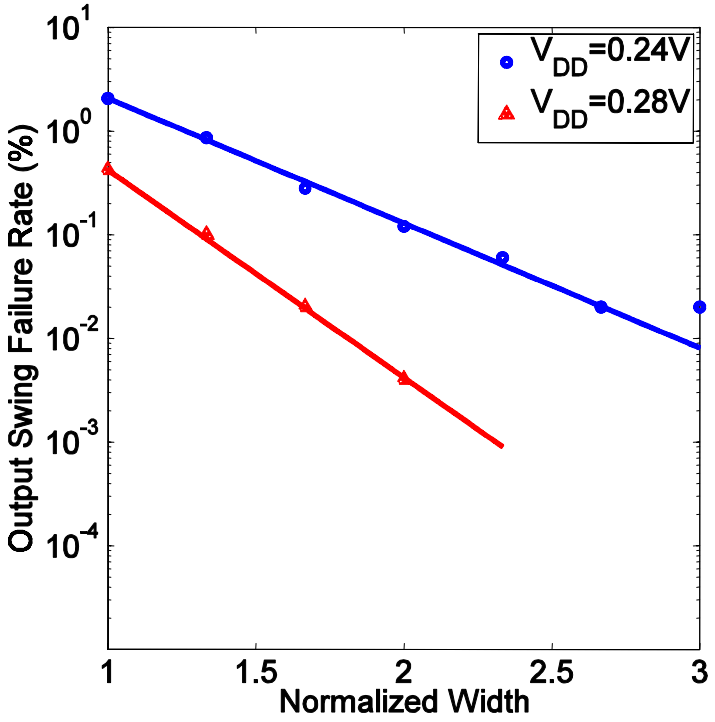
Can't support two logic levels

[J. Kwong, et al. ISLPED'06]

Sub-V_t Library Design

Define failure as loss of butterfly plot intersections

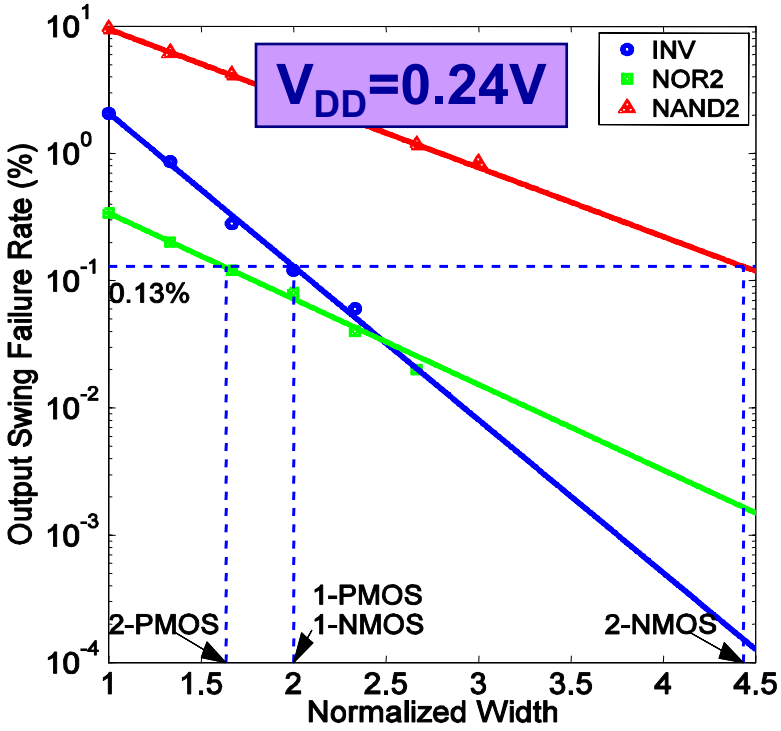




Failure rate decreases exponentially with device width and V_{DD}

Sub-V_t Library Design

- Find failure rate vs. width plots for different circuit primitives
- Keep device sizes as small as possible, subject to yield constraint

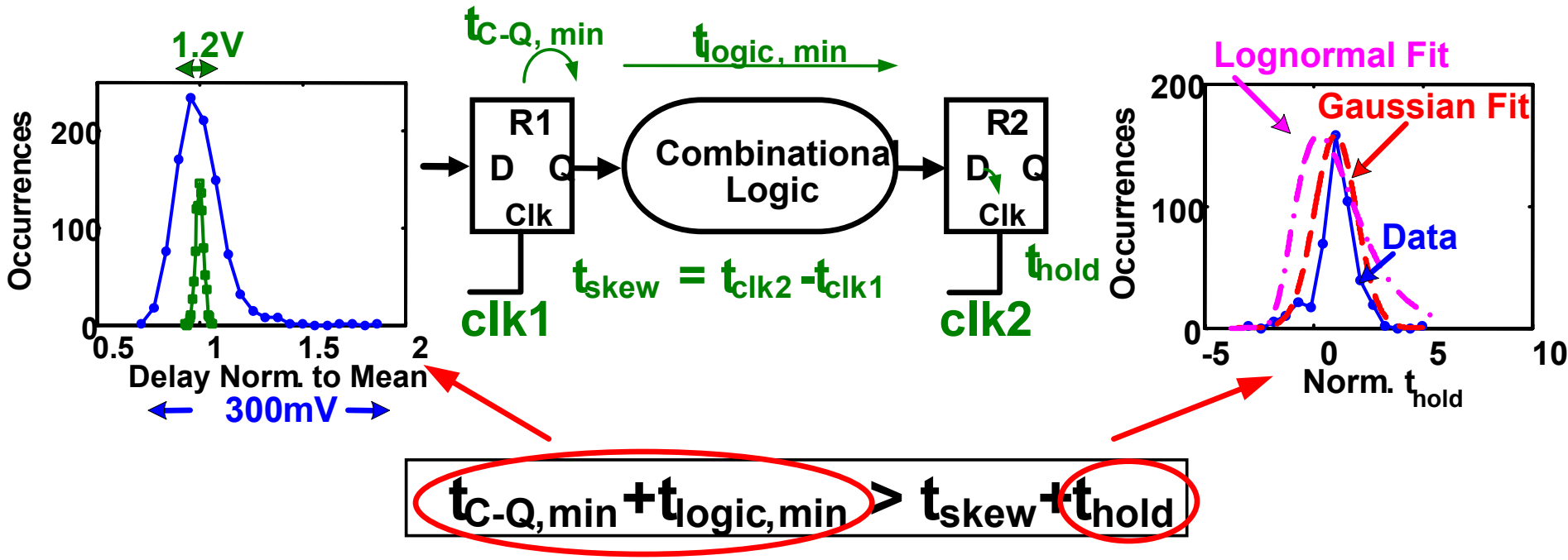


Width Increase:

V_{DD}(V)	0.24	0.26	0.28	0.30	0.32	0.34
1-NMOS	2	1.67	1.33	1	1	1
1-PMOS	2	1.67	1.33	1	1	1
2-NMOS	4.43	2.93	2.3	2.27	1.3	1
2-PMOS	1.63	1	1	1	1	1

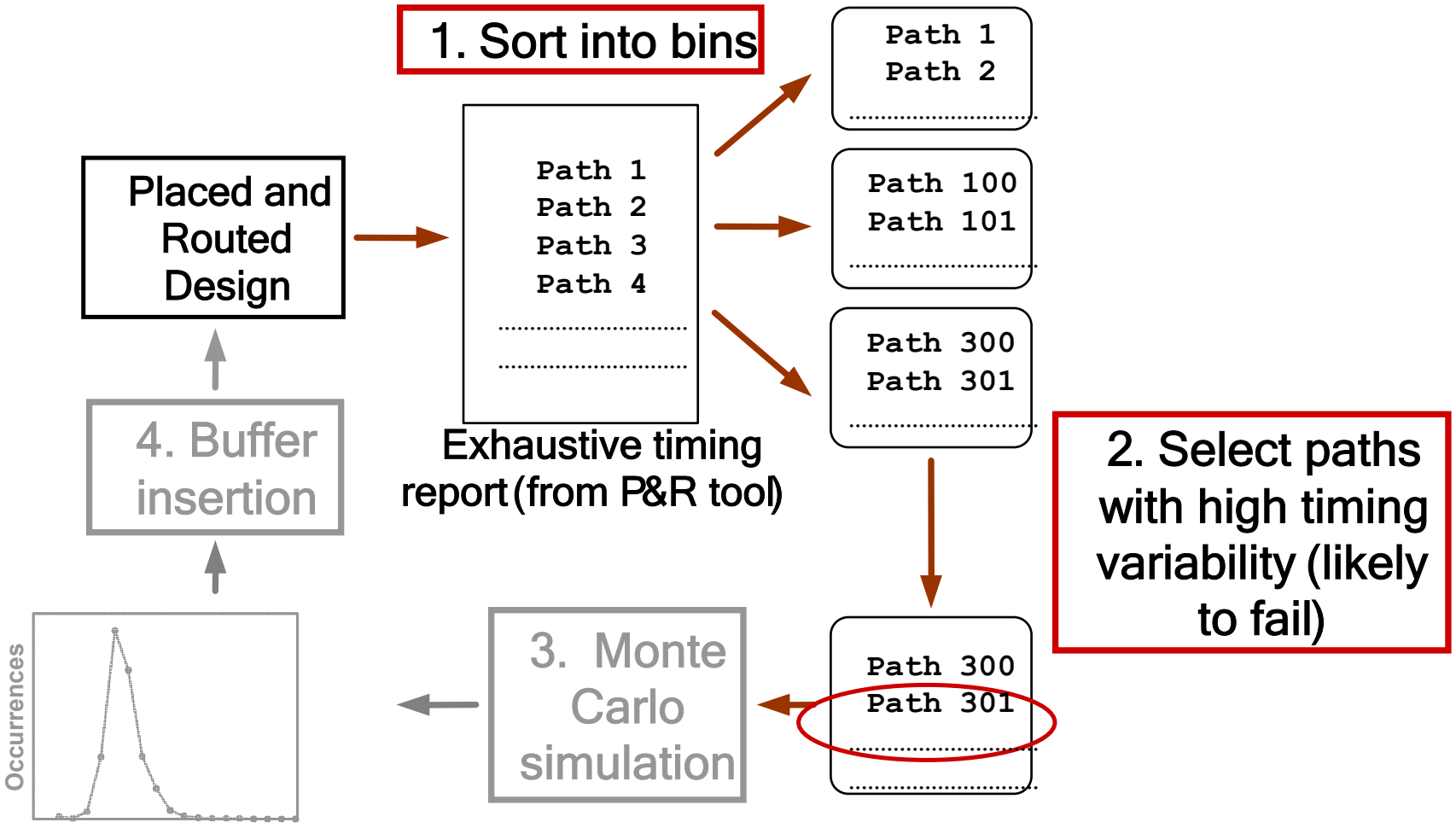
Sub-V_t Timing Analysis - Challenges

Order-of-magnitude higher delay variation in sub-V_t

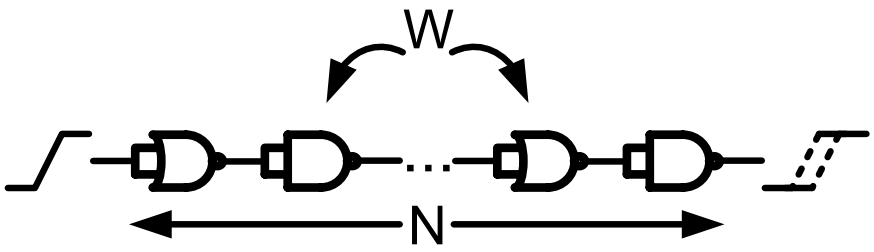


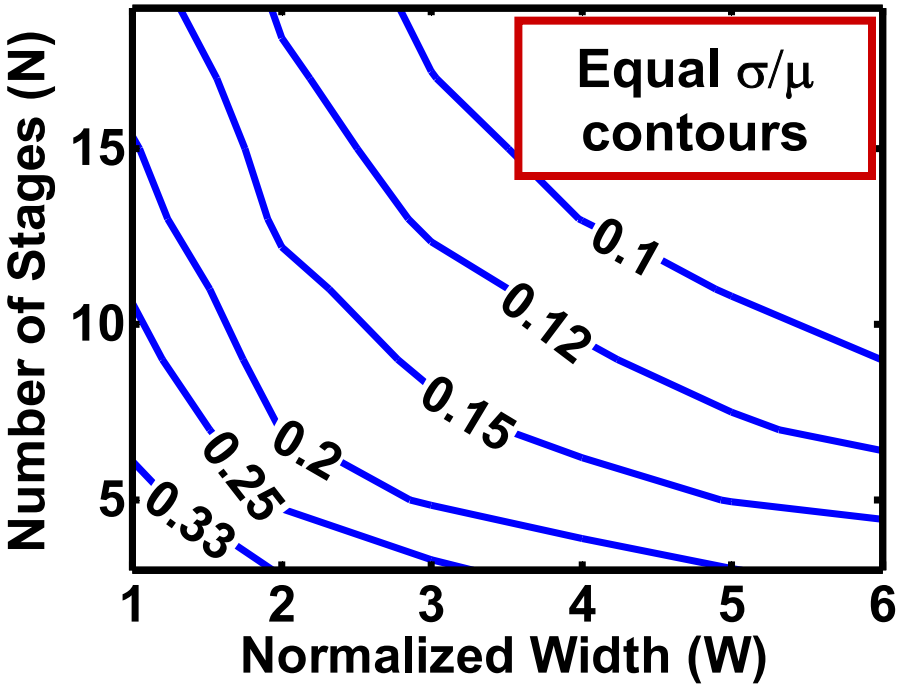
STA Methodology

Focus on hold time violations



Determining Path Variability



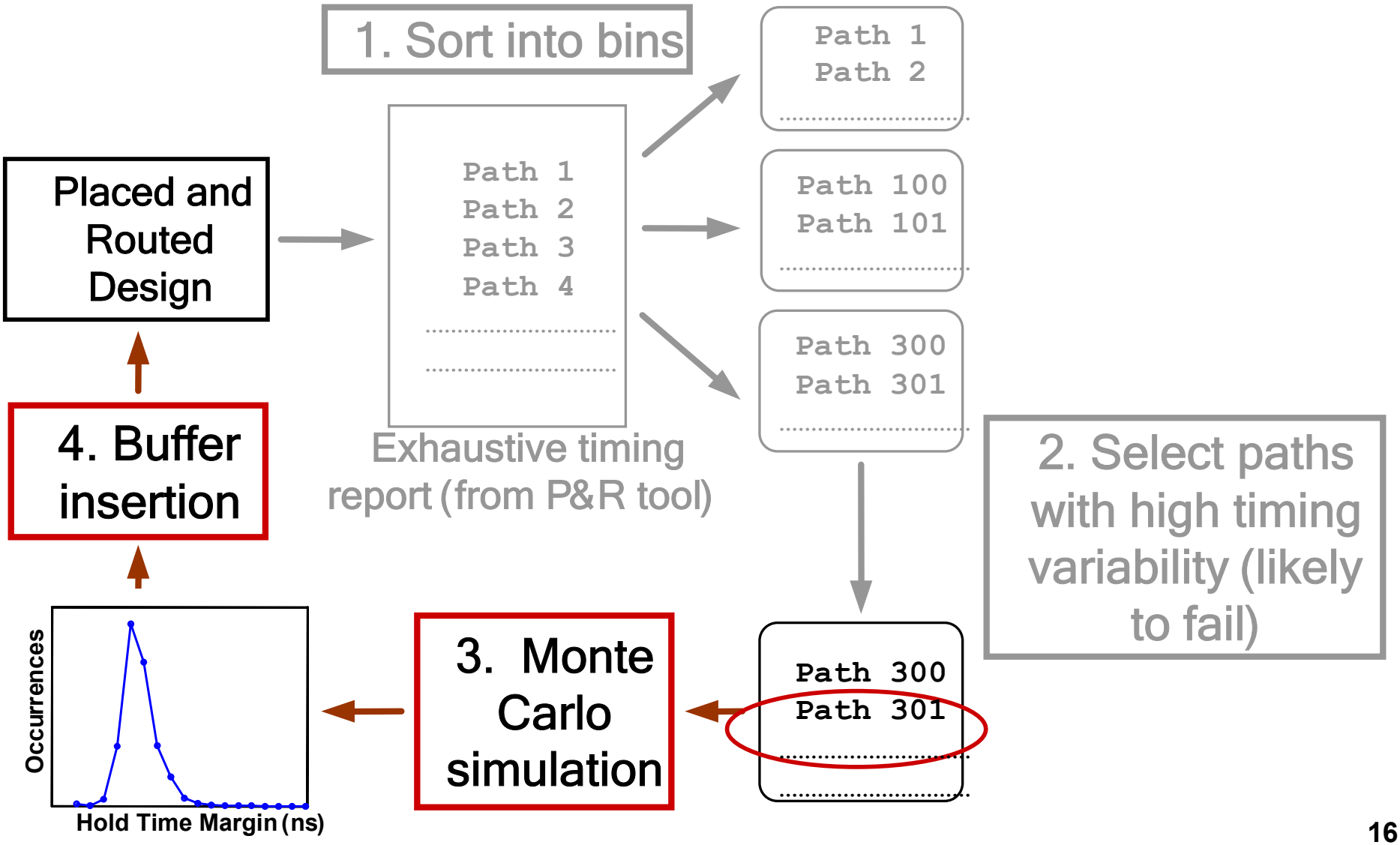


Path variability metric:

(1) Sum σ/μ of all logic gates in path

(2) Assign weighting to each path according to logic depth

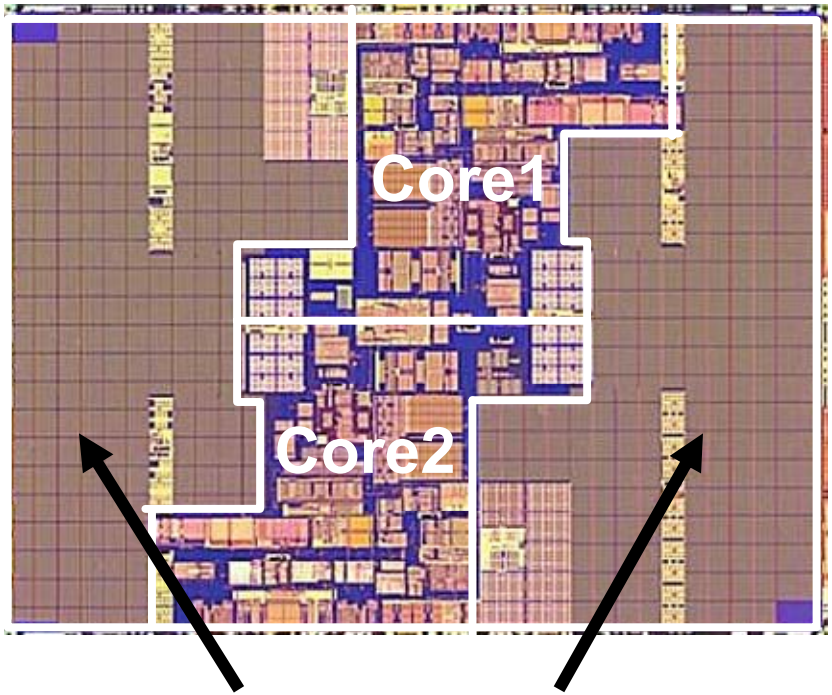
STA Methodology



SRAM Power Consumption

SRAMs can't be power-gated: leakage-power matters

90nm 2-Core Itanium

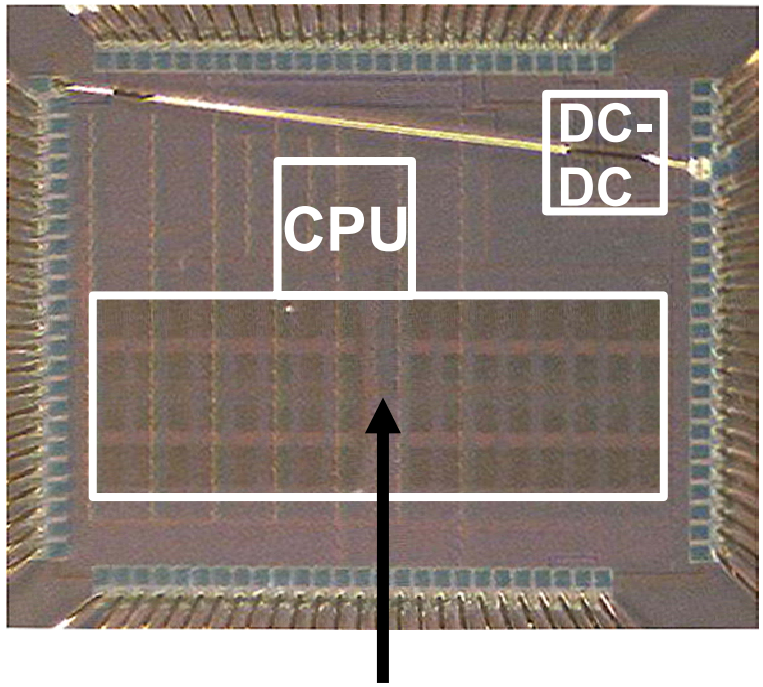


26MB SRAM cache

Power: 12%

[J.Wuu, et al. *ISSCC*, 2005]

65nm 0.3V MSP430



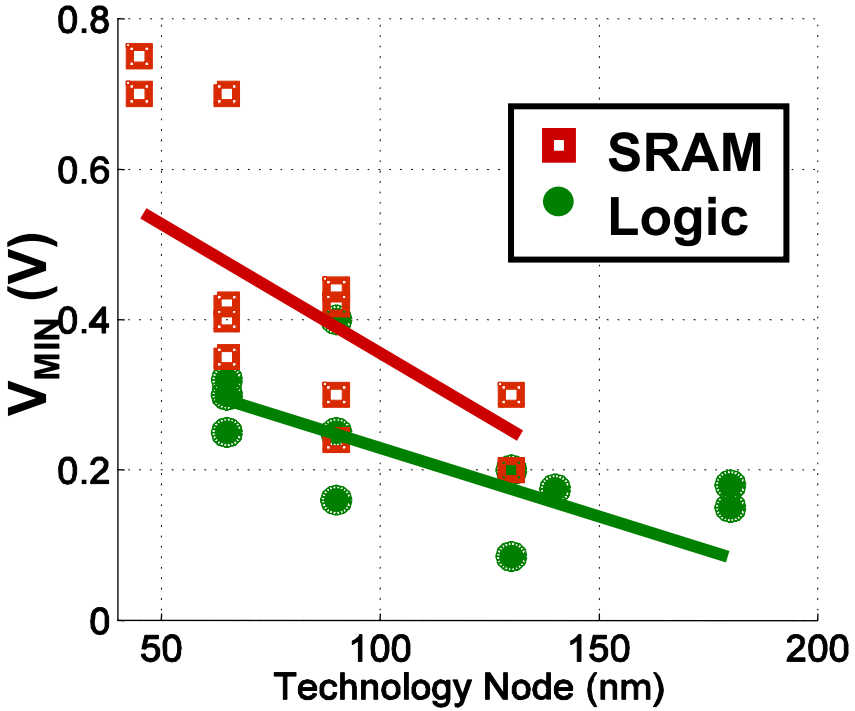
128kb SRAM cache

Power: 69%

[J.Kwong, et al. *ISSCC*, 2008]

SRAM Voltage Scaling

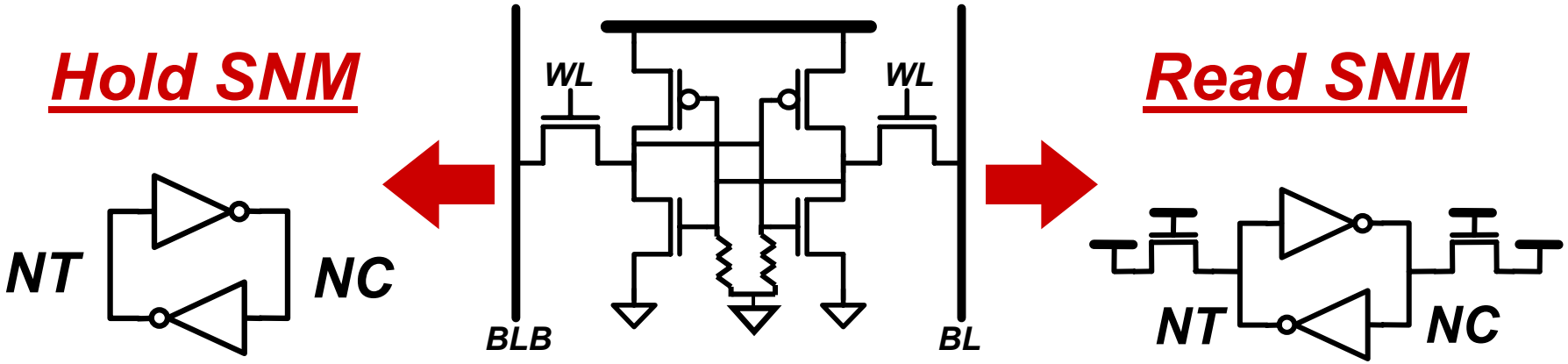
Low-V_{MIN} SRAMs provide major leakage-power savings (>20x) <u>without active-energy overhead of sleep modes</u>



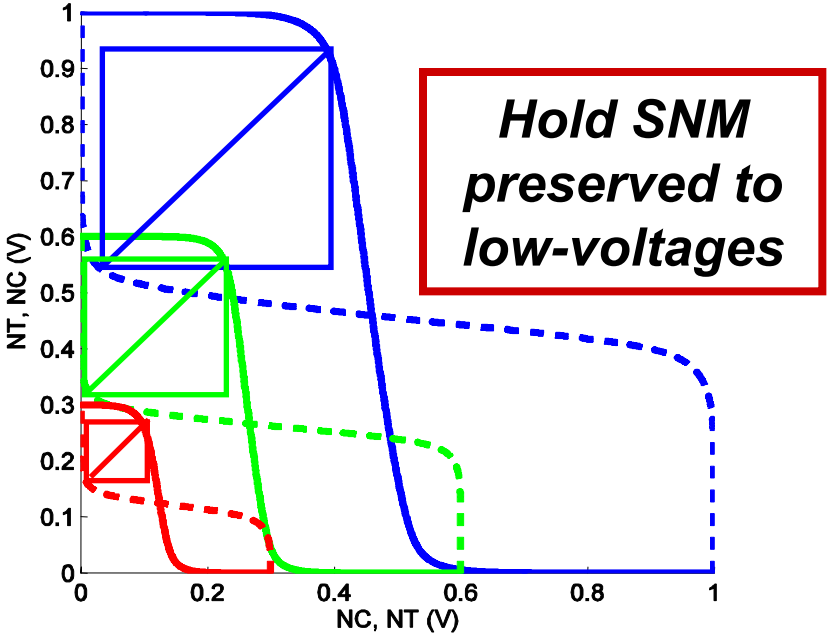
[*ISSCC, JSSC, VLSI, CICC, ISLPED* `02-`07]

SRAMs pose primary limit to voltage scaling

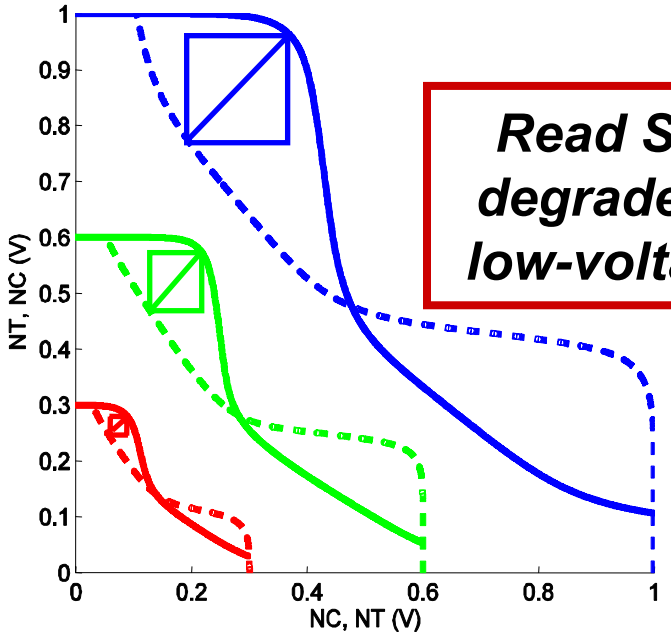
SRAM Bit-Cell Stability



*Soft-oxide breakdown further distorts curves



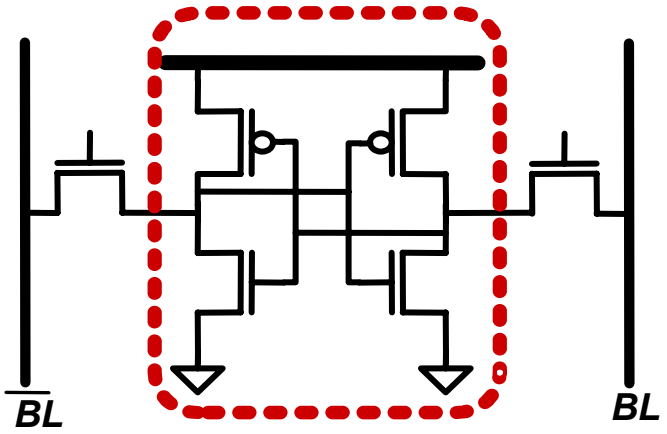
Hold SNM preserved to low-voltages

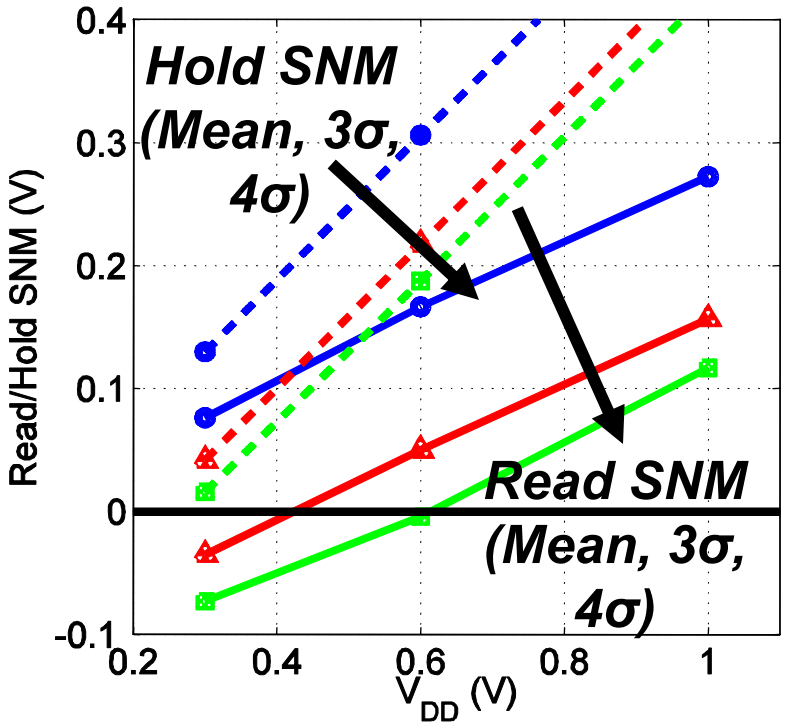


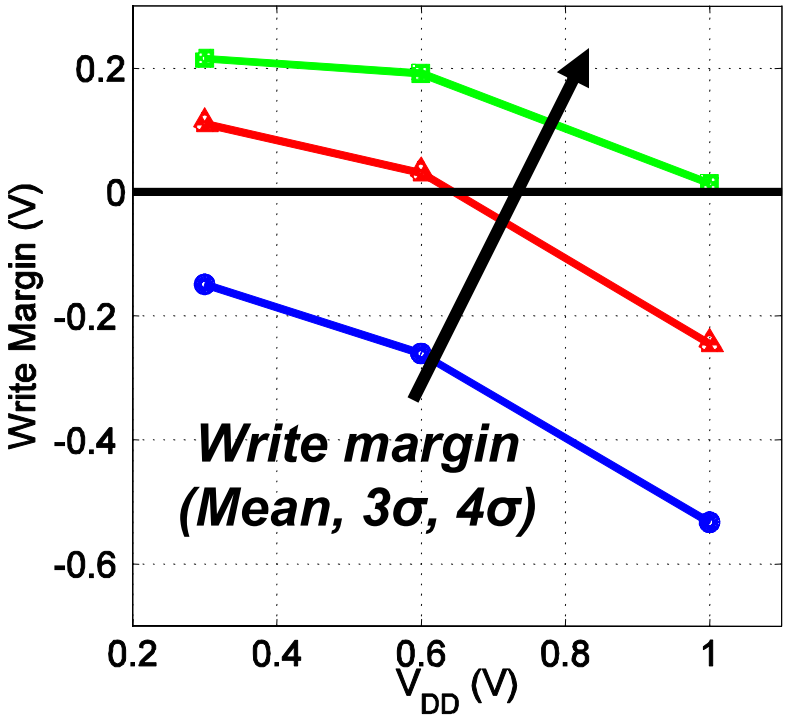
Read SNM degraded at low-voltages

6T Low Voltage Failures

Relative device strengths determine readabilty/writeability

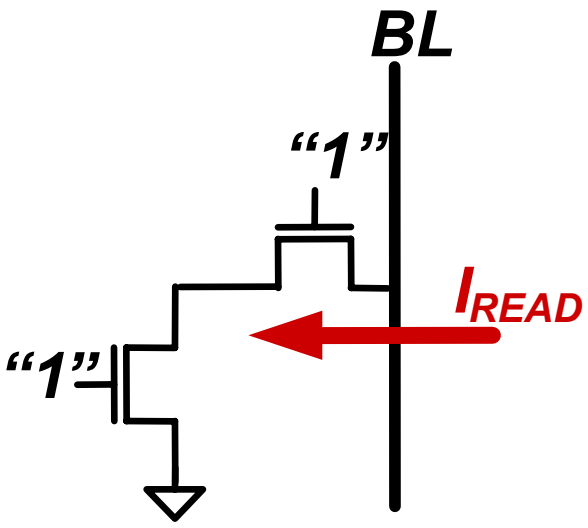


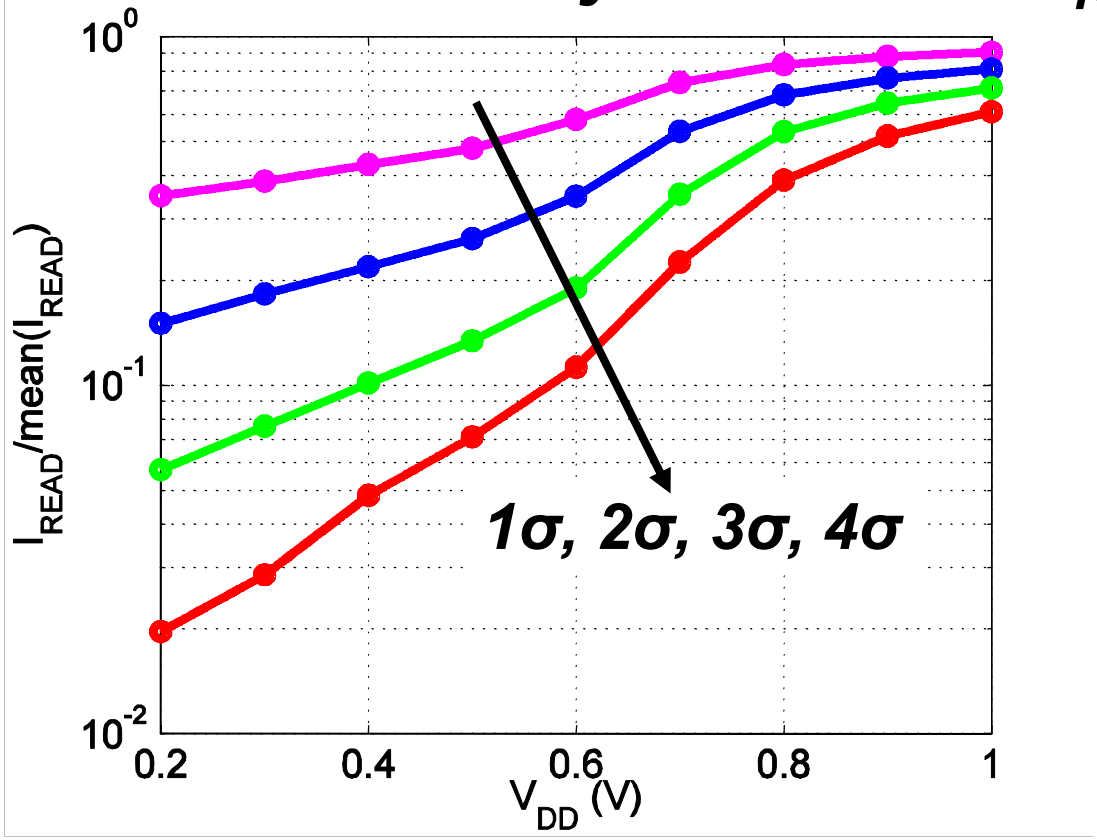




Read Current Distribution

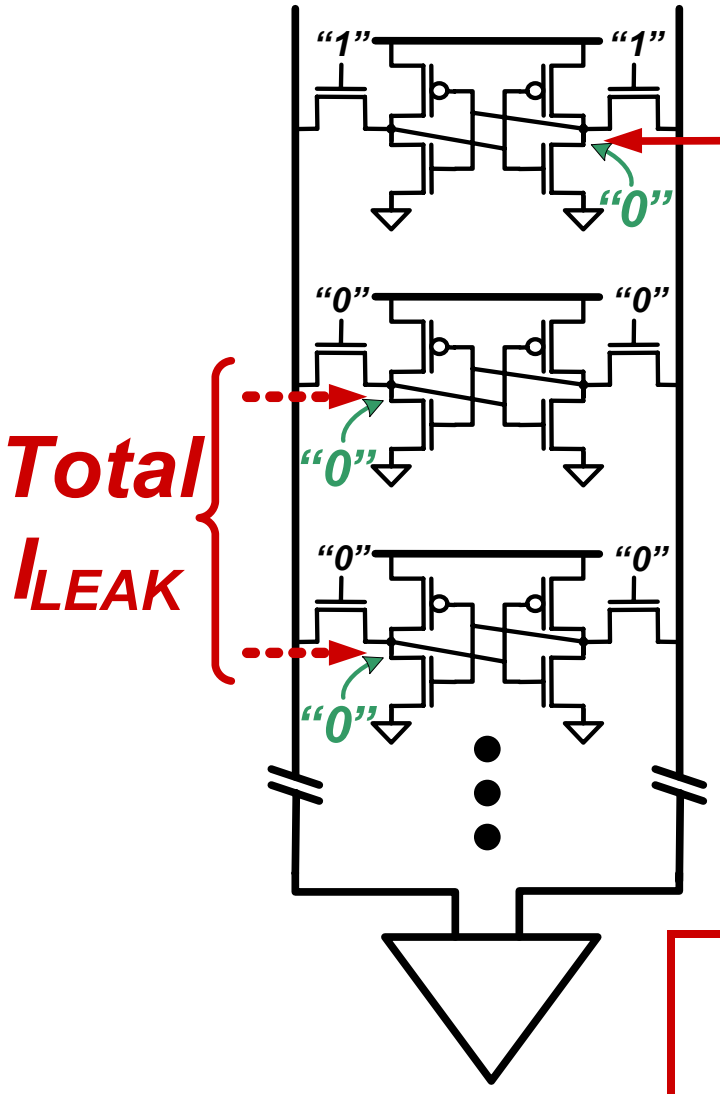
Array performance determined by worst-case I_{READ}

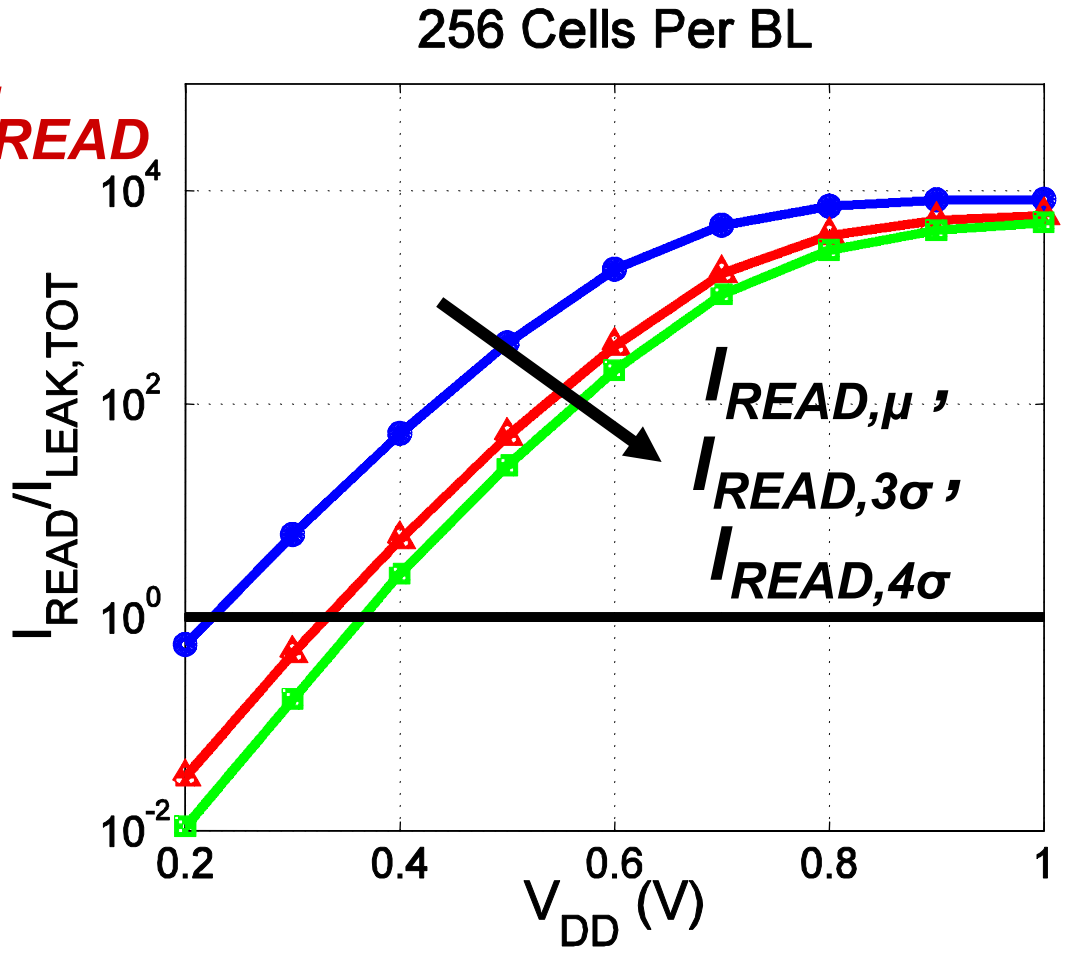




In sub-V_t, reduced overdrive lowers mean I_{READ}, and variation causes larger degradation of tail I_{READ}

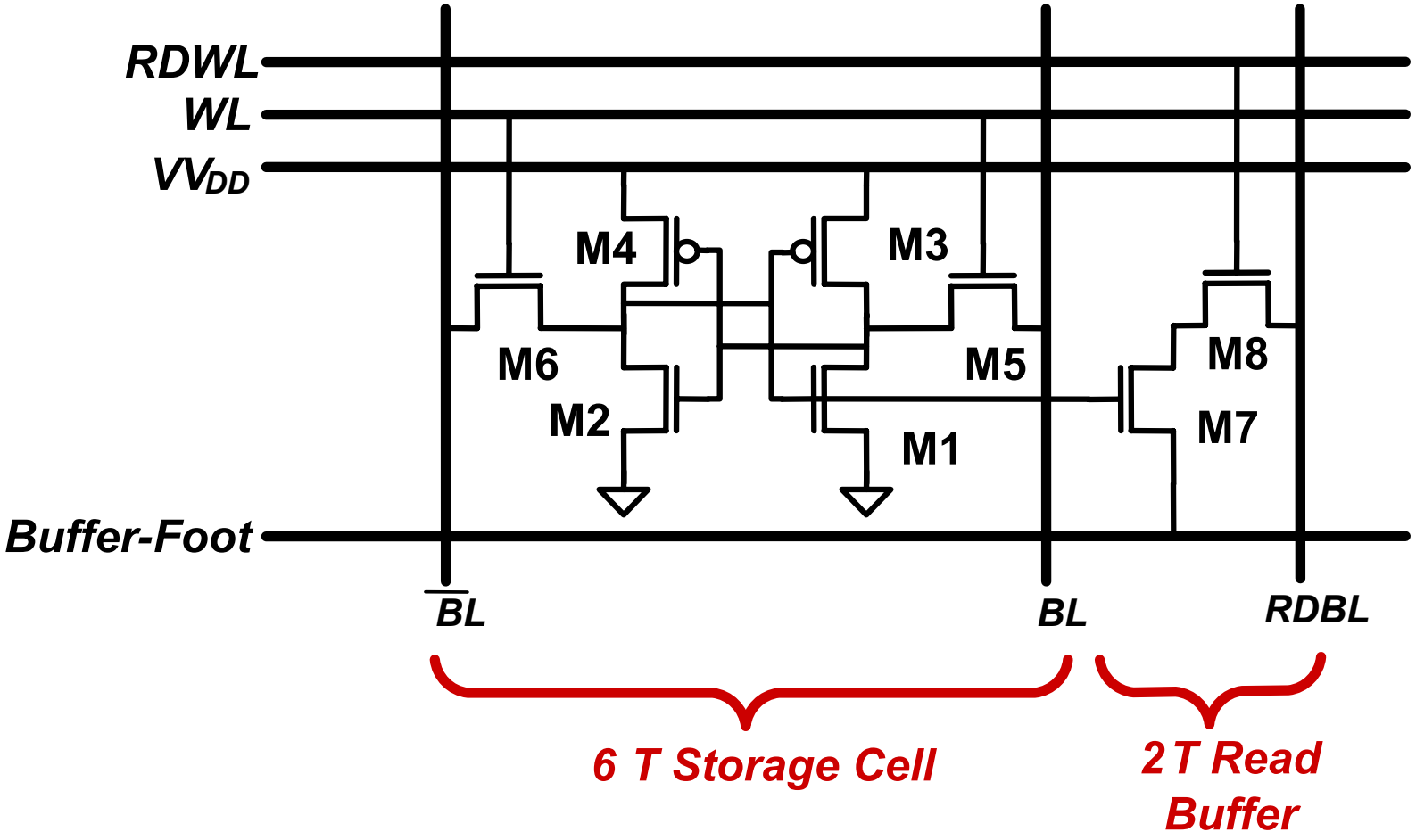
Bit-Line Leakage





I_{LEAK} depends on stored data and can exceed I_{READ} at low voltages

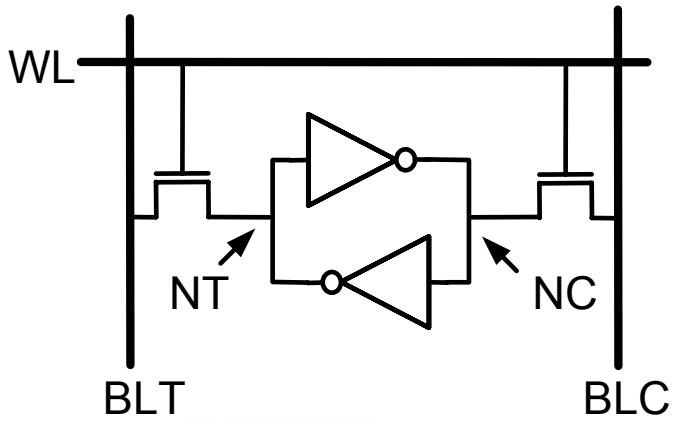
8T Bit-Cell For Sub-Vt SRAM

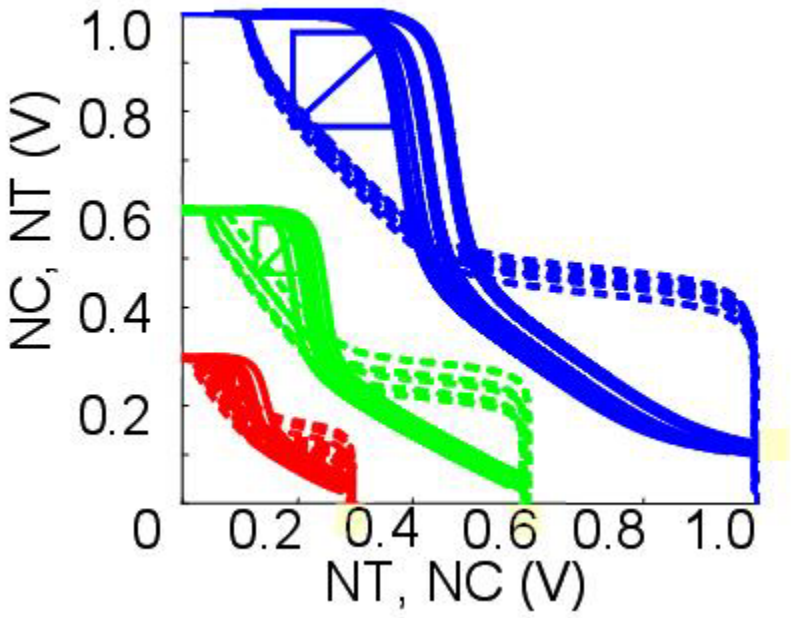


Buffer eliminates read SNM limitation, peripheral assists allow sub-V_t write and sensing

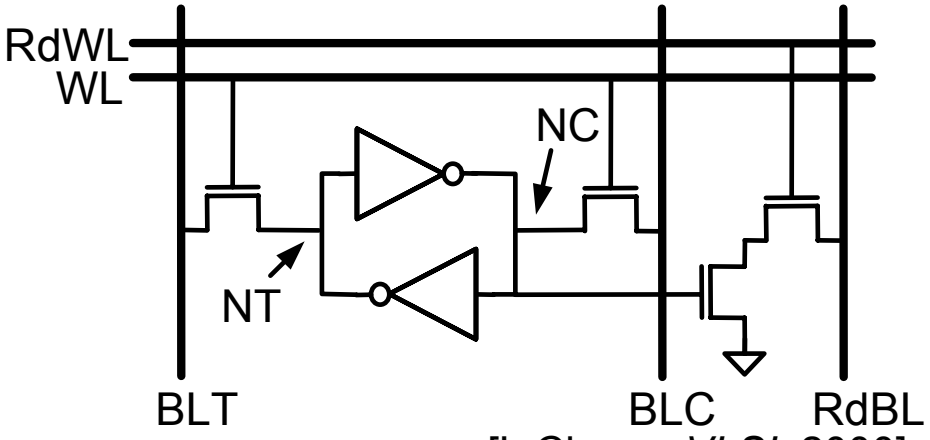
8T vs. 6T for ULV

6T: Fails at low V_{DD}

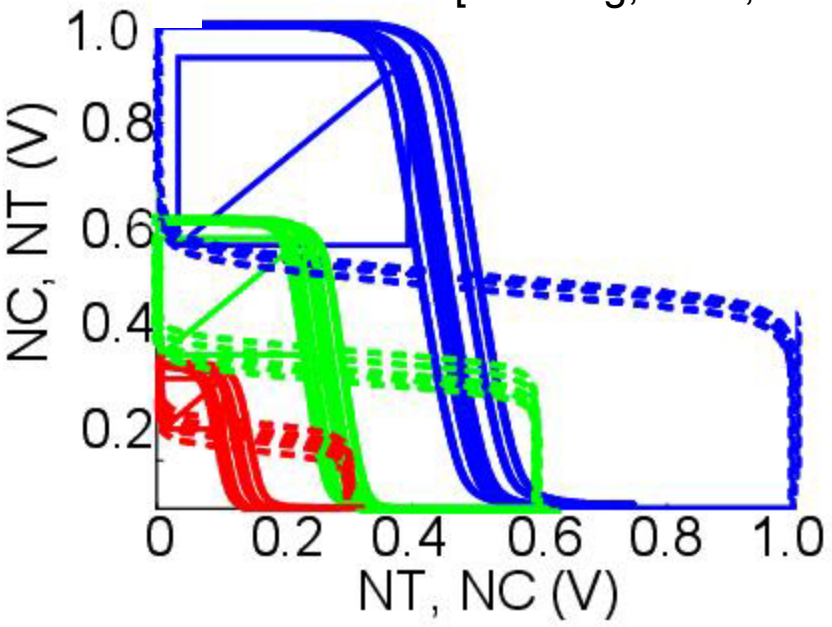




8T: Wide margins at low V_{DD}

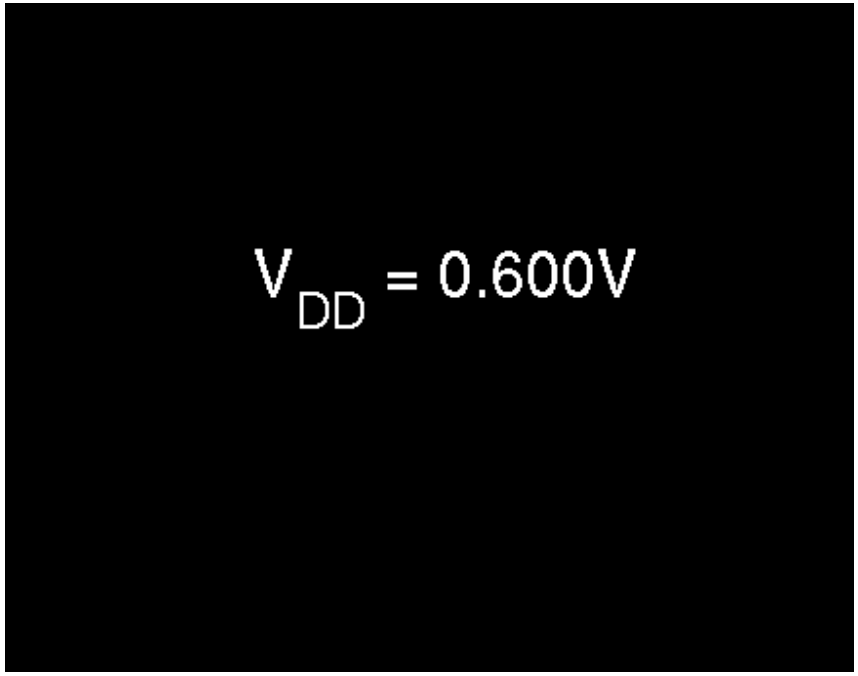


[L.Chang, *VLSI*, 2000]



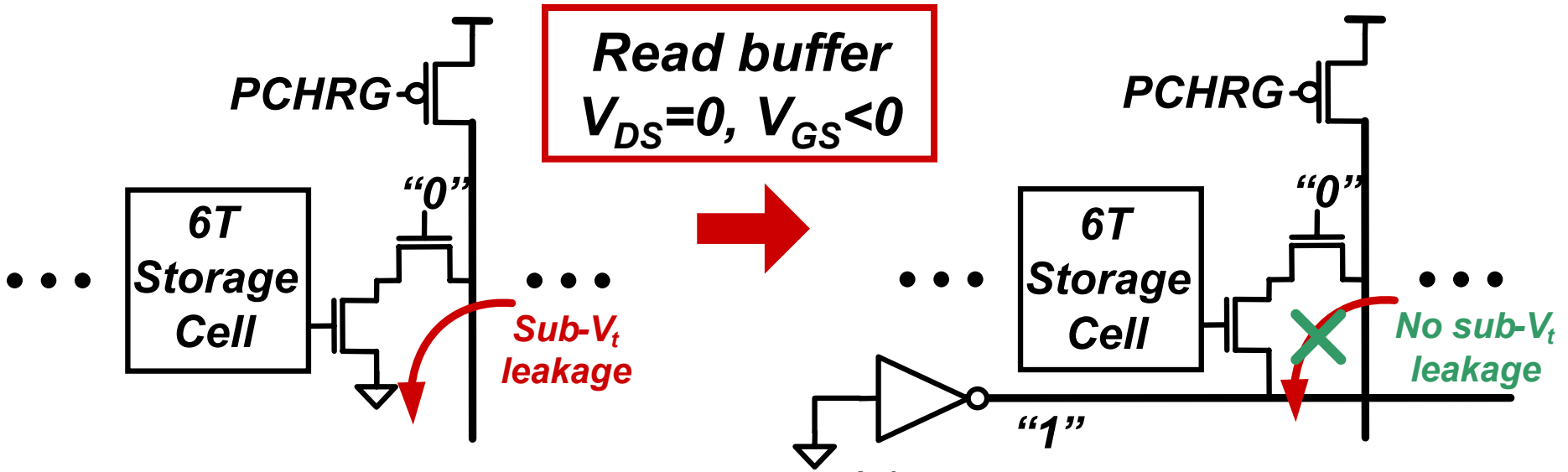
8T vs. 6T for ULV

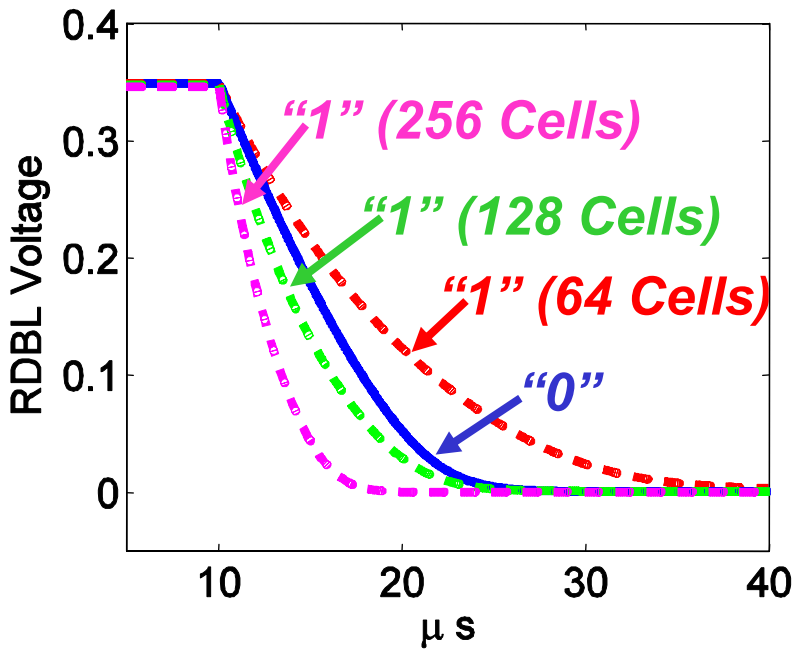
Single-bit read failures for equal sized 6Tand 8T

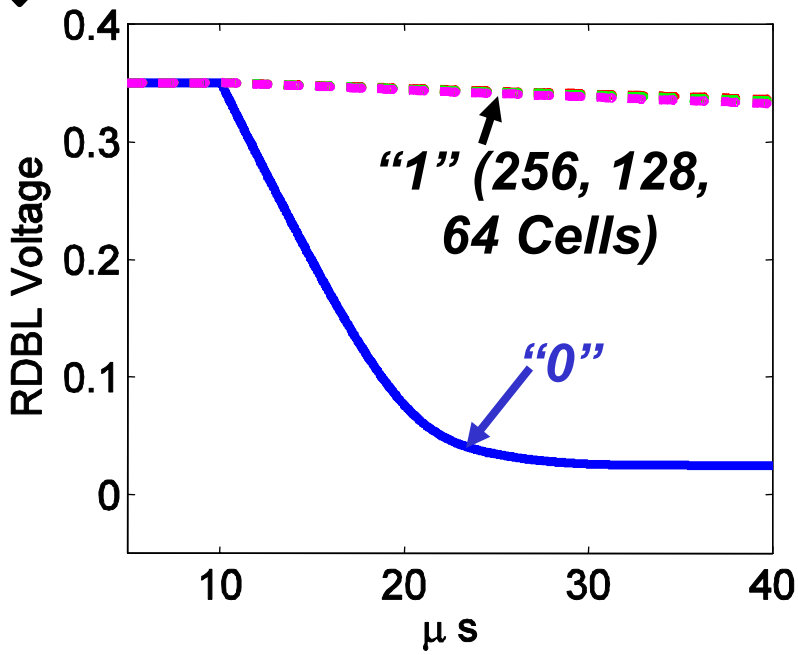


<u>For same area</u>, $V_{DD,MIN}$ goes from 0.6V to 0.3V: Leakage power goes down by 8X

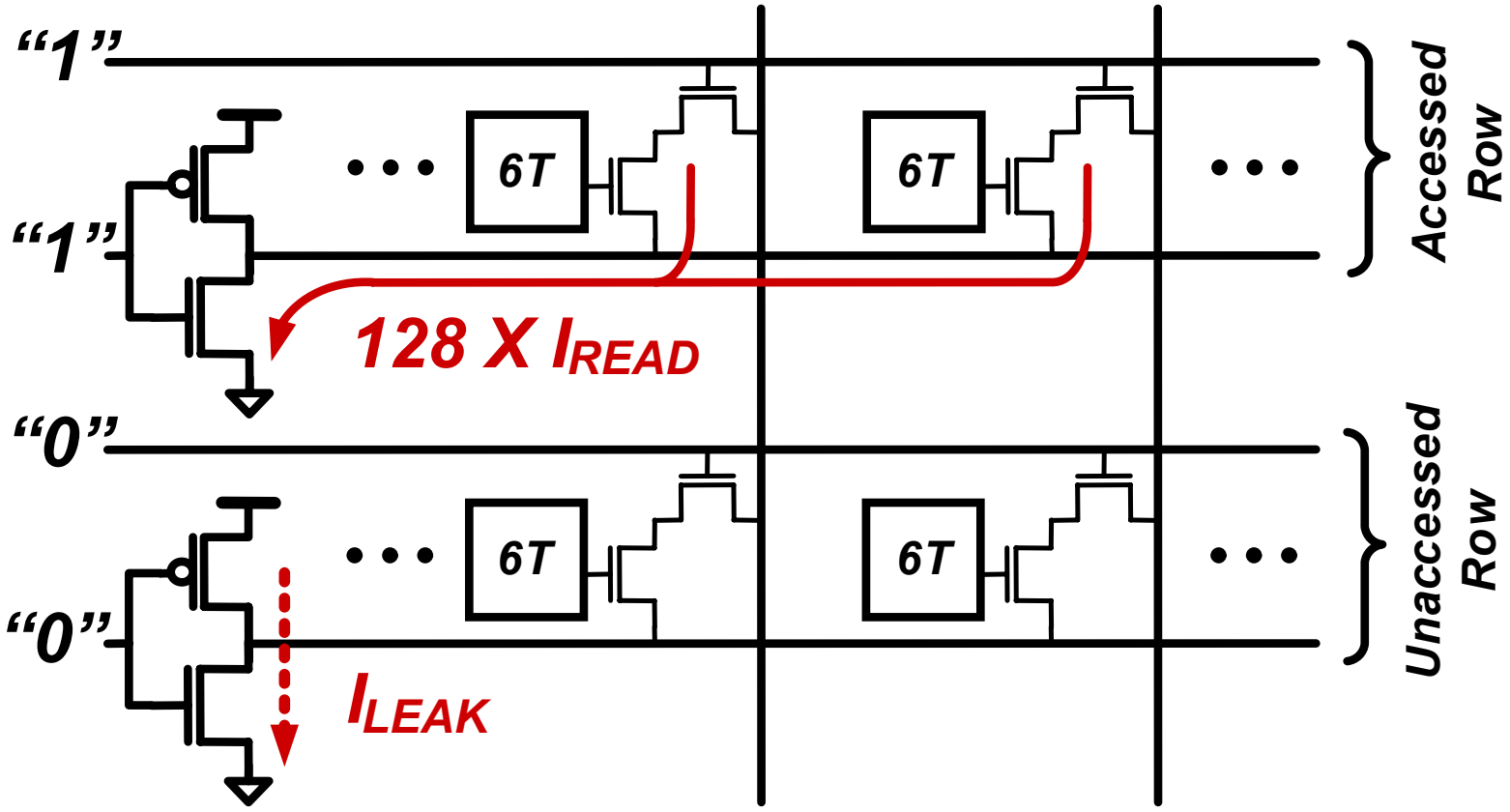
"Zero" Sub-Vt Leakage Read-Buffer





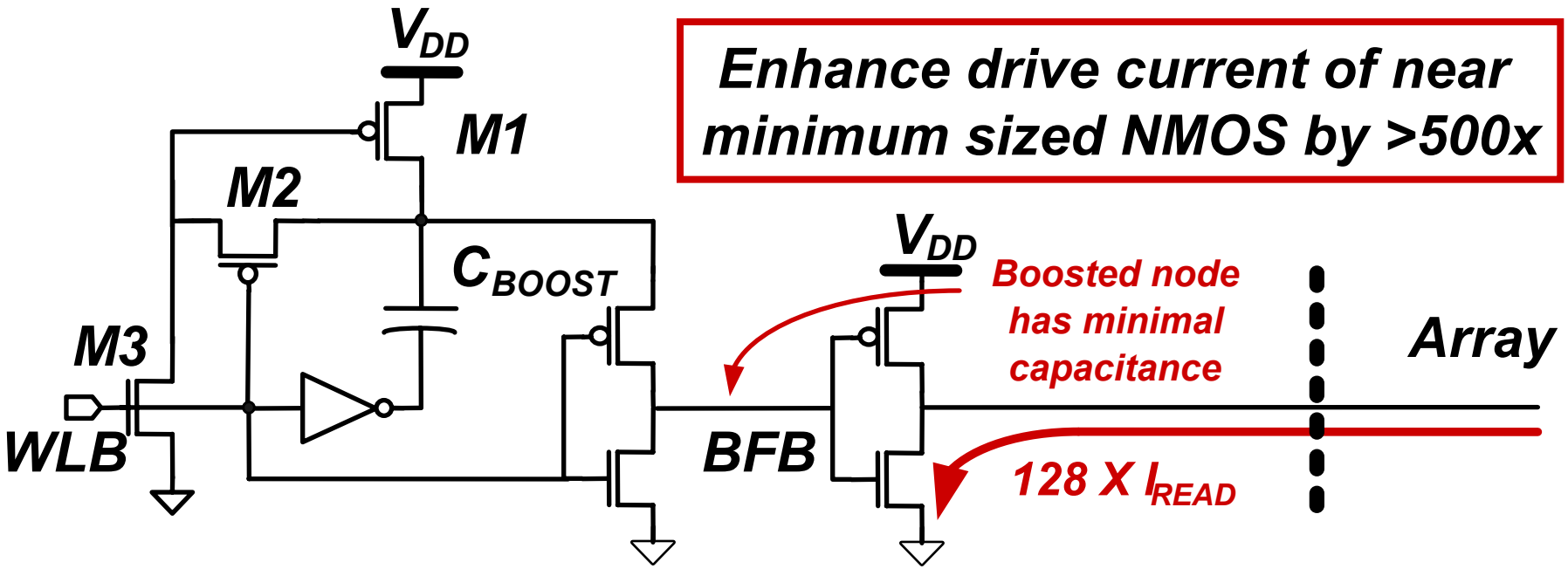


Read-Buffer Foot-Driver Limitation

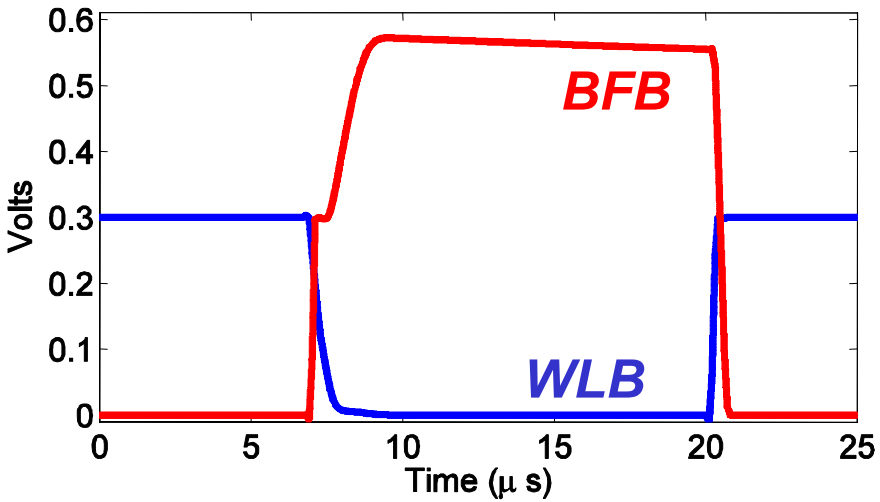


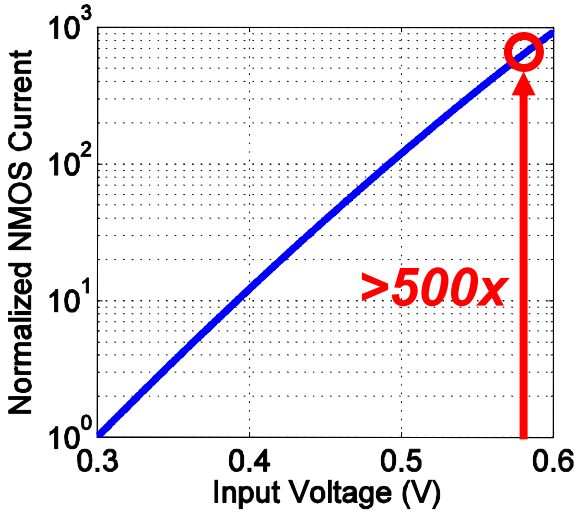
Read-buffer foot-driver must have strong drive current but consume minimal leakage power and area

Gate-Boosted Foot-Driver



Enhance drive current of near minimum sized NMOS by >500x

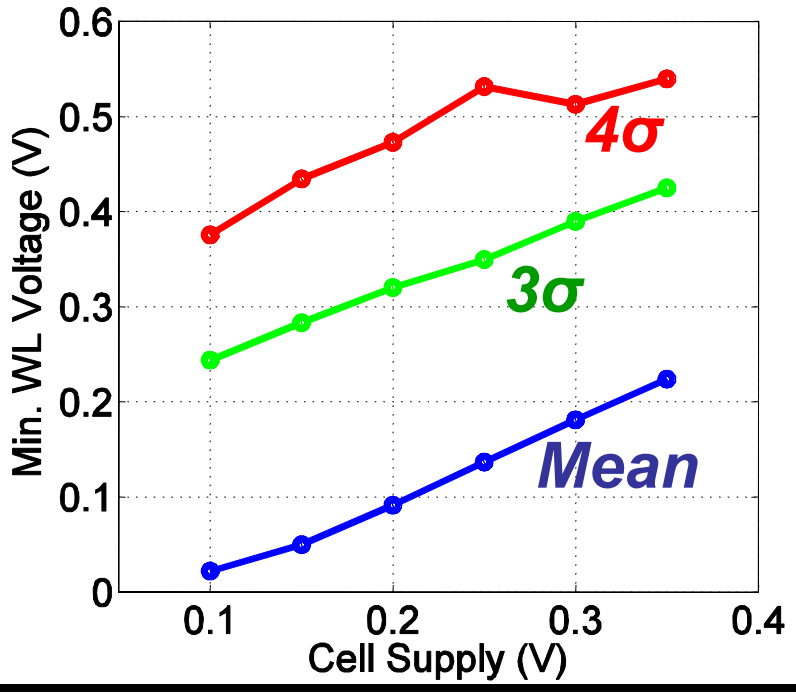




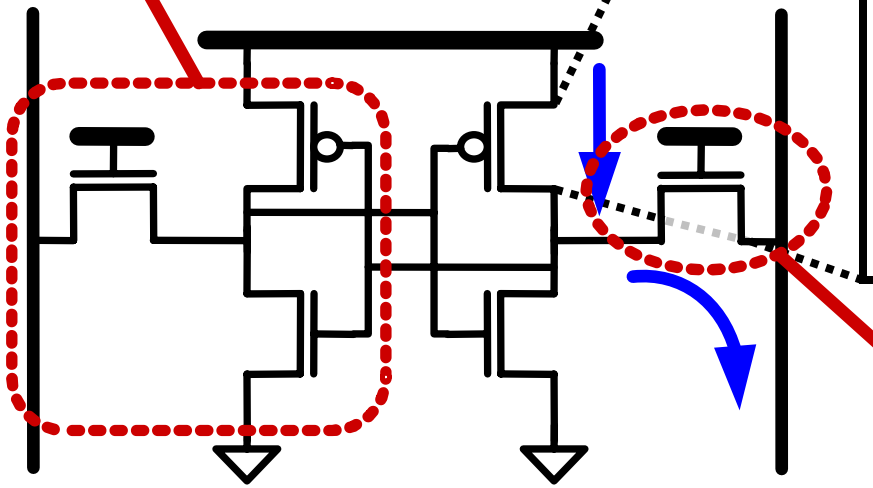
Sub-Vt Write

To ensure write, boost WL 50mV and reduce cell supply

Reduce gate drive



Adjust trip voltage

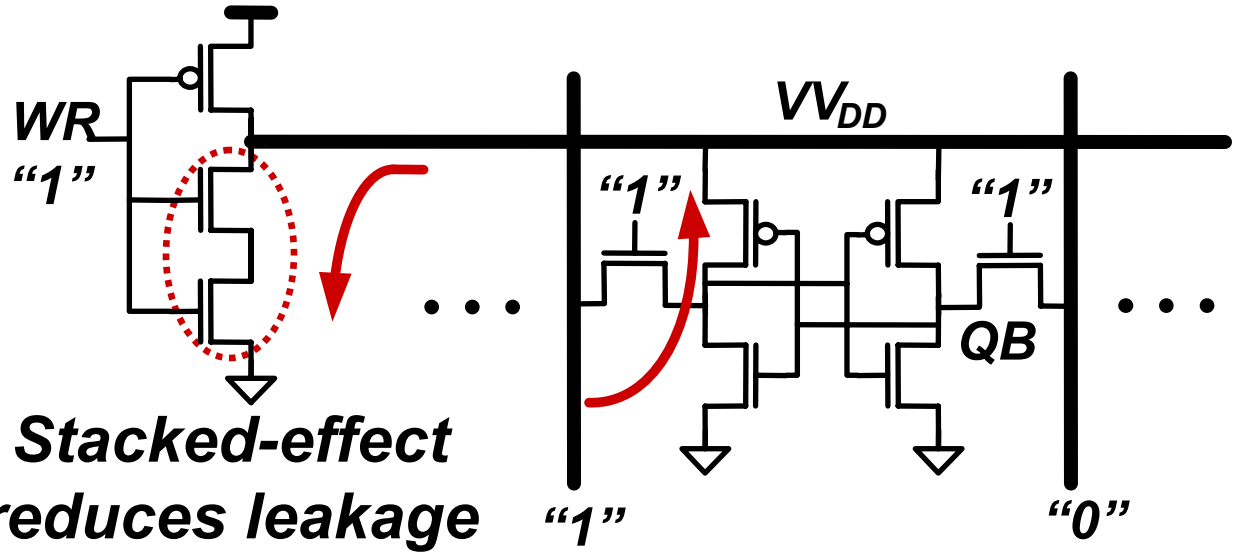


Increase gate drive

"1"

"0"

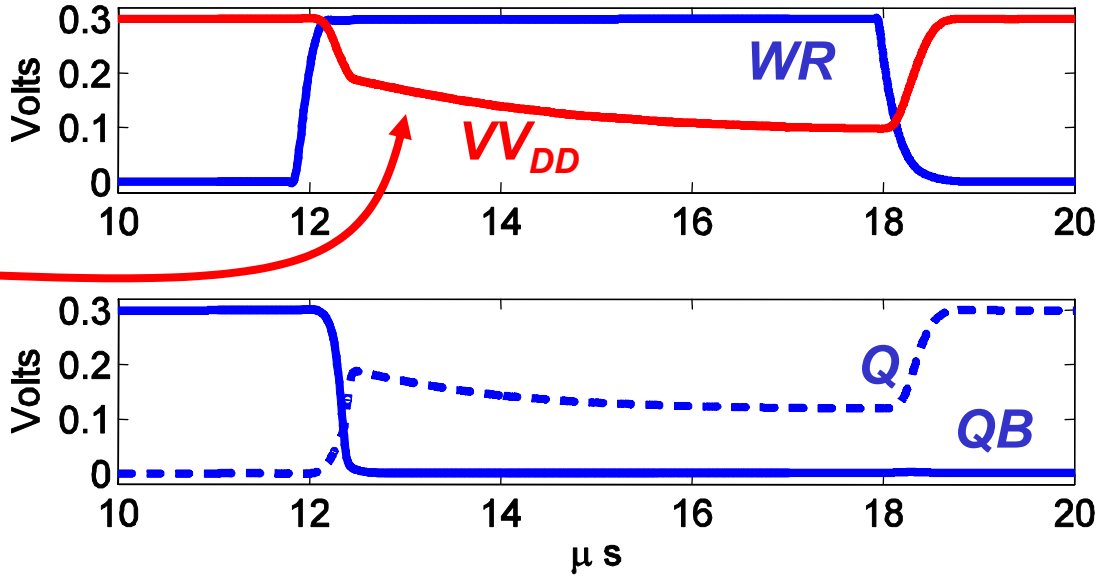
Virtual Cell Supply



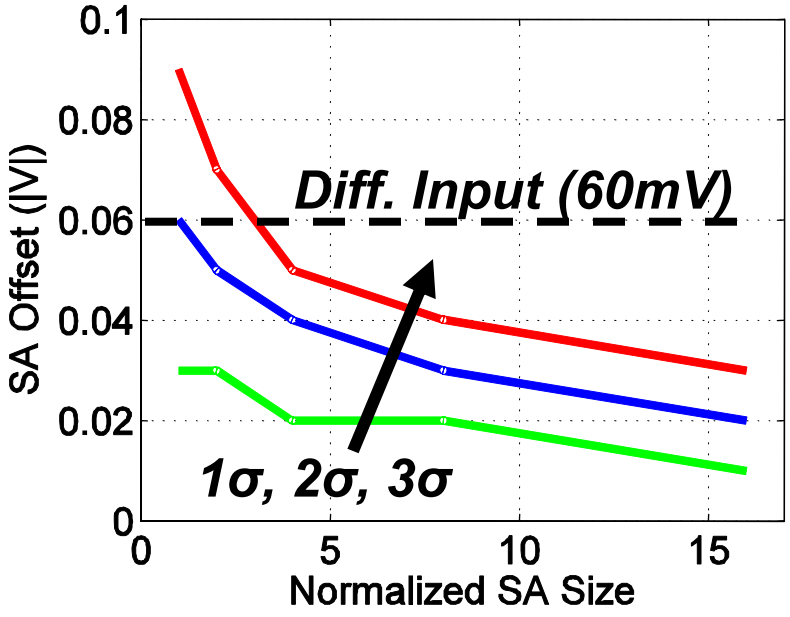
Stacked-effect reduces leakage during hold

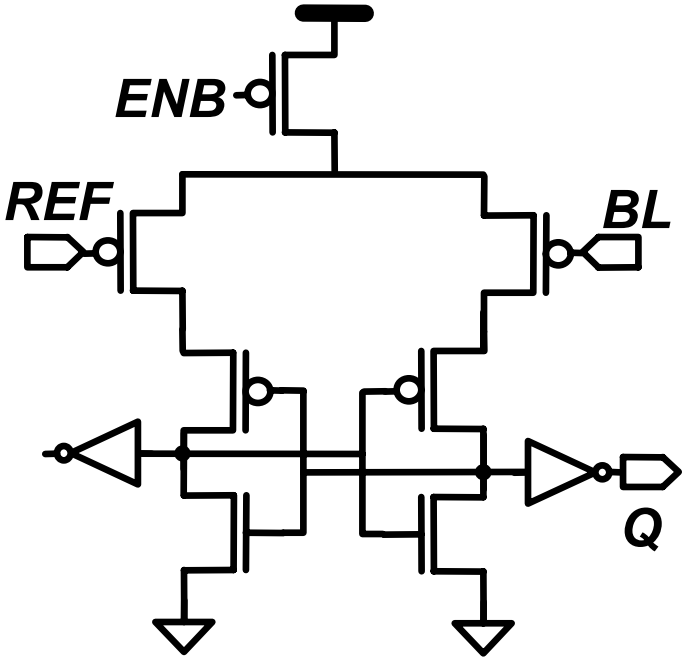
Access devices and supply-driver interact to accurately set VV_{DD}

VV_{DD} settles to low intermediate voltage



Sense-Amplifier Offset

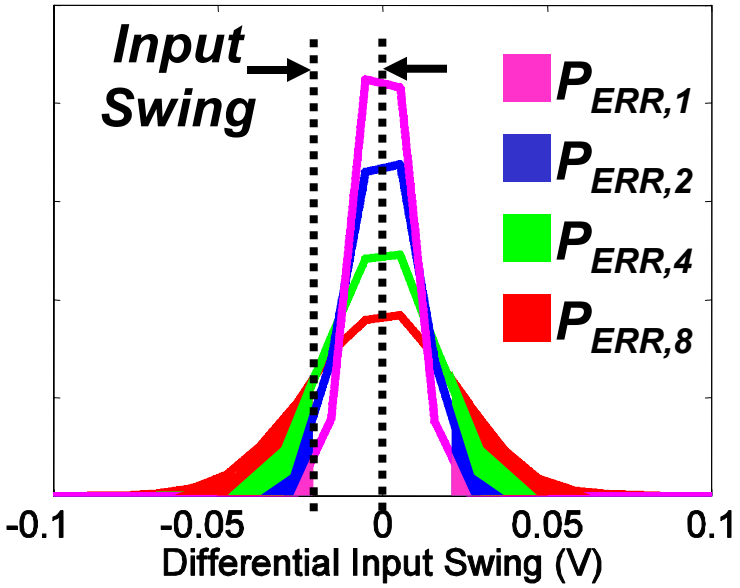


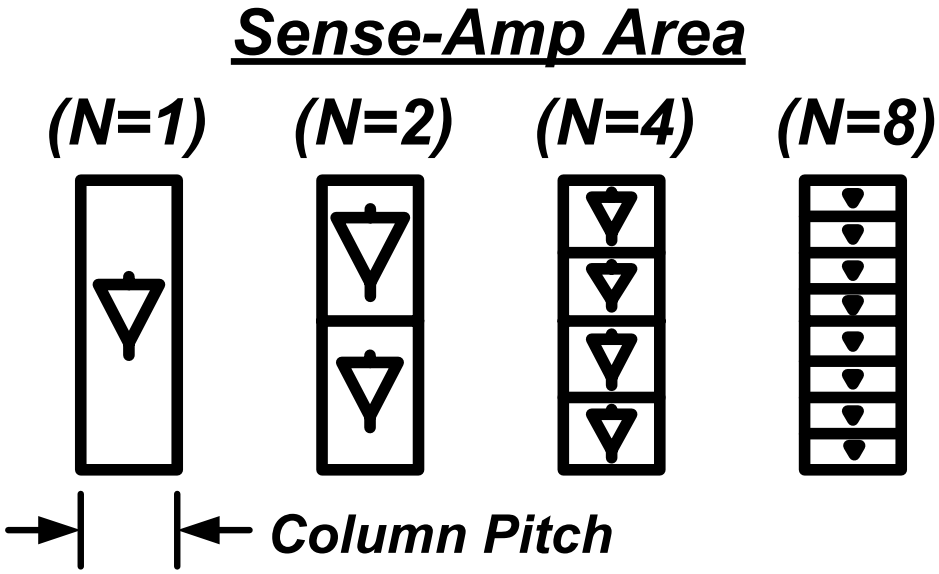


1) <u>Global variation</u> degrades sense-amp accuracy for single-ended read
   - *Pseudo-differential structure eliminates offset*

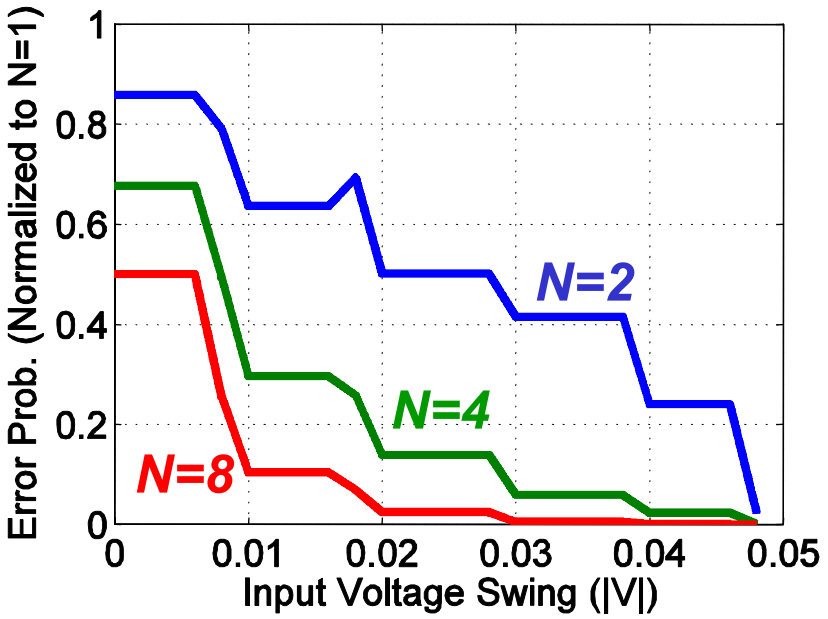
2) <u>Local variation</u> results in uncorrelated error distribution of sense-amps
   - *Only device up-sizing can reduce offset deviation*

Sense-Amplifier Redundancy

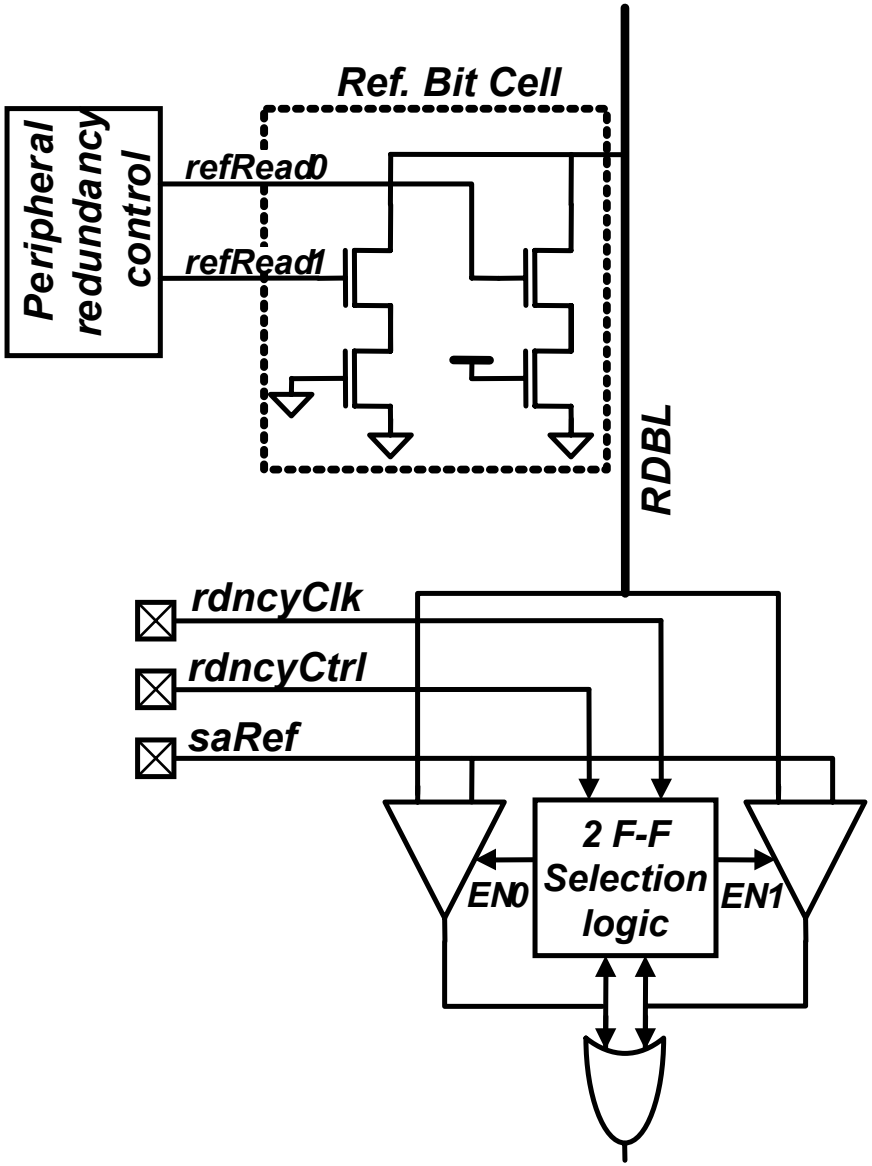




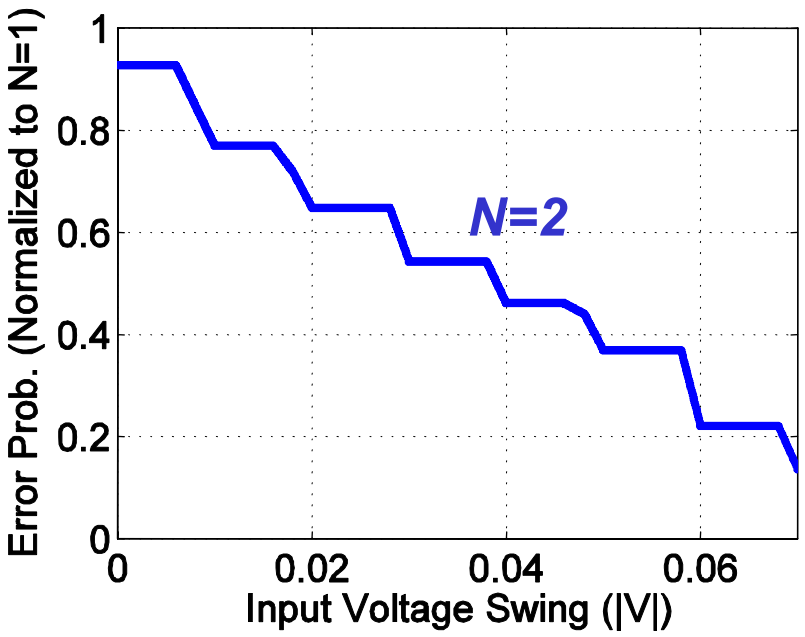
Probability of error depends on joint probability that all sense-amps fail:
$P_{ERR,tot}=(P_{ERR,N})^N$



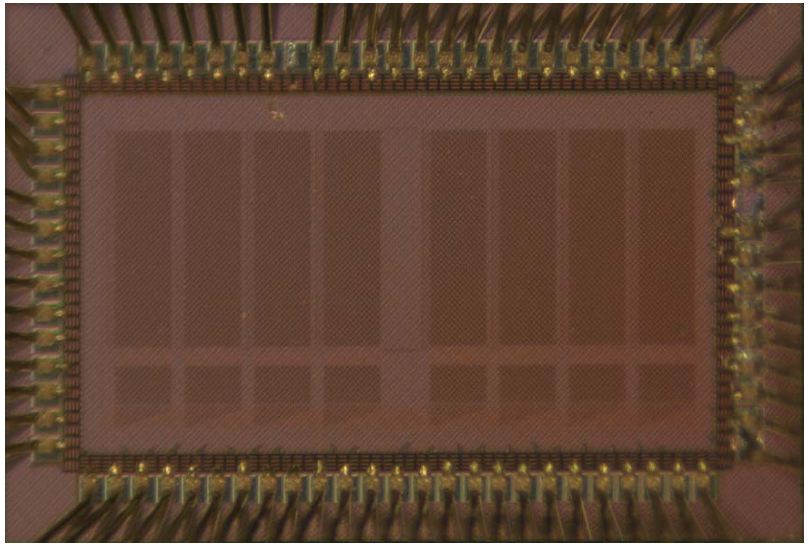
Redundancy Implementation



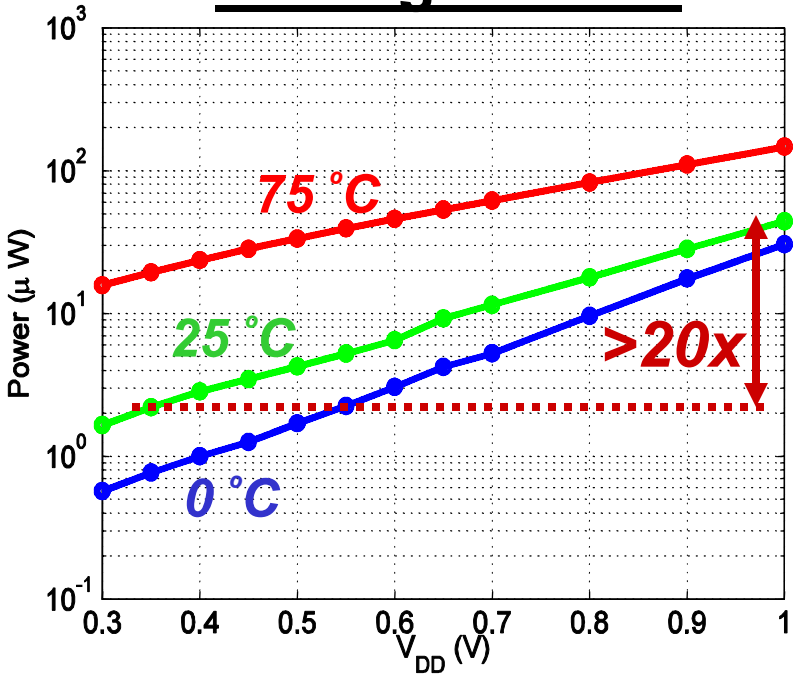
Start-up loop selects between 2 sense-amps, yielding error improvement of 5x



Prototype SRAM



Leakage Power

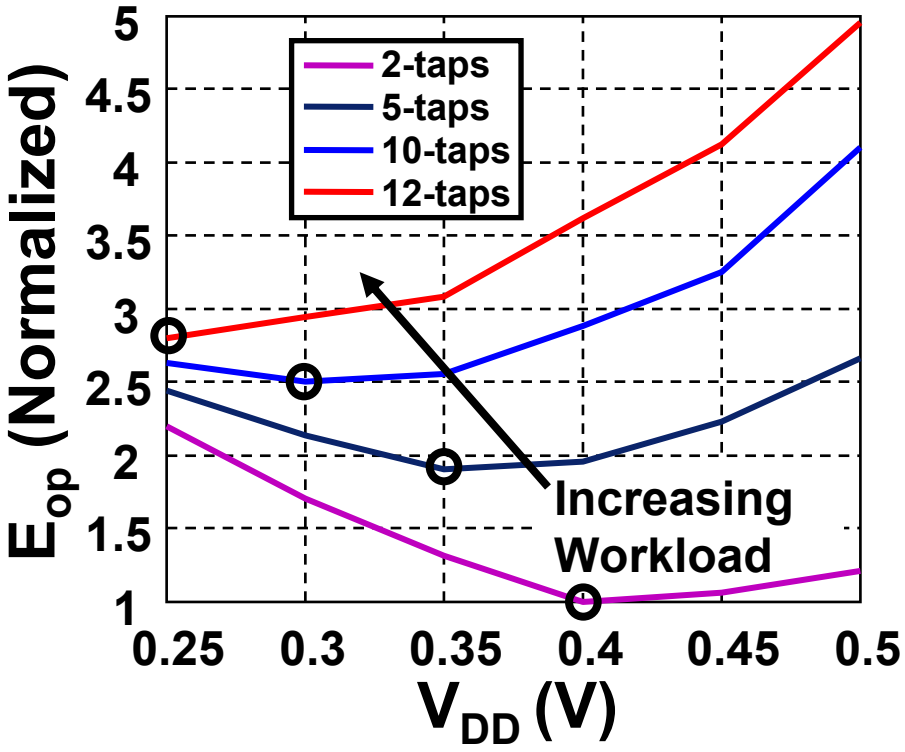


Process	*65nm CMOS*
Architecture	*8 Blocks X 256 Rows X 128 Columns*
Capacity	*256kb*
V_{MIN}	*350mV*

[N. Verma, et al., ISSCC'07]

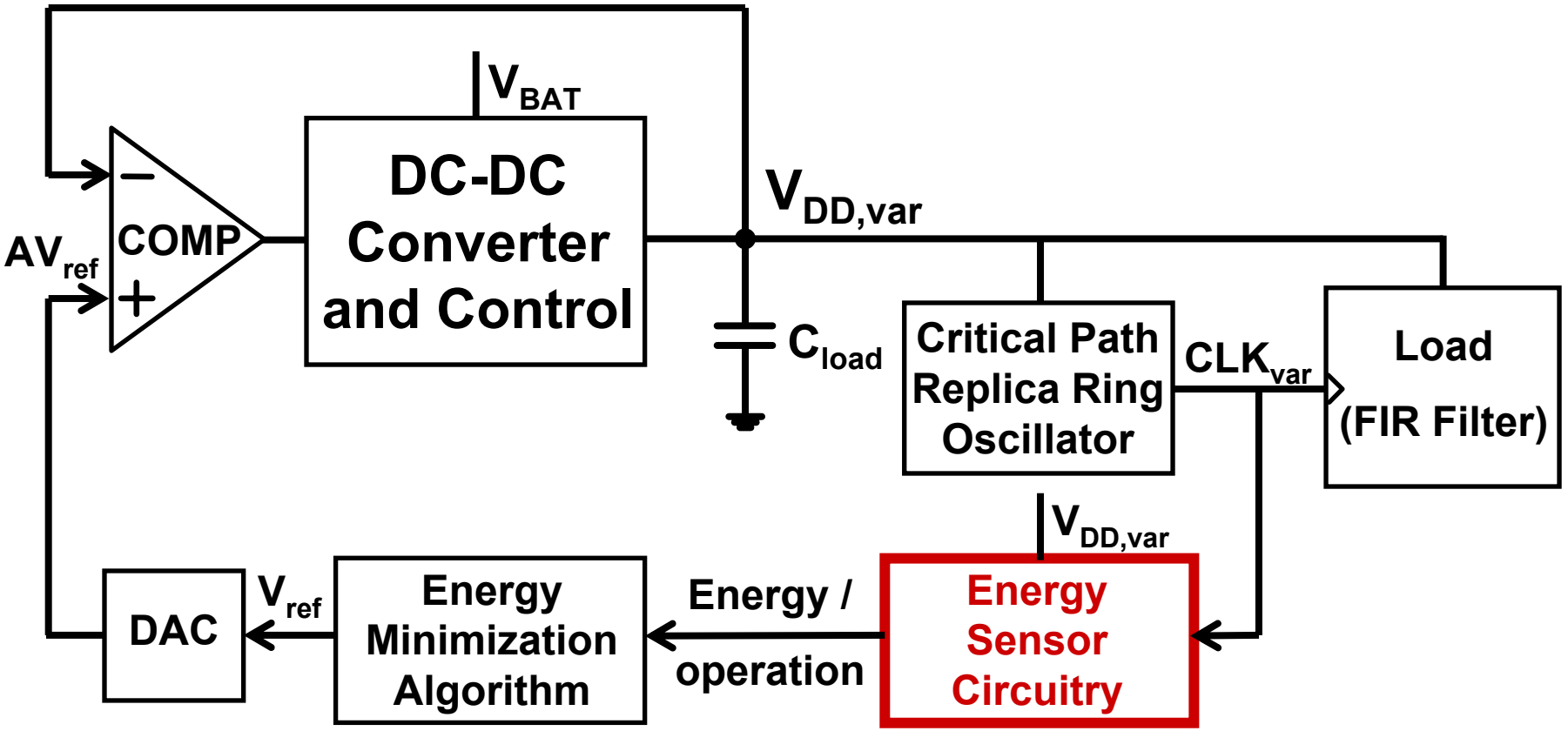
Delivering the Optimum V_{DD}

Workload, Activity ↑	E_{ACTIVE} ↑	V_{MEP} ↓
Temperature, Duration of Leakage ↑	$E_{LEAKAGE}$ ↑	V_{MEP} ↑



- Minimum Energy Point (MEP) varies with workload and temperature
- Tracking the MEP : *Energy changes by ~3X*

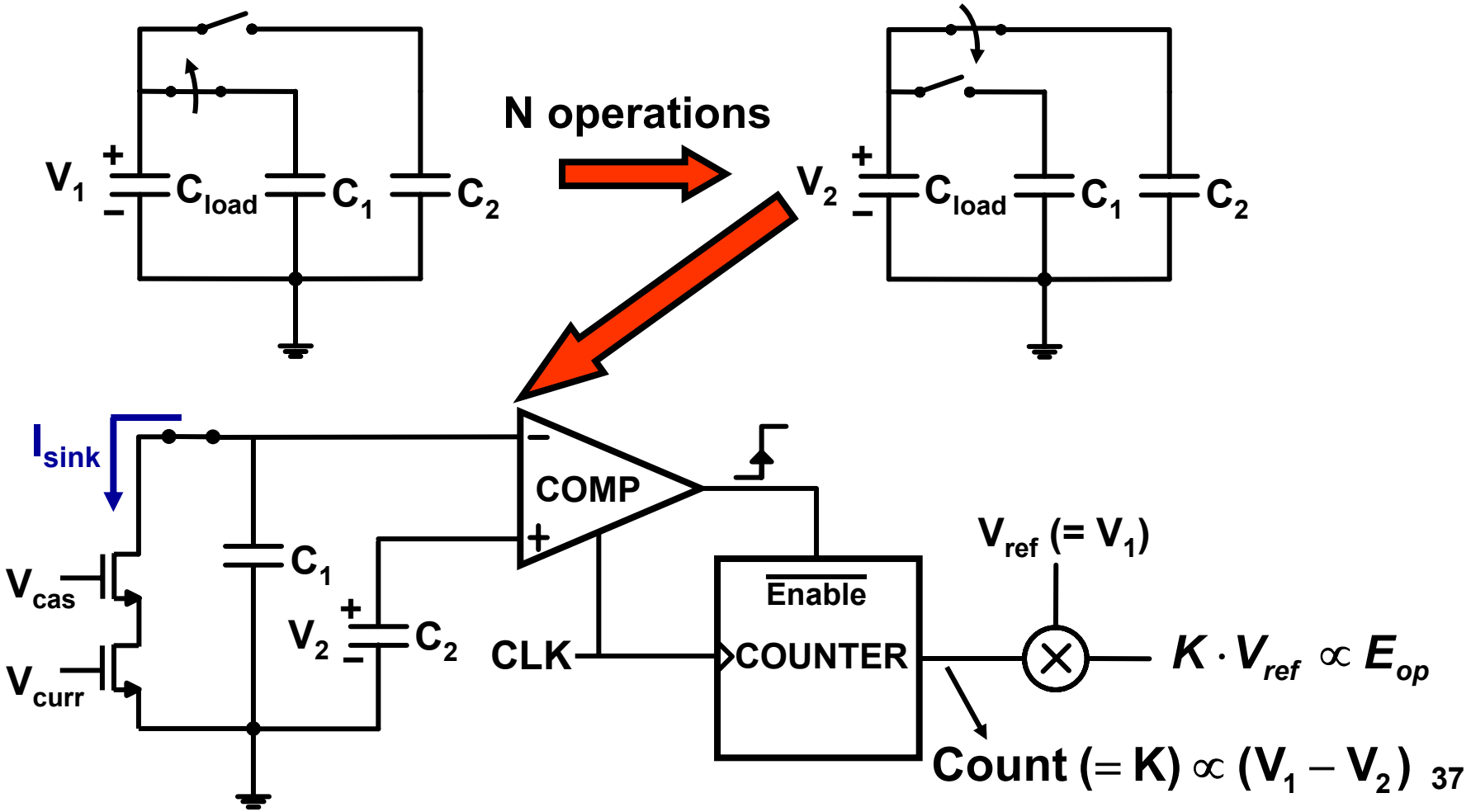
Minimum Energy Tracking Loop



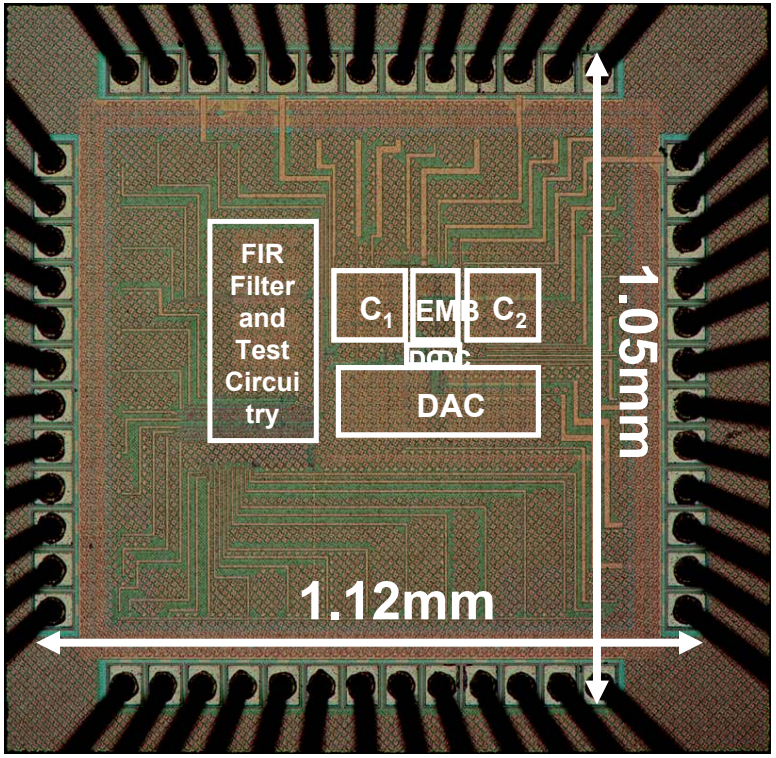
Completely on-chip except for the passive filter components

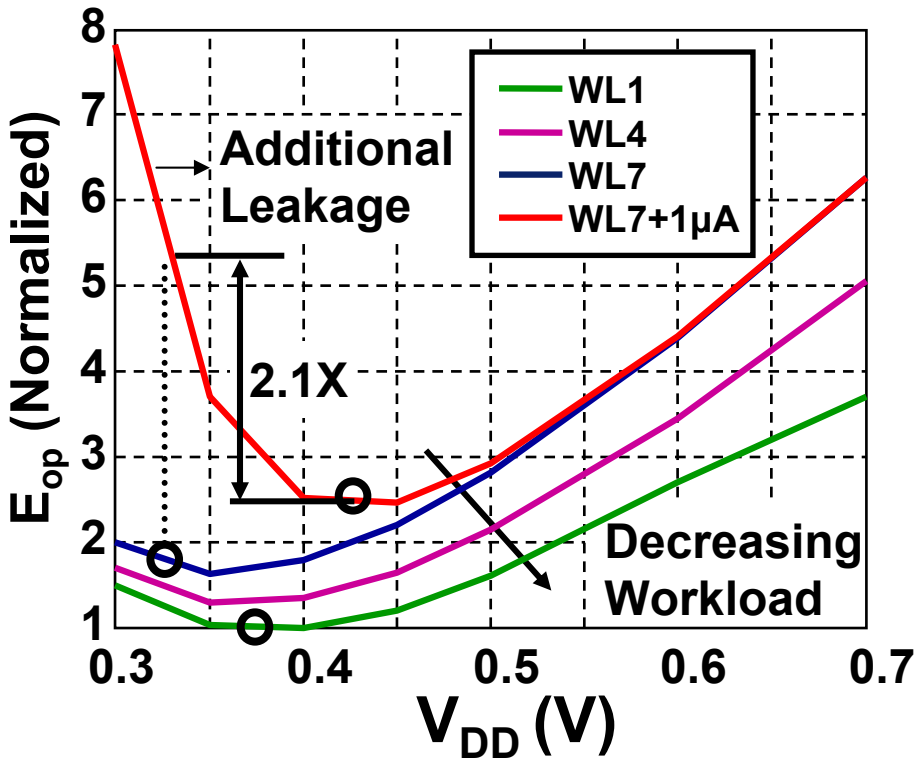
Calculating Energy/Operation

$$E_{OP} \propto V_1^2 - V_2^2 \approx 2V_1(V_1 - V_2)$$



Prototype MEP Tracking Loop

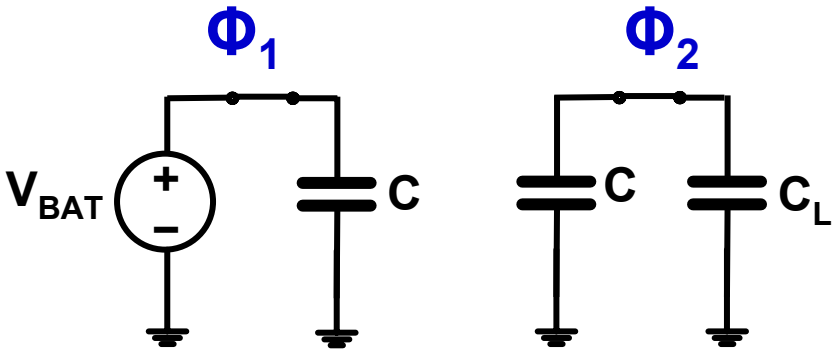




Automatic adjustment of MEP based on workload gives 2.1X energy savings

Capacitive DC/DC Conversion

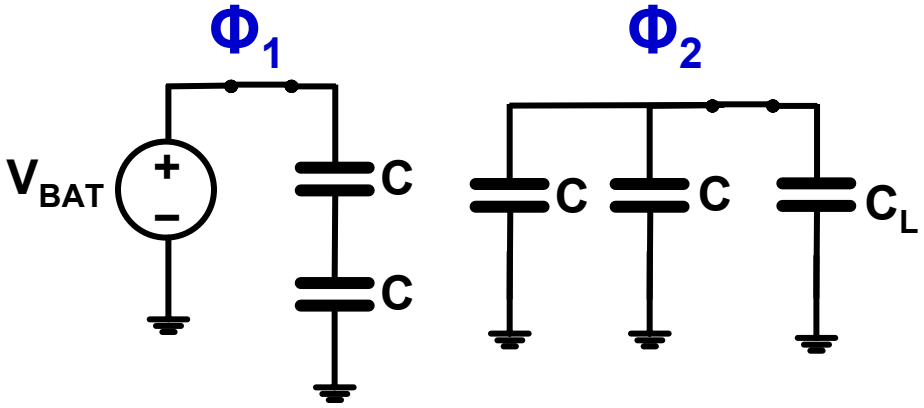
$V_{CL} = V_{BAT} - \Delta V$



$$\eta_{BL} = \frac{V_{BAT} - \Delta V/2}{V_{BAT}} \cdot \frac{V_{BAT} - \Delta V}{V_{BAT} - \Delta V/2}$$

$$\eta_{BL} = \frac{V_{BAT} - \Delta V}{V_{BAT}} = \frac{V_{CL}}{V_C}$$

$V_{CL} = V_{BAT}/2 - \Delta V$

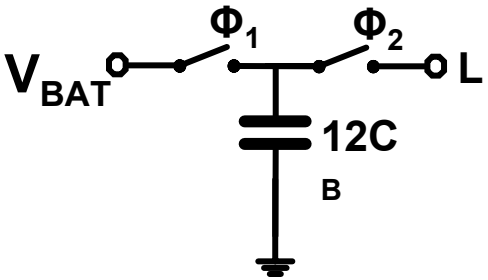


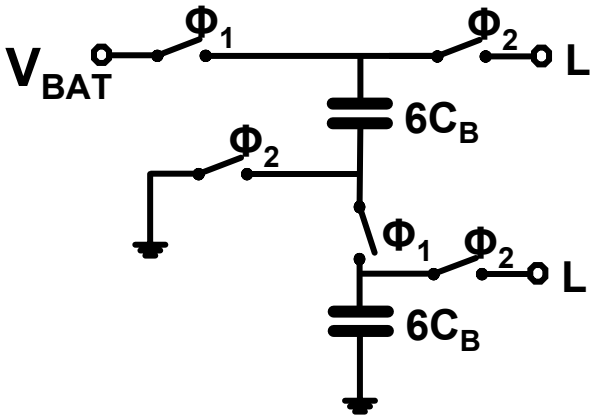
$$\eta_{BL} = \frac{V_{BAT} - \Delta V}{V_{BAT}} \cdot \frac{V_{BAT}/2 - \Delta V}{V_{BAT}/2 - \Delta V/2}$$

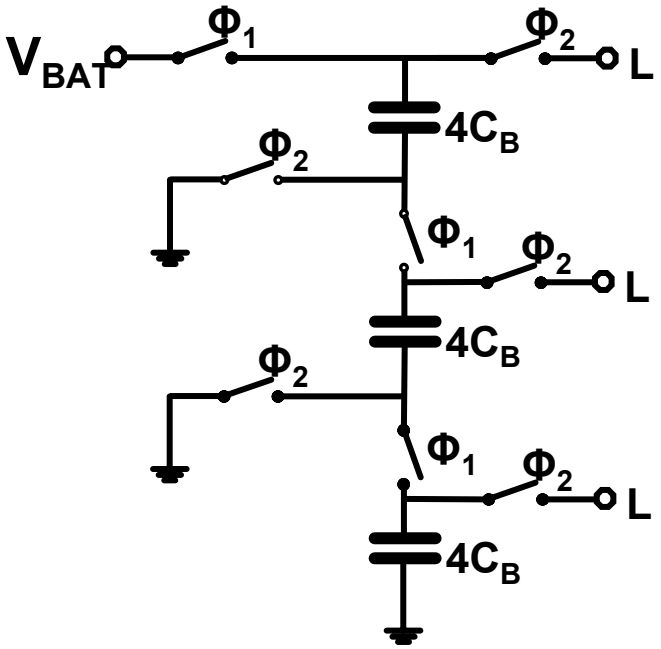
$$\eta_{BL} = \frac{V_{BAT}/2 - \Delta V}{V_{BAT}/2} = \frac{V_{CL}}{V_C}$$

Linear efficiency drop: need $V_C \approx V_{CL}$

Scalable Voltage Generation







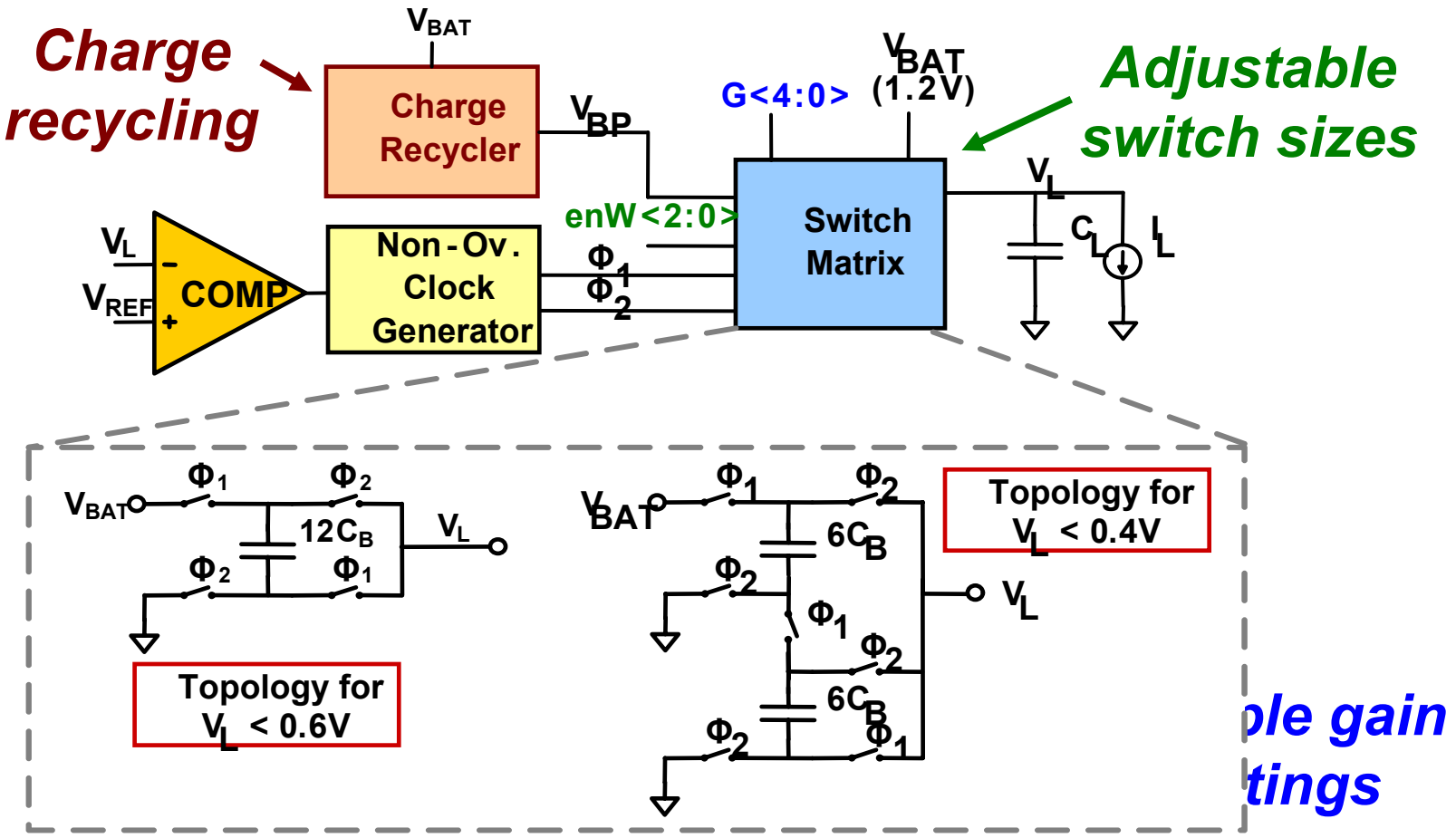
Ratio: 1/1

Ratio: 1/2

Ratio: 1/3

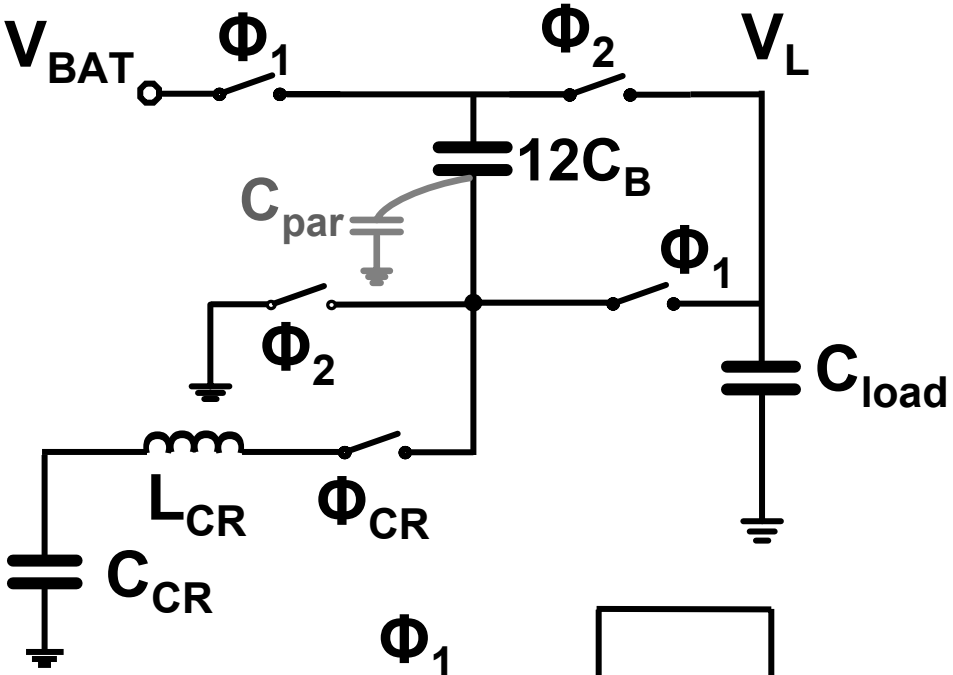
Programmable switches yield DC/DC conversion for desired load voltages

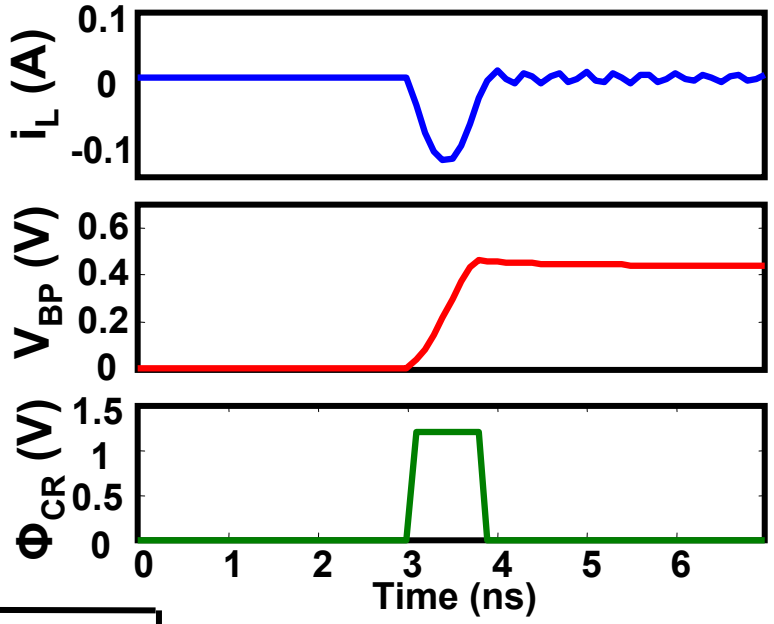
Fully On-Chip Conversion to 0.3V

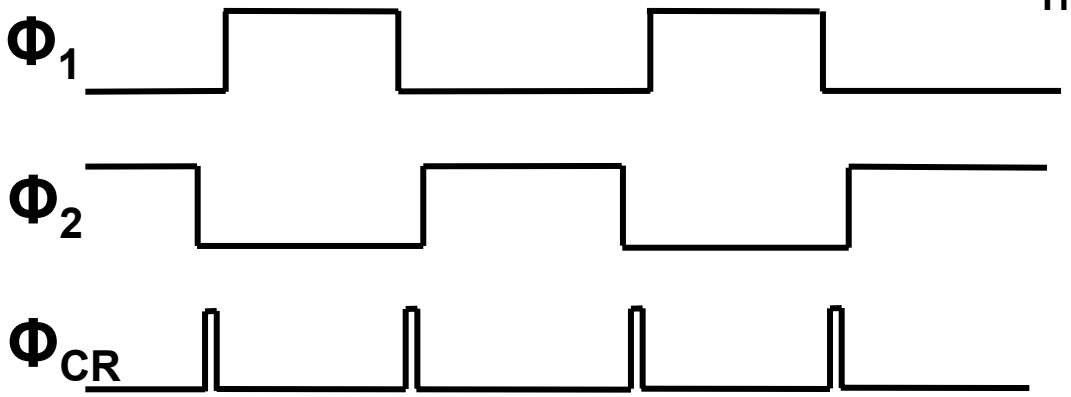


Switch capacitors can be integrated on-chip for low load currents

Charge Recycling



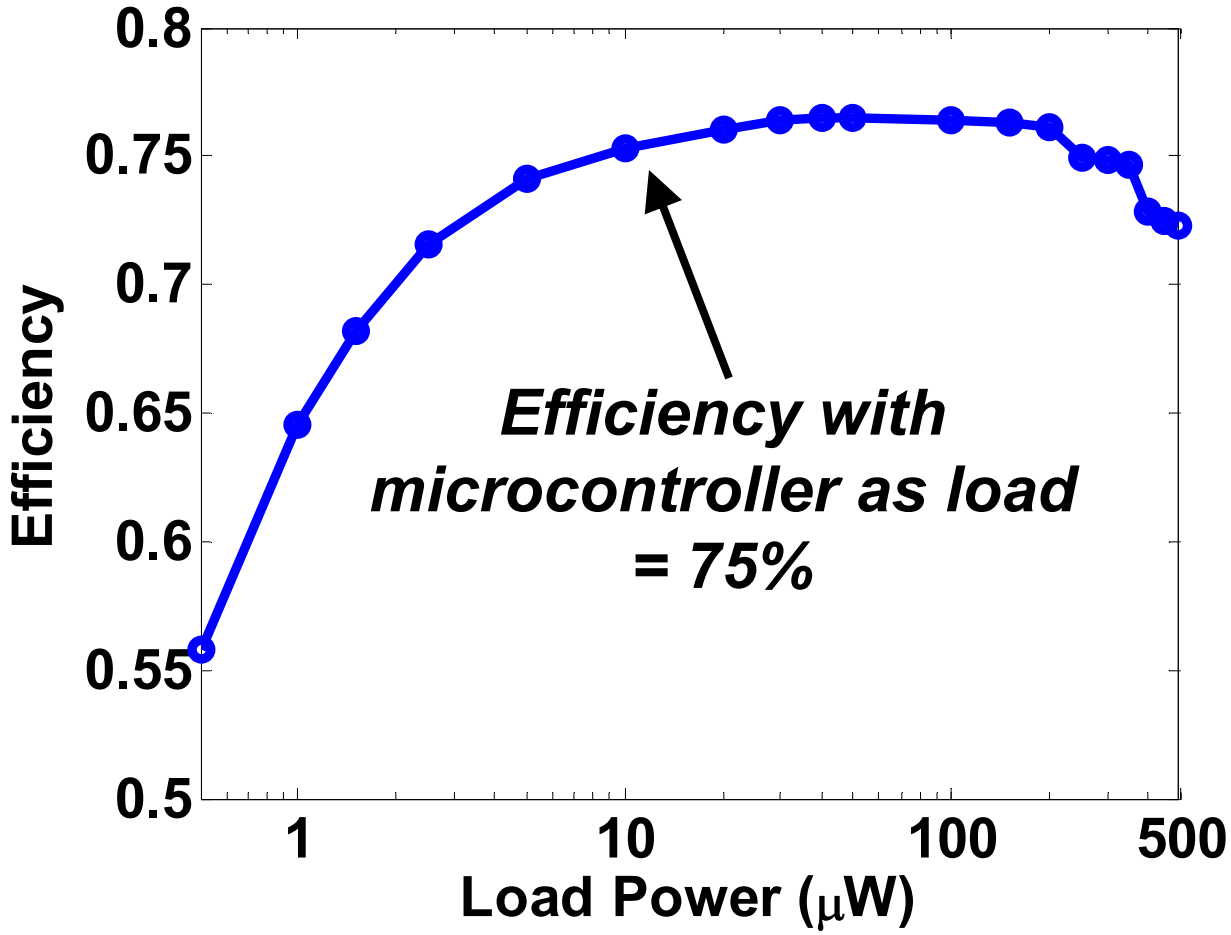




Reduce losses due to bottom plate parasitic capacitance

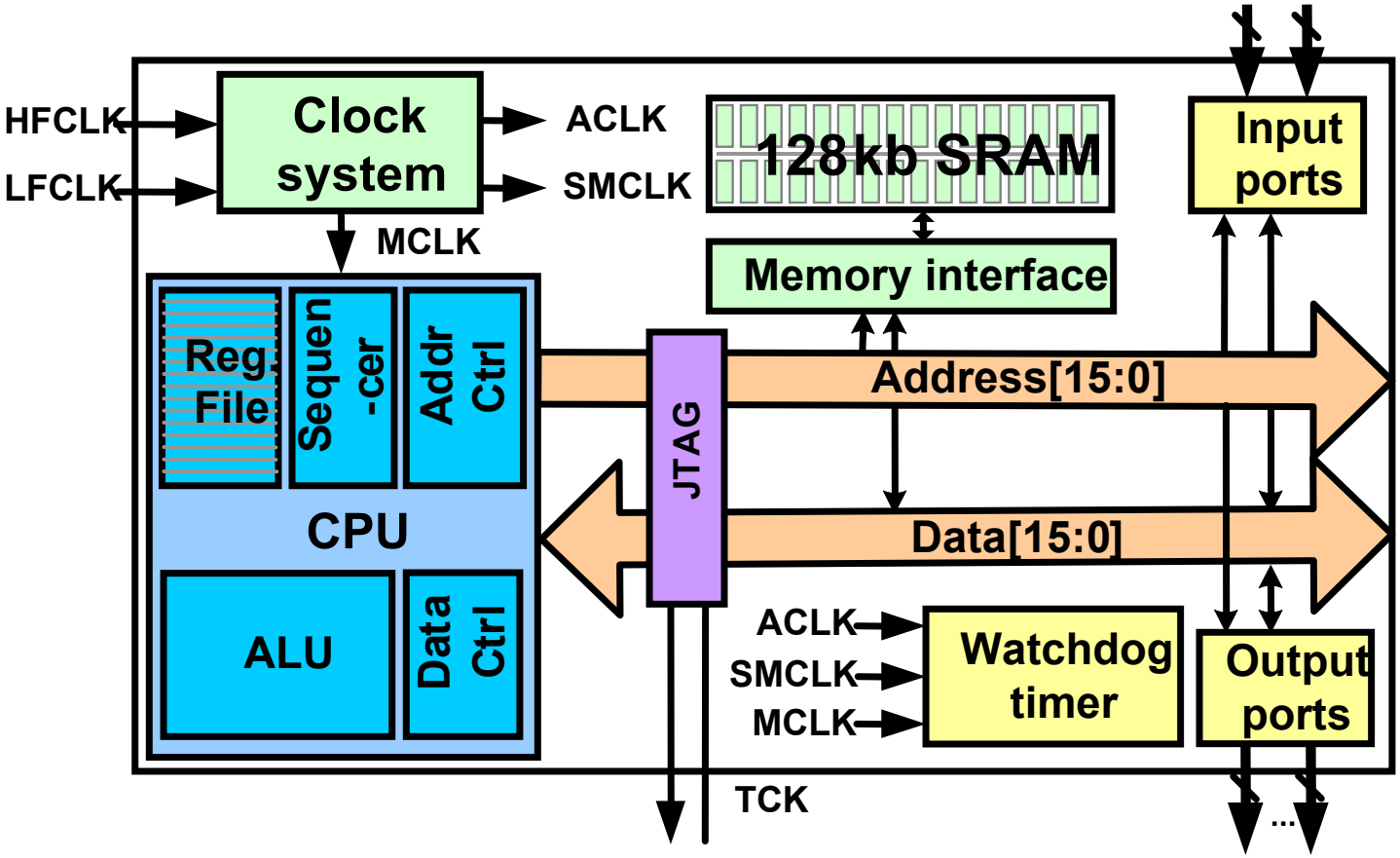
DC-DC Converter Efficiency

Measured efficiency while delivering 500mV

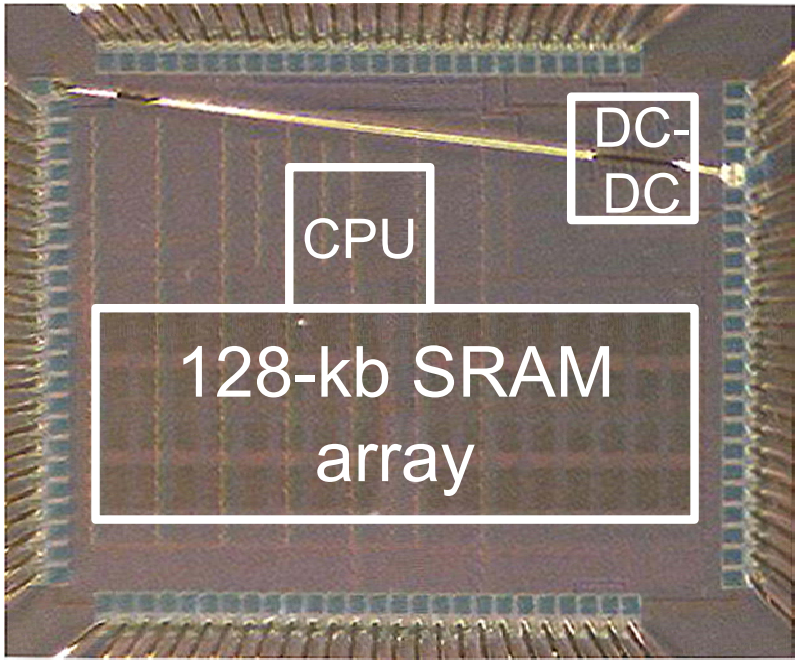


Sub-V_t Microcontroller

- 16-bit RISC architecture
- Supports 27 instructions and 7 addressing modes of the standard MSP430 instruction set



Prototype 0.3V SoC



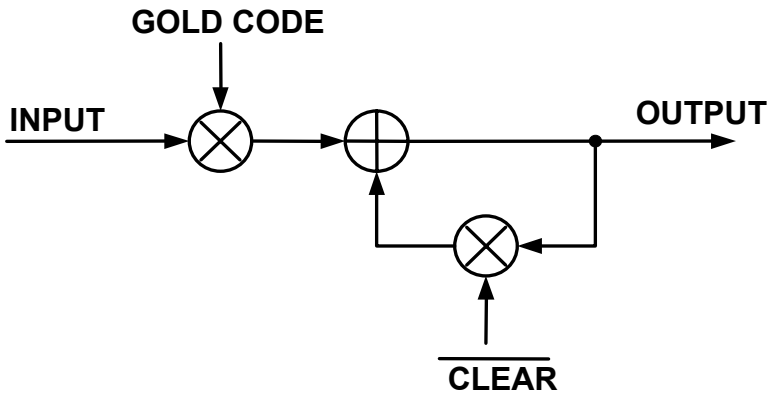
Process	65nm CMOS
Area	
DC-DC Converter	0.12mm^2
SRAM	1.36mm^2
Logic	0.14mm^2
Performance	
Minimum Energy Point	V_{DD} = 500mV
Minimum Functional V_{DD}	V_{DD} = 300mV

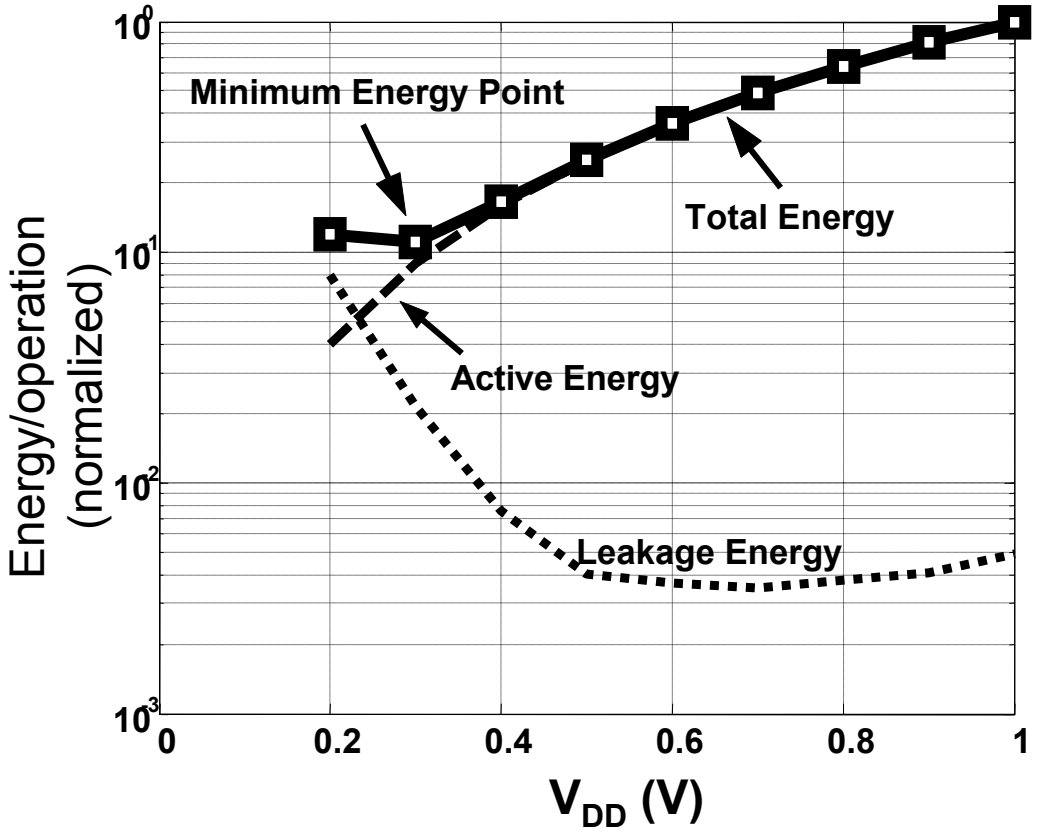
2.5µW leakage power, 10µW total power at 400kHz

[J. Kwong, et al., ISSCC'08]

Parallelism to Meet Performance

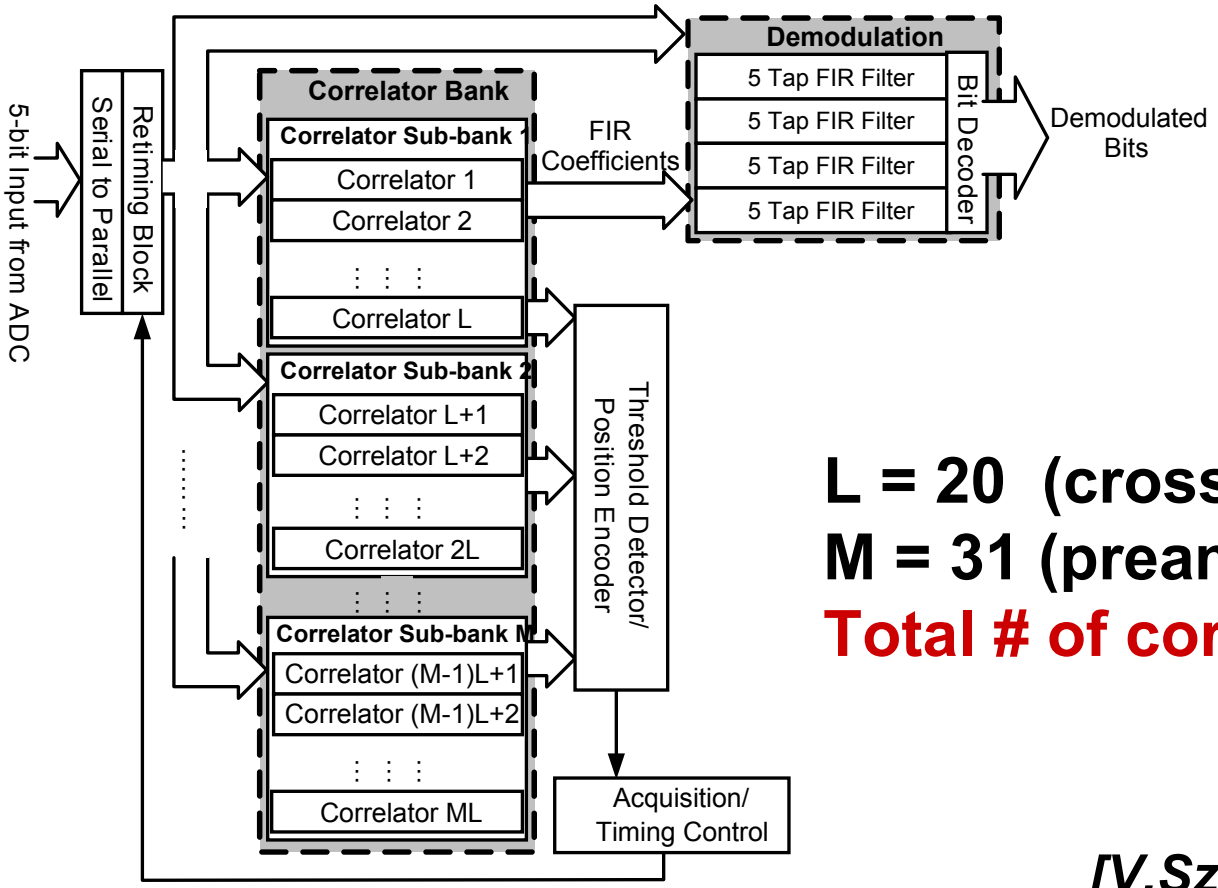
Baseband energy dominated by correlators





MEP occurs at 0.3V, BUT baseband throughput is constrained (500MSymb./s)

Parallelize Baseband Architecture

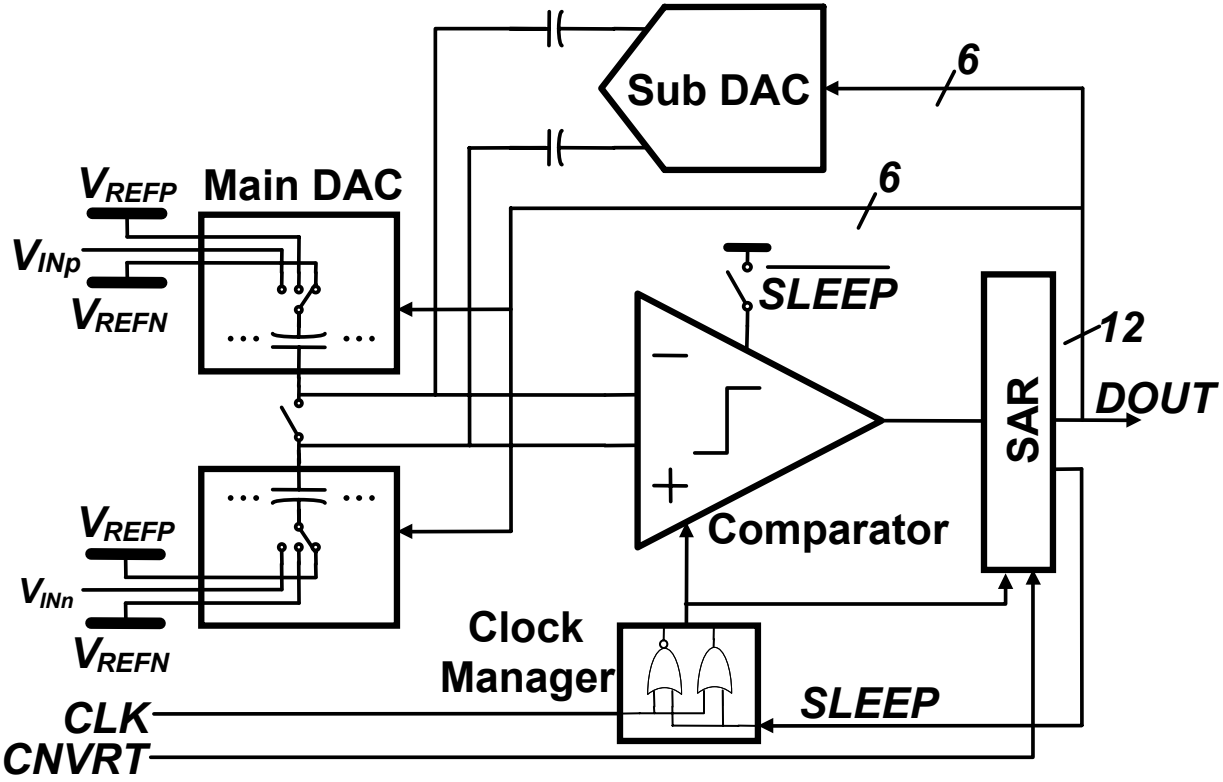


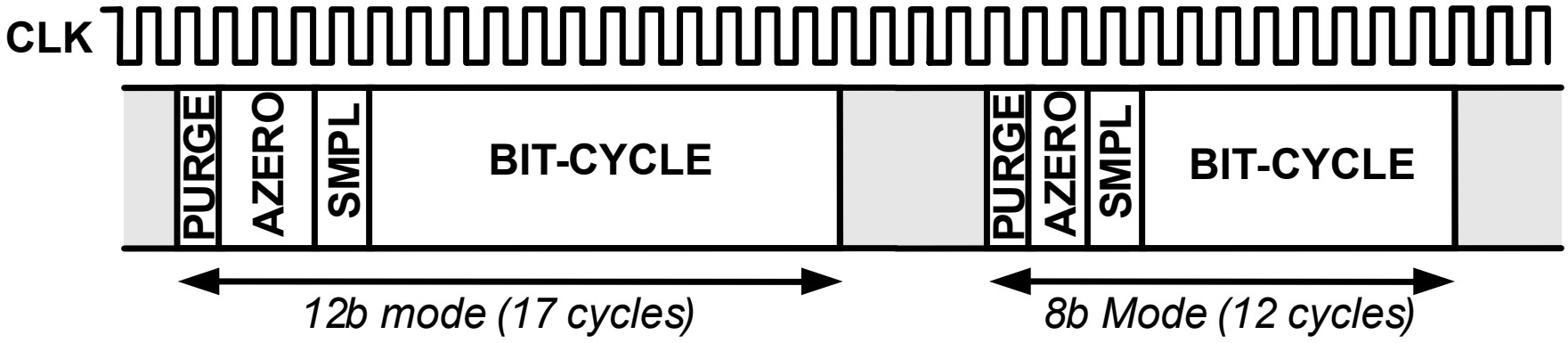
L = 20 (cross-correlation)
M = 31 (preamble symbols)
Total # of correlators = 620

[V.Sze, et al., ISLPED'07]

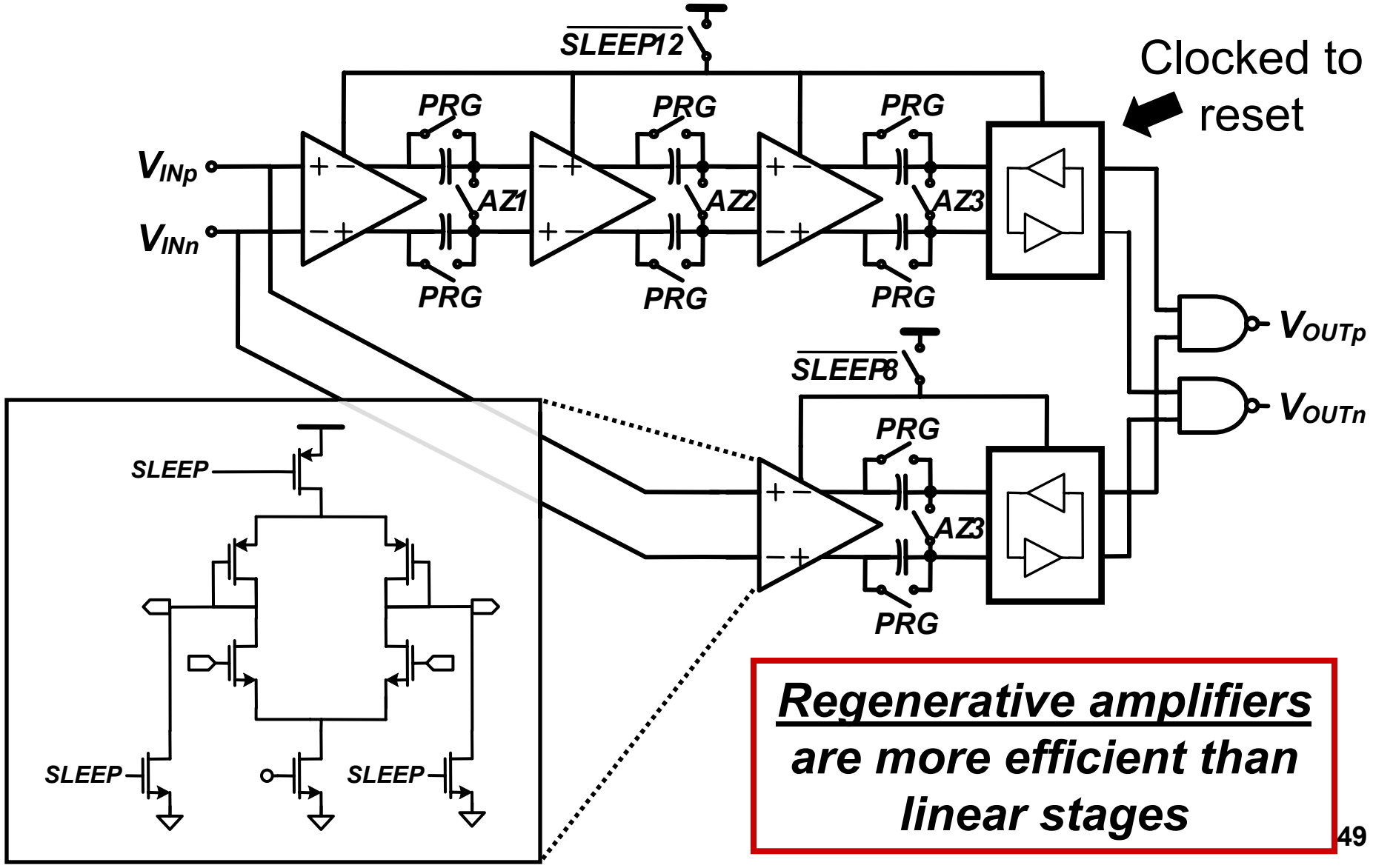
500MSymb/s performance at 0.4V: 5.8X energy savings

Scalable, Low-Power SAR ADC



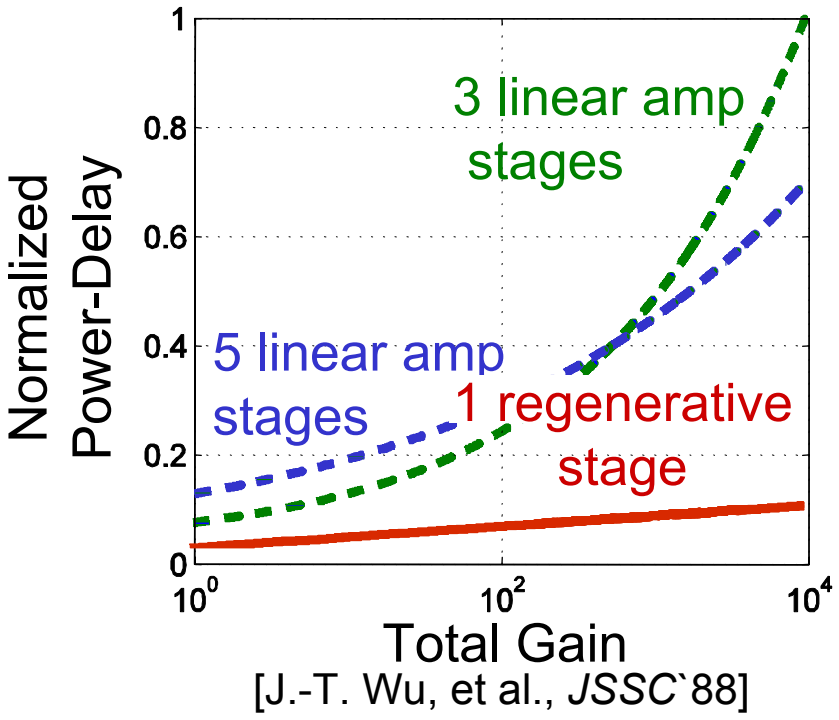


Scalable Comparator

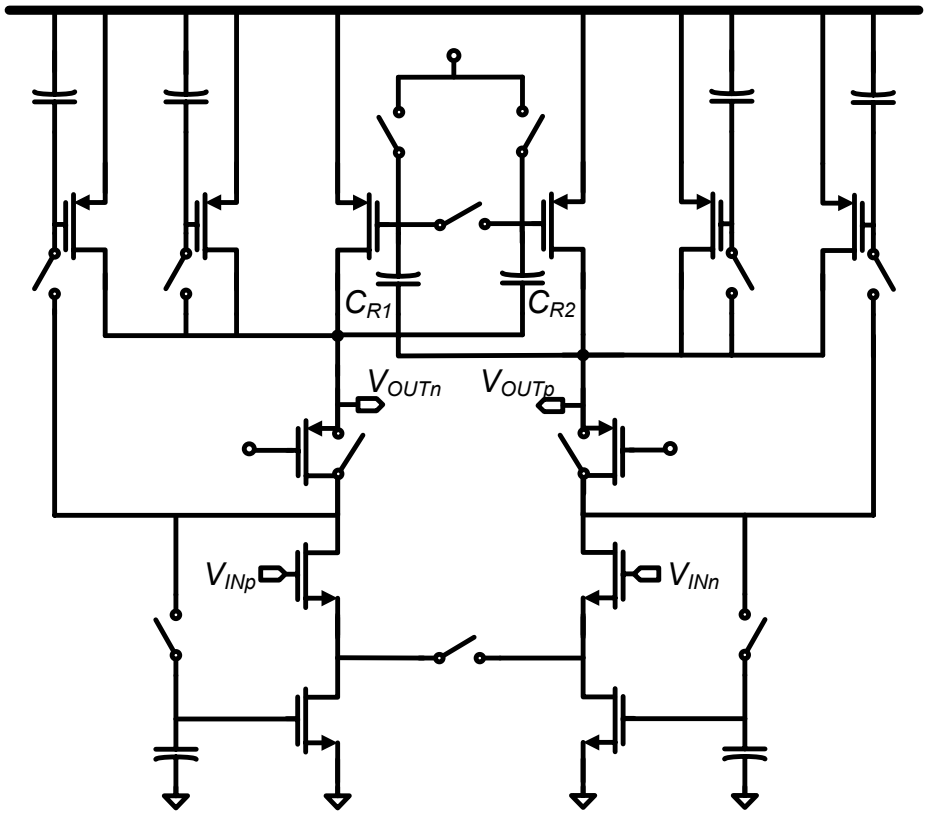


Regenerative amplifiers are more efficient than linear stages

Offset Compensating Latch

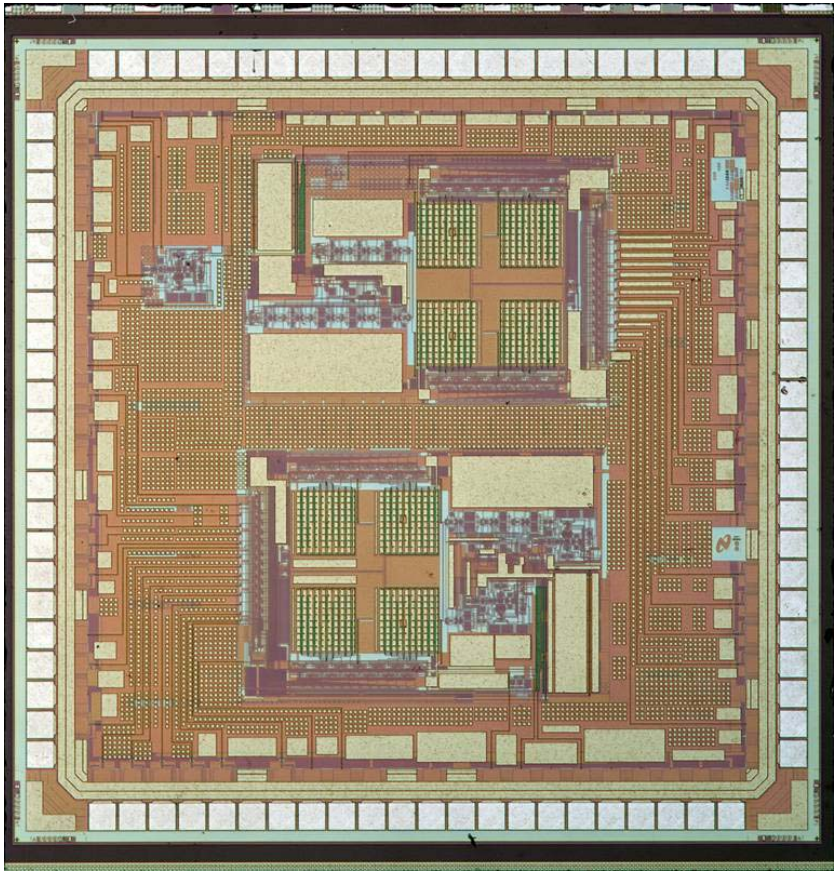


[J.-T. Wu, et al., *JSSC*`88]



Reduces gain requirement of less efficient linear pre-amps by 100X

12/8b 0-100kS/s SAR ADC

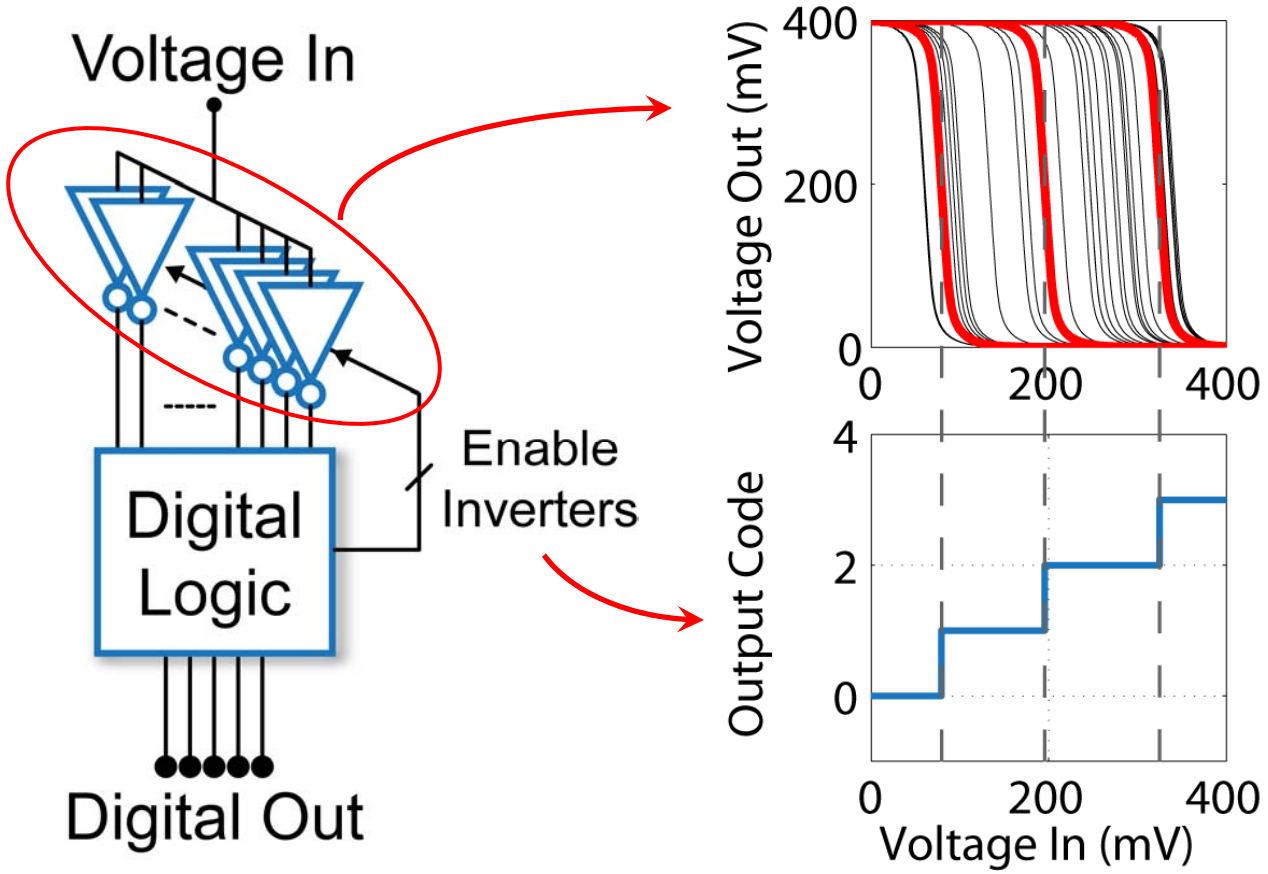


	12b Mode
Power	25μW
Max. Fs	100kS/s
SNDR	65.5dB
FOM	165fJ/Conv. Step

[N.Verma, et al., ISSCC'06]

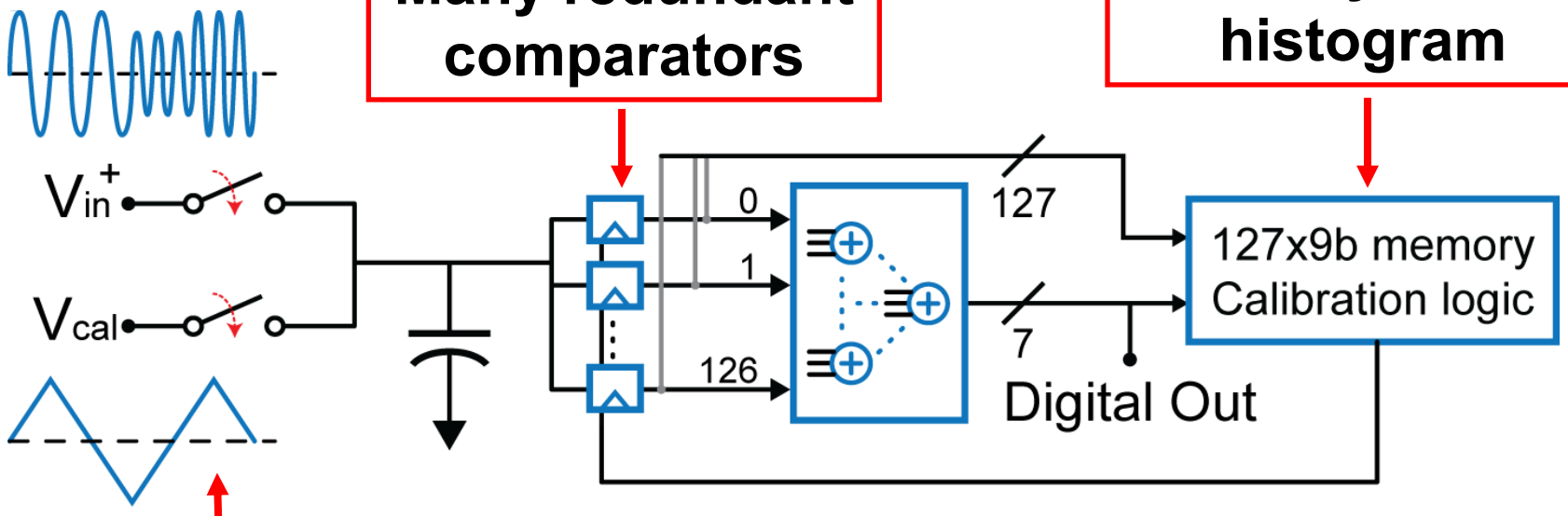
Variation Resilient ULV ADC

- CV_{DD}^2 highly digital, low-voltage flash ADC



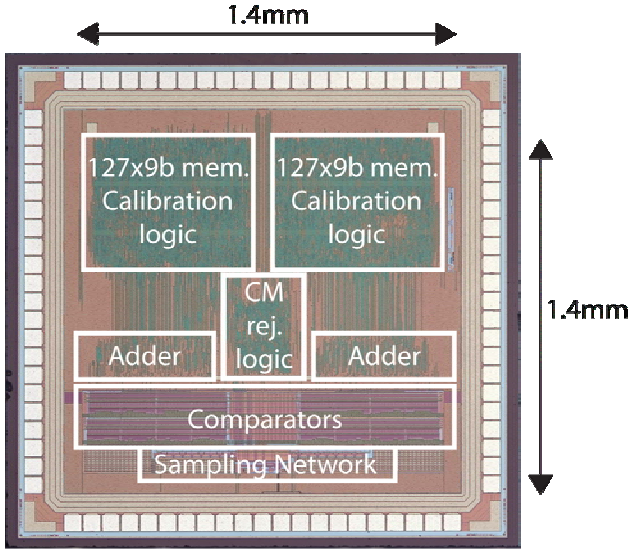
Required resolution allows use of redundancy to improve yield

Simplified ADC Architecture

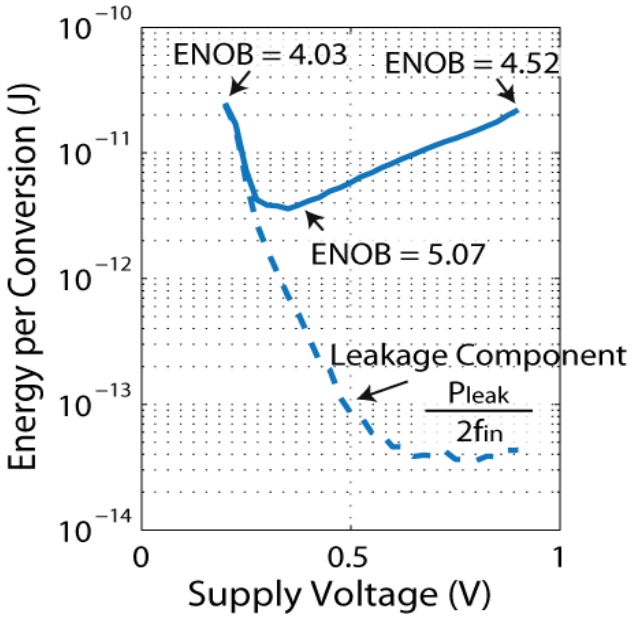


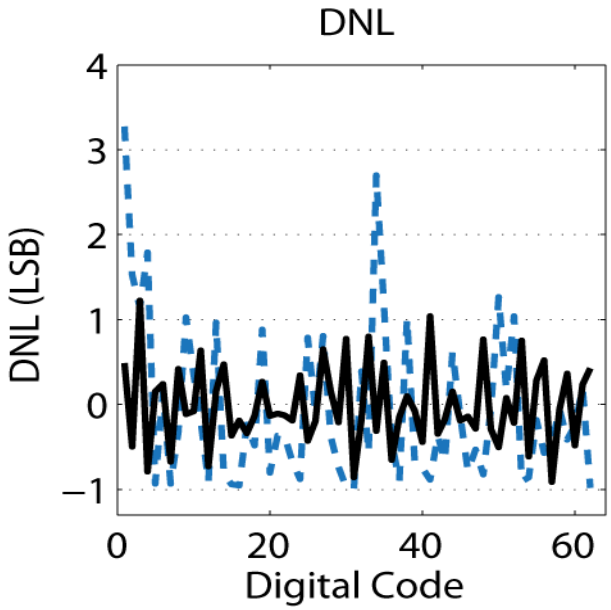
Highly digital, voltage scalable architecture

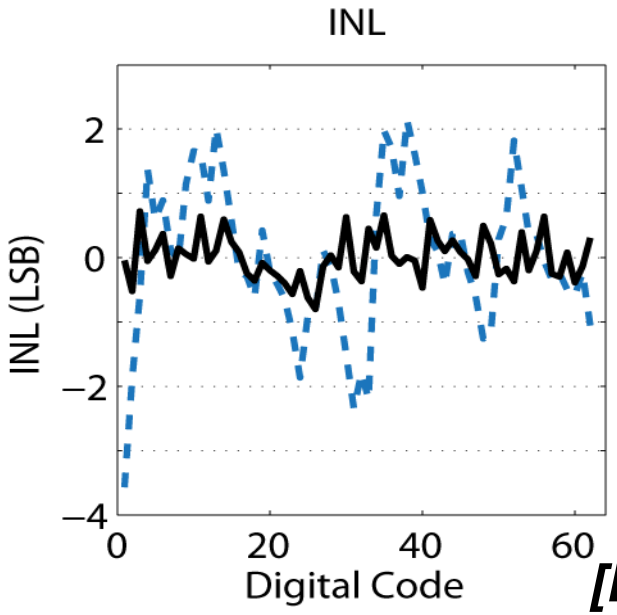
6-bit Static Performance



0.2-0.9V Operation







Before calibration

After calibration

[D.Daly, et al. ISSCC'08]

Conclusions

- Energy Efficient operation (Joules/op, Joules/conversion, Joules/bit) requires system-level optimization
- Exploit application specific attributes (reduced performance requirements) to save energy
- Exploit highly digital approaches for traditional analog function
- *Slower is Better*–exploit sub-threshold operation to minimize energy dissipation

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