

A Micro-power EEG Acquisition SoC with Integrated Seizure Detection Processor for Continuous Patient Monitoring

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Abstract

Continuous on-scalp EEG monitoring provides a non-invasive means to detect the onset of seizures in epilepsy patients, but cables from the scalp pose a severe strangulation hazard during convulsions. Since the power of transmitting the EEG wirelessly is prohibitive, a complete SoC is presented, performing low-power EEG acquisition, digitization, and local digital-processing to extract detection features, reducing the transmission-rate by 43x. To maximize power-efficiency, the acquisition LNA operates at the lowest reported V_{DD} (of 1V, drawing $3.5\mu W$), but is able to reject offsets (characteristic of metal-electrodes) that are even larger than the supply voltage. Importantly, its topology simultaneously optimizes noise-efficiency and input-impedance to maximize electrode signal-integrity, and it uses switch-capacitor transformers to improve the noise and manufacturability of large on-chip resistors. The complete SoC generates EEG feature-vectors every 2sec, consuming a total of $9\mu J$ per feature-vector.

System Approach

Epileptic seizures arise from abnormal electrical neural activity in the brain. Detection, via non-invasive on-scalp EEG, of the subtle onset enables actuation of alert signals or stimulators to abort the seizure before motor control is catastrophically lost. Early detection relies on deciphering fine shifts in the spectral energy distribution from up to 18 EEG channels. Generally, EEG is highly irregular from patient-to-patient; so, here, machine-learning is used, where a feature-vector corresponding to the spectral energies is extracted, and a vector classifier is trained on patient-specific seizure and non-seizure feature-vectors to establish precise detection decision boundaries. 536 hours of patient tests show this leads to very good sensitivity, detection latency, and specificity (92%, 6.8sec, 0.2/hr respectively [1]).

The key strength of this approach from the power perspective is shown in the actual hardware measurements of Fig. 1, where local digital-processing, to derive the feature-vector, reduces the wireless data-rate by 43x and the overall system power, using a low-power short-range radio [2], by 15x. Each EEG channel in Fig. 1 consists of an electrode and the SoC (placed close-by for signal-integrity). The SoC integrates a low-power instrumentation amp (I-amp), 12b ADC, and low-energy digital processor to derive a feature-vector from each channel; the feature-vectors from all channels are concatenated for wireless transmission.

Low-Power Instrumentation Amplifier and ADC

The first stage of the I-amp, which is critical to its overall noise and power, utilizes chopper-stabilization [3] to mitigate $1/f$ noise degrading low-frequency EEG ($<200\text{Hz}$). A critical limitation to bio-potential sensing is large electrode offsets (EO) (up to 100's of mV) originating from charge accumulation at the skin-metal interface. EO cancellation through differential biasing of the amplifier input-stage [4] compromises noise-efficiency. Alternatively, cancellation of EO on the up-modulated inputs before the amplifier, via servo-biasing of series capacitors [5],

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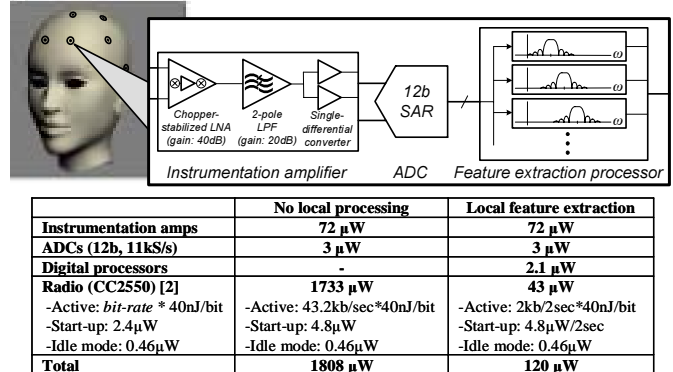


Fig. 1. SoC block diagram (for one channel) and power consumption (aggregated over 18 channels), highlighting benefit of local-processing for radio data-rate reduction.

degrades the input resistance (R_{IN}). Though practical for implanted electrodes, much weaker EEG signal strength on-scalp requires R_{IN} larger than $100\text{M}\Omega$. In both cases, EO tolerance is less than 50mV, and it restricts the minimum V_{DD} (to at least 1.8V), limiting power-efficiency.

The amplifier in Fig. 2a is optimized for noise-efficiency and operates below 1V while tolerating EO even larger than V_{DD} . EO are filtered-out before up-modulation via AC coupling, and chopper-modulation is performed at the op-amp input. Importantly, the virtual-ground condition here ensures that the charge on the op-amp's parasitic input capacitances, C_P (shown in Fig. 2b), is independent of the electrode signal. Consequently, even though the input modulator introduces effective switch-capacitor (SC) conductances between IN_+ and IN_- , these do not load the electrodes. They do, however, multiply with the input offset of the op-amp, giving rise to an offset current, $I_{OS,CHOP}$. To prevent this from saturating the amplifier through R_{HP} , which is intentionally large for a high-pass cut-off of less than 0.5Hz, a $G_M C$ -integrating servo-loop provides a DC current through R_{INT} to cancel $I_{OS,CHOP}$. Lastly, the op-amp of Fig. 2b employs two-stages with Miller compensation, but signal de-modulation is performed before the dominant-pole [5], so chopper-stabilization does not increase its required bandwidth.

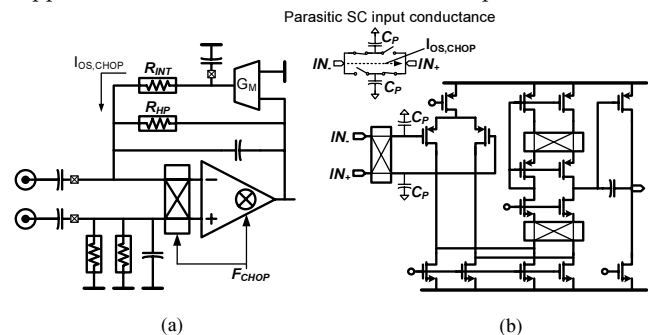


Fig. 2. Instrumentation amplifier (a) front-end chopper-stabilized LNA utilizing (b) folded-cascode op-amp.

The low cut-off frequencies necessary to detect EEG require large on-chip resistors, R_{HP} and R_{INT} , greater than $700\text{M}\Omega$. SC resistors are highly area-efficient and stable, but require

fast switching frequencies to minimize noise PSD elevation due to aliasing [3], leading to unmanufactureably small switch-capacitors. However, by using the *SC* transformer of Fig. 3, where current is conveyed from node *X* to *Y* through series-charging/parallel-discharging, the individual capacitors can be made 10x larger than that of a conventional *SC* (also shown) of an equivalent resistance.

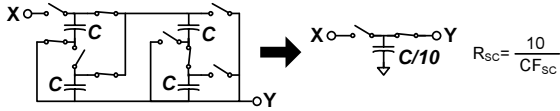


Fig. 3. 2-stage series-charging/parallel-discharging switch-capacitor topology to improve manufacturability of large resistances.

The 12b SAR ADC operates at 1V, consuming only dynamic-power, except in the comparator, where static preamps reduce hysteresis and improve accuracy. The ADC is fully differential, and, to avoid sampling input common-mode, its S/H uses no internal references, easing the comparator CMRR required [6].

Low-Energy Feature Extraction Processor

Extraction of spectral energy from each EEG channel, to derive the feature-vector, is implemented using a modulated filter bank (shown in Fig. 4), formed by seven FIR filters (*BPF0* – 6 centered from 2Hz-20Hz). Each of these is followed by a magnitude accumulator to derive the bin energy over a two second window. To minimize area, active-energy, and leakage-power, the minimum tolerable filter order, coefficient-precision, and accumulator width was validated by simulating the detection algorithm on 20hrs of pre-recorded patient data consisting of seizure and non-seizure EEG.

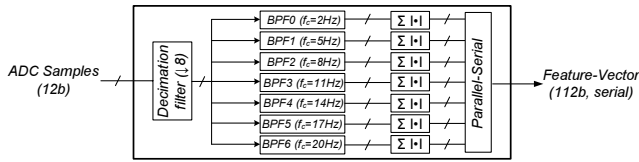


Fig. 4. Spectral feature extraction processor block diagram.

The optimal filter order was obtained by applying a decimation filter to the ADC samples. In addition to the 100Hz cut-off of the I-amp (set for general EEG acquisition), on-scalp EEG is affected by $1/f$ filtering through the skull, providing some band-limiting prior to ADC sampling; however, to ensure at least 20dB of aliasing suppression in the highest EEG band used for seizure detection (i.e. beta-band 13-33Hz), the ADC oversamples at 600Hz. Consequently, digital decimation (by eight) eases the filter implementation. The order and coefficient-precision of the decimator is 48 and 8b respectively, and that of the modulated filters is 46 and 8b respectively.

Supply voltage	1V
I-amp LNA power	3.5 μ W
I-amp input impedance	>700M Ω
I-amp noise (input referred, 0.5Hz-100Hz)	1.3 μ Vrms
I-amp electrode offset tolerance	>1V
I-amp CMRR	>60dB
ADC resolution	12b
ADC energy per conversion	250pJ
ADC max. sampling rate	100kS/s
ADC INL/DNL	0.68/0.66LSB
ADC SNDR	65dB
Digital energy per feature-vector	234nJ
Feature vector computation rate	0.5Hz
Total energy per feature-vector	9μJ

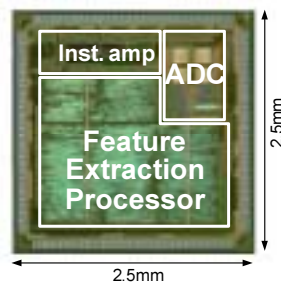


Fig. 5. IC performance summary and die-photo.

Measurement Results

The prototype IC is fabricated in 5M2P 0.18 μ m CMOS and operates from a single 1V supply. A performance summary is in Fig. 5 along with a die-photo. Fig. 6 shows the I-amp and

ADC output recording of actual EEG from the frontal (forehead) and occipital (behind the neck) scalp locations using Ag/AgCl electrodes. Periodic eye-blinks are visible on the frontal channel, and alpha-wave (indicating a relaxed eyes-closed state) is visible on the occipital channel, but then immediately abolished after eyes are opened. The FFT shows the occipital output during both eyes-open and closed, highlighting 8-13Hz activity of alpha.

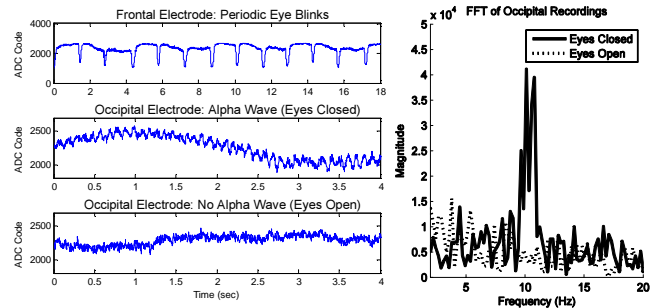


Fig. 6. EEG's captured using on-chip I-amp/ADC (without any post-processing) and FFT of occipital channel.

EEG Classification System Demonstration

Before patient seizure testing, complete EEG acquisition, feature-vector extraction, and final classification is demonstrated by configuring a one-channel system to detect a subject's relaxed state with eyes-closed (i.e. onset of alpha at occipital channel). First, to train the vector classifier, the IC generates 10 feature-vectors (requiring 20sec of monitoring) corresponding to both relaxed eyes-closed and eyes-open states. Then, the IC continuously generates feature-vectors and transmits them to the vector classifier for real-time alpha detection. Fig. 7 shows a segment of output feature-vector classification as well as the EEG (recorded by the IC, and annotated with the observed onset of alpha). Over a detection period exceeding 200sec, the onset of all alpha-waves are detected with less than 2.5sec latency.

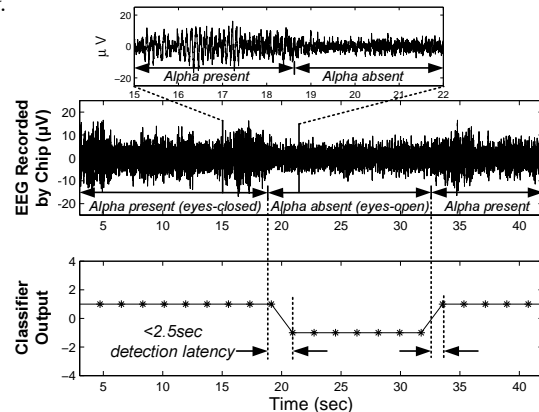


Fig. 7. Demonstration of EEG classification by IC trained to detect relaxed eyes-closed state characterized by alpha-wave.

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