Flexible Solar-energy Harvesting System on Plastic with Thin-film LC Oscillators Operating Above f_t for Inductively-coupled Power Delivery

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***Abstract*- This paper presents an energy-harvesting system consisting of amorphous-silicon (a-Si) solar cells and thin-film-transistor (TFT) power circuits on plastic. Along with patterned planar inductors, the TFTs realize an LC-oscillator that provides power inversion of the DC solar-module output, enabling a low-cost sheet for inductively-coupled wireless charging of devices. Despite the low performance of the TFTs (f_t=1.3MHz at a voltage of 15V), the oscillator can operate above 2MHz by incorporating the device parasitics into the resonant tank. This enables increased quality factor for the planar inductors, improving the power-transfer efficiency and the power delivered. Delivering power to an inductively-coupled load through 3cm-radius single- and double-layer inductors, the measured power-transfer efficiency is 22.6% and 31% (approaching the analytically-predicted bound), while the power delivered is 20mW and 22mW.**

I. Introduction

Thin-film electronics can be processed at low temperatures enabling the integration of diverse transducers with functional circuits on large, flexible sheets. This can lead to transformational systems for high-resolution sensing [1] and energy harvesting [2]. A critical limitation, however, is the low performance of thin-film transistors (TFTs), which typically have f_t around 1MHz. LC oscillators are a key building block in circuits for communication, control, and power conversion. An important characteristic is that they can operate above f_t and could thus play a key role in overcoming the limitations of thin-film systems.

In this work, we present a thin-film energy-harvesting system based on amorphous-silicon (a-Si) solar modules and TFTs. In contrast to previous work [2], we demonstrate energy-harvesting devices and power circuits in the same technology, thus enabling a path to low-cost, fully-integrated sheets for ubiquitous power conversion and delivery. Such sheets could be applied onto existing surfaces to convert them into charging stations for wireless powering of mobile devices. Compared to other designs [3], the proposed approach uses inductors rather than capacitors for coupling power to load devices. This enables greater power transfer for a given size (i.e., by a factor of 200 compared to [3]) as well as superior robustness to variations in proximity [4]. The key challenge with inductors, however, is reduced quality factor at low frequencies. We thus employ a thin-film LC oscillator as a power inverter to convert the DC solar-module outputs into AC waveforms, enabling inductive coupling at higher frequencies than that limited by f_t. The resulting topology also avoids the need for explicit switching control circuits, thus overcoming limitations to both performance and efficiency imposed by the TFTs. In the following sections, we analyze circuit tradeoffs, taking into account inherent component-level parasitics, which lead to a design-optimization methodology.

II. System Overview

Fig. 1 shows a block diagram of the energy-harvesting system. The solar module consists of solar cells in series operating at an output voltage V_{op} of 10-25V. Although LC oscillators offer the benefits mentioned, in order to function, they must have sufficient gain to meet the positive-feedback condition. This depends partially on device characteristics related to f_t (i.e., transconductance and capacitances), which are not favorable for TFTs; however, it also depends on the inductance-to-resistance ratio achievable with patterned planar inductors. We thus exploit the ability to create physically-large inductors on plastic, which can lead to large values of this ratio, enabling oscillations despite poor TFT characteristics.

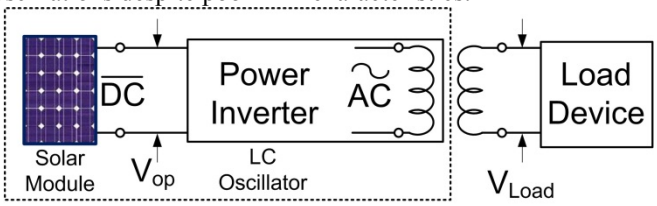


Fig. 1: Block diagram of thin-film energy-harvesting system.

Fig. 2 (left) shows the LC-oscillator including the circuit parasitics of importance. In addition to the TFT capacitances, the TFT gate resistances (R_{gate}) and inductor resistances (R_{ind}) are included. The gate resistances and capacitances are modeled as lumped elements since the frequencies of interest are much lower than that due to the associated time constant (which is several giga-Hertz). Nonetheless, R_{gate} is significant for the analysis due to the use of a bottom-gate TFT structure (as described in Sec. IV), which requires thin gate metallization in order to ensure reliable gate dielectric formation. At resonance, the parasitics can be represented as shown in Fig. 2 (right), where R_{Par} can be estimated by

$$R_{Par} \approx Q^2\left(R_{ind} + R_{gate}\right) = \frac{\omega^2 L^2}{R_{ind}+R_{gate}} = \frac{L}{C_{Par}(R_{ind}+R_{gate})}, \quad (1)$$

and C_{Par} can be estimated by taking into account Miller multiplication effects:

$$C_{Par} = 2 \times \left(C_{gd1} + C_{gd2}\right) + C_{gs1,2} + C_{ox} \approx 5 \times C_{ov} + C_{ox}. \quad (2)$$

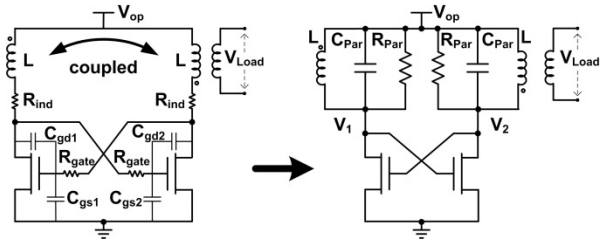


Fig. 2: LC oscillator with parasitics and equivalent circuit for analysis.

With TFT output resistances being much larger than typical values for R_{Par}, the positive-feedback condition requires that $g_m \times R_{Par} > 1$, leading to the following requirement:

$$\frac{g_m}{C_{Par}} \times \frac{L}{(R_{ind}+R_{gate})} > 1. \quad (3)$$

While the first term on the left represents a dependence related to device f_t, the second term suggests that this can be overcome by a suitable inductor. Fig. 3 plots $L/(R_{ind}+R_{gate})$ values, both from measurement (using prototyped inductors) and from simulated prediction (using [5]). Fabricated TFTs achieve a measured f_t of 1.3MHz (i.e., $g_m/C_{par} = 4.2 \times 10^6$ rad/s) at 15V, thus suggesting that the oscillation condition of Eq. 3 can be met with sufficient margin.

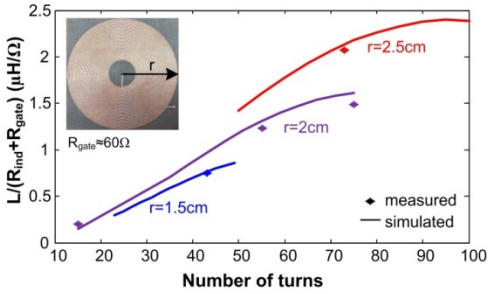


Fig. 3: $L/(R_{ind}+R_{gate})$ ratios for prototyped planar inductors.

III. Power Inverter Analysis And Optimization

Given the viability of thin-film LC oscillators, this section analyzes their efficiency and power-transfer capabilities when used as power inverters with an inductively-coupled load. As shown in Fig. 2, power is delivered to a single load by coupling the inductors in the two LC tank branches. The load causes an associated resistance to be reflected to the oscillator outputs. For analysis, as in Fig. 4, we use an equivalent topology, with equal-valued inductors for each oscillator branch, independently coupled to load inductors with nearly-perfect coupling efficiency (i.e., $k \approx 1$, which is reasonable for proximity power transfer). A reflected load (R_{Load}) hence appears in each branch. This has two effects: (1) R_{Load} impacts the positive-feedback condition, effectively altering the oscillation amplitude; and (2) R_{Load} splits the power extracted from the LC tank with R_{Par} in order to achieve the desired power delivery. These effects result in a design optimization methodology for maximum output power and efficiency. To analyze this, we define an oscillator strength parameter S; S is derived from the oscillation condition, and, as described in the following subsections, it suggests how the designer-selectable parameters, R_{Load} and g_m, should be set to maximize output power and efficiency:

$$S = g_m \times (R_{Load} \parallel R_{Par}). \quad (4)$$

An additional parameter of importance is the operating-point voltage of the solar-module (V_{op}), which affects both the absolute output power and efficiency that can be achieved.

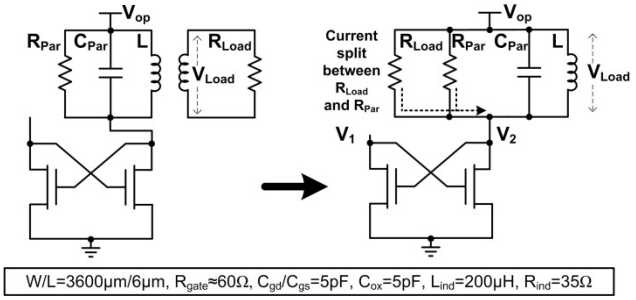


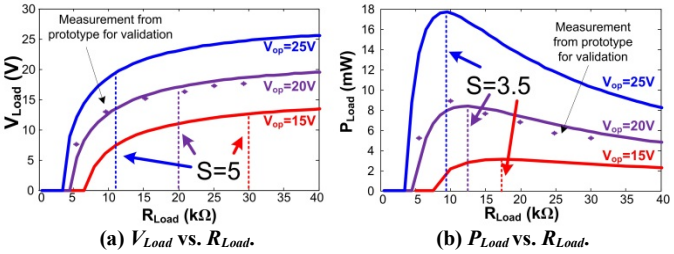
Fig. 4: Oscillator circuit with reflected load resistance; parameter values from a fabricated sample are shown for illustration.

A. Power-transfer Optimization

This section describes how the designer-selectable parameters should be set to optimally achieve a desired output power. For each oscillator branch, the power delivered to the load is:

$$P_{Load} = \frac{{V_{Load}}^2}{2 \times R_{Load}}, \quad (5)$$

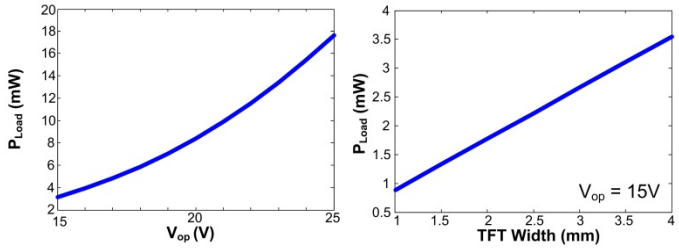
where V_{Load} is the amplitude of the AC oscillations. Eq. 5 suggests that R_{Load} should be minimized for maximum power transfer; however, due to its impact on S, R_{Load} affects V_{Load}. In order to sustain oscillations, reducing R_{Load} thus requires g_m to be increased. This can be achieved in two ways: (1) by increasing V_{op}, which raises the gate-overdrive of the TFTs; or (2) by increasing the W/L of the TFTs. Fig. 5(a) shows the effect of increasing V_{op} (based on transistor-level simulations using extracted SPICE Level 61 models for the TFTs; measurement results are also shown for $V_{op} = 20V$ to illustrate validity of the models). Due to the increased g_m, nearly full-swing oscillations can be achieved at reduced values of R_{Load} (as determined by S). Although increasing R_{Load} increases V_{Load} further, the effect saturates once sufficient S is achieved. Combined with the inverse dependence in Eq. 5, Fig. 5(b) shows that an optimal point thus occurs by balancing R_{Load}. The resulting optimal R_{Load} shown corresponds to a value of $S \approx 3.5$; however, as discussed in Sec. III-B, efficiency optimization requires a higher value ($S \approx 5$) for V_{Load} saturation. Nonetheless, with regards to P_{Load}, increasing V_{op} also increases the achievable V_{Load}, causing the effect in Fig. 6(a), where P_{Load} scales roughly cubically (as predicted by Eq. 5).



(a) V_{Load} vs. R_{Load}. **(b) P_{Load} vs. R_{Load}.**

Fig. 5: Effect of R_{Load} scaling on oscillation amplitude and output power.

Similarly, increasing W/L increases g_m, enabling oscillations to be sustained at a lower R_{Load}. However, raising W/L also increases C_{Par}, thereby reducing R_{Par} in proportion.



(a) P_{Load} vs. V_{op} **(b) P_{Load} vs. W/L**

Fig. 6: Scaling of output power through designer-selectable parameters.

As a result, S remains unchanged, causing V_{Load} to also remain unchanged. As shown in Fig. 6(b), P_{Load} thus scales linearly (due to R_{Load}).

B. Efficiency Optimization

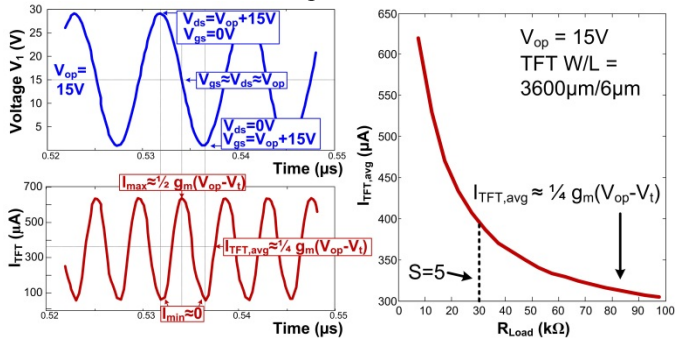
This section first examines the power consumed by the LC oscillator, and then uses this with the output power to analyze the power-transfer efficiency. Although the solar module's output voltage (V_{op}) and current are coupled, the circuit operates in a region close to the open-circuit module voltage, hence we approximate the average power consumed as

$$P_{avg} = V_{op} \times I_{TFT,avg}, \quad (6)$$

where $I_{TFT,avg}$ is the average current drawn by each TFT. During each cycle, the V_{gs} and V_{ds} of the TFTs oscillate in counter phase. For large oscillations of V_{Load}, the instantaneous TFT current (I_{TFT}) is thus near zero both when V_{gs} is maximum (due to low V_{ds}) and when V_{ds} is maximum (due to low V_{gs}). As shown in the simulation of Fig. 7(a), I_{TFT} is maximized when V_{gs}=V_{ds}=V_{op}, and the average current is thus roughly half this. As a result, the g_m in Eq. 4 is related to $I_{TFT,avg}$ as follows:

$$I_{TFT,avg} = \frac{1}{4} g_m (V_{op} - V_t). \quad (7)$$

Fig. 7(b) shows $I_{TFT,avg}$ with respect to R_{Load} (plotted for the circuit parameters in Fig. 4). $I_{TFT,avg}$ begins to saturate as R_{Load} is increased. This occurs due to increasing V_{Load}, which causes the current waveform (I_{TFT}) to reach the extreme values described above. This corresponds to S≈5.



(a)V_{Load} and I_{TFT} waveforms. **(b) $I_{TFT,avg}$ vs. R_{Load}.**

Fig. 7: Transistor-level simulation of the effect of R_{Load} on TFT current.

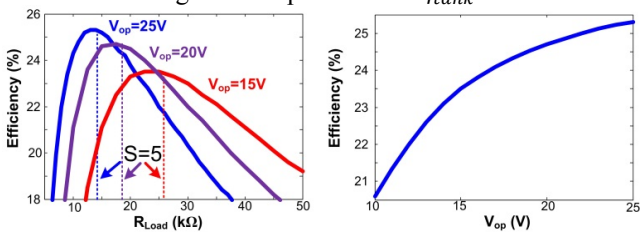
Now, the oscillator efficiency can be expressed as follows

$$\eta = \frac{\frac{V_{Load}^2}{2\times R_{Load}}}{V_{op} I_{TFT,avg}} = \frac{\left(\frac{V_{Load}^2}{2\times(R_{Load}\|R_{par})}\right)}{V_{op} I_{TFT,avg}} \times \frac{R_{Par}}{R_{Par}+R_{Load}} = \eta_{osc} \times \eta_{tank}, \quad (8)$$

where two effective efficiencies are explicitly defined: η_{osc} corresponds to the efficiency of maintaining oscillations in the presence of R_{Par} and R_{Load} (i.e., ensuring sufficient S); and η_{tank} corresponds to the efficiency with which current is delivered to R_{Load} versus R_{Par}.

From Eq. 8, the impact on η due to R_{Load} and g_m can be understood. In addition to its explicit impact, R_{Load} has an implicit effect through V_{Load} and thus $I_{TFT,avg}$; the profile in Fig. 5(a) shows the saturating effect of R_{Load} on V_{Load}. Thus, combined with the effect on $I_{TFT,avg}$ and the inverse impact of R_{Load} on η, the efficiency exhibits the optimal values shown in Fig. 8(a) at S≈5.

On the other hand, increasing g_m through W/L sizing causes a linear increase in P_{Load} (Fig. 6(b)), but also a linear increase in $I_{TFT,avg}$, due to TFT width scaling. As a result, η exhibits no net change with W/L. To understand the effect of increasing V_{op}, it is helpful to look at η_{osc} and η_{tank} separately. For η_{osc}, the achievable V_{Load} is increased linearly, $I_{TFT,avg}$ is increased quadratically (assuming square-law TFT behavior), and $R_{Load}\|R_{Par}$ can be decreased linearly for a required value of S (thanks to increased g_m); as a result, η_{osc} remains unchanged. However, the reduction allowed to R_{Load}, improves η_{tank}. As a result, the overall η initially improves, as shown in Fig. 7(b); however, this improvement eventually saturates according to the expression for η_{tank}.



(a) η vs. R_{Load}. **(b) η vs. V_{op}.**

Fig. 8: Simulations of harvester efficiency with respect to R_{Load} and V_{op}.

Given these effects, we can estimate a bound for the maximum overall efficiency achievable by the topology. Using Eqs. 4, 7, and 8, and assuming, V_{op}>>V_t and V_{Load}≈V_{op}

$$\eta_{max} \approx \frac{V_{op}^2 \times \frac{g_m}{S}}{2V_{op} \times \frac{1}{4} g_m V_{op}} = \frac{2}{S} \approx 40\%, \quad (9)$$

where S≈5 has been used based on discussed optimizations.

IV. Experimental Results

The energy-harvesting system is fabricated on 50μm-thick polyimide foil using patterned inductors of several sizes (i.e., radii of 2, 2.5, 3cm). All measurements are performed with an inductively-coupled load at a distance of 1mm. A sample photograph is in Fig. 9. TFTs with W/L of 3600μm/6μm are used with a layout optimized for minimum C_{gs}, C_{gd}, since maximizing g_m/C_{Par} is critical for the positive-feedback condition (Eq. 3). TFTs with 5μm gate-source/drain overlap, give a measured f_t of 1.3MHz (at 15V). Further reduction in overlap is unreliable for lithographic alignment on plastic.

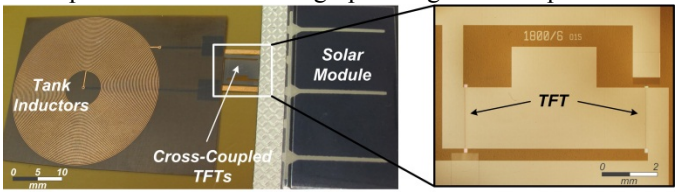


Fig 9: Sample inductively-coupled, energy-harvesting system on plastic.

Typical oscillator waveforms from measurement are in Fig. 10; while nearly full swing oscillations are achieved at 2MHz, oscillations with reduced amplitude are also observed at 3.64MHz. A performance summary is shown in Table I.

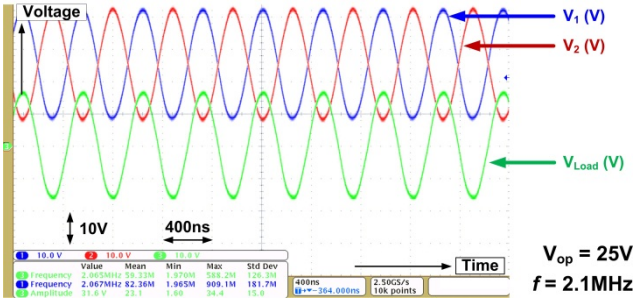


Fig. 10: Measured waveforms from system captured via oscilloscope.

Table I: Prototype system performance (shown for V_{op} =15V, 25V).

Inductor size	radius= 2, 2.5, 3cm		
TFT W/L	3600µm / 6µm		
f_t	1.3MHz (V_{op}=15V)		
Max. Freq.	2.1MHz (V_{Load}=16V), 3.64MHz (V_{Load}=5V)		
Coupling distance to load	1mm		
V_{op}	15	25	25 (2-layer inductor)
Solar Modules	180cm^2	300cm^2	300cm^2
Optimal R_{Load}	20kΩ	8kΩ	2kΩ
Max. P_{LOAD}	2.6mW	20.3mW	22.1mW
Max. η	15.4%	22.6%	31%

Fig. 11 shows the structure of a-Si NMOS TFTs as well as a measured typical I-V characteristic. Fabrication is achieved by PECVD deposition at low temperature (180°C), enabling the use of a polyimide foil substrate. For robustness under flexing, metal layers use chrome-aluminum-chrome stacks.

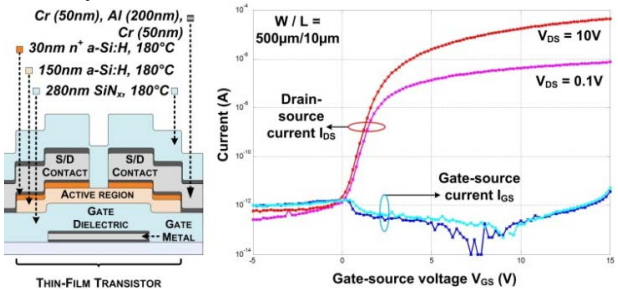
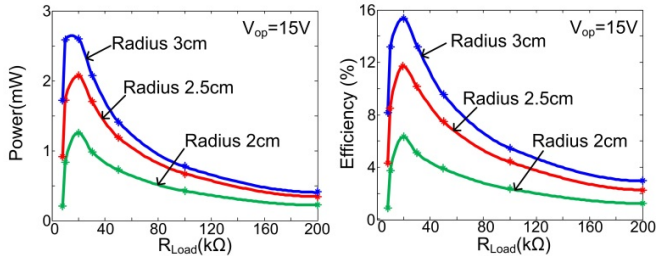


Fig. 11: Low-temperature processing of a-Si NMOS TFTs.

A. Power and Overall Efficiency versus R_{Load}

The measured output power delivered to a load (P_{Load}) and the overall efficiency (η) are shown in Fig. 12. Optimal values exist, as described in Sec. III-A & III-B. Additionally, physically-larger inductors lead to larger R_{Par}, improving η_{tank}, and thereby increasing the overall efficiency.

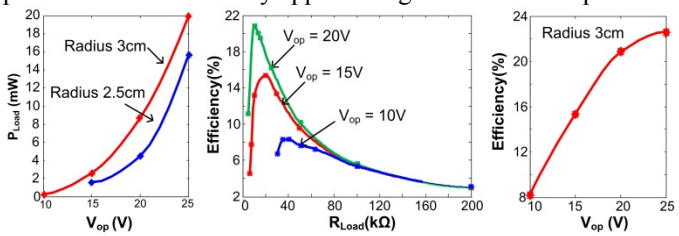


(a) P_{Load} vs. R_{Load}. **(b) η vs. R_{Load}.**

Fig. 12: Output power and efficiency measurements with R_{Load}.

B. Power and Overall Efficiency versus V_{op}

Fig. 13(a) shows P_{Load} with respect to V_{op} (for an optimal R_{Load}), Fig. 13(b) shows η with respect to V_{op} and R_{Load}, and Fig. 13(c) shows the optimal η with respect to V_{op} (for an inductor radius of 3cm). As described in Sec. III-A, Fig. 13(a) shows that P_{Load} increases approximately cubically with V_{op}. Larger inductors result in improved P_{Load} for the same reason as in Section IV-A. Further, as mentioned in Sec. III-B, η initially increases with V_{op} due to resulting improvement in η_{tank} through reduced R_{Load}. Since Fig. 13(c) approaches the voltage limit of the TFTs, to further explore this effect, we increase η_{tank} by explicitly increasing R_{Par}. R_{Par} can be increased by further increasing the inductor size or by stacking inductors in multiple layers; this causes the number of turns to effectively double, increasing L by a factor of four, while causing R_{ind} to increase by only a factor of two. The third column of Table I shows the measured results, demonstrating power-transfer efficiency approaching the bound of Eq. 9.



(a) P_{Load} vs. V_{op} **(b) η vs. R_{Load}.** **(c) η vs. V_{op}**

Fig. 13: Efficiency measurements with respect to V_{op}.

V. Conclusions

Thin-film systems face performance limitations due to the f_t limit of the TFTs. LC oscillators can resonate device capacitances with the tank inductors, enabling operation beyond the f_t. This, however, requires inductors with sufficiently small resistances. Thin-film systems fabricated on plastic substrates can achieve this through physically-large planar inductors that can be patterned on large substrates. We thus demonstrate operation of a thin-film LC oscillator above device f_t. We exploit this to then create an energy-harvesting system that uses an LC-oscillator-based power inverter to convert a DC solar-module output into an AC waveform for inductively-coupled wireless power delivery to load devices. The oscillator operates at a maximum frequency of 2.1MHz, and the system achieves an output power of up to 22mW, with a maximum power-transfer efficiency of 31%, which approaches the predicted maximum value for the topology.

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