A Figure of Merit for Oscillator-Based Thin-Film Circuits on Plastic for High-Performance Signaling, Energy Harvesting and Driving of Actuation Circuits

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For even basic sensing and energy-harvesting functions, large-area systems-on-plastic require digital oscillators as a key circuit block [1]. However, their use to generate control signals, or drive actuator/energy-harvesting circuits requires different performance metrics compared to conventional digital circuits. In this abstract we (1) propose a figure of merit for these applications and (2) show experimentally how the dependence of this new metric on the scaling of resistive loads differs from that of the conventional digital circuit metric of power-delay (PD) product [2].

Large output voltage swings are desirable for signal transmission, energy-harvesting or overdriving of a subsequent actuating circuit block. This is in addition to the usual low power and high frequency considerations. Thus we propose the following oscillator design metric: 

$$M_0 = \frac{f_{OSC} \times V_{SWING}}{P_{SUPPLY}}$$

where $f_{OSC}$ is the oscillator frequency, $V_{SWING}$ is the voltage swing at the oscillator output and $P_{SUPPLY}$ is the power consumption of the oscillator. This metric differs from standard power-delay product analysis ($M_{PD} = f_{OSC}/P_{SUPPLY}$), which simply quantifies the relation between oscillator power consumption and frequency, by now also incorporating a dependence on output voltage swing.

For this analysis, we fabricated 5-stage NMOS ring oscillators based on a-Si TFTs with doped a-Si thin-film integrated pull-up resistors (TFR) on flexible 50µm polyimide (Fig. 1). The TFT channel lengths are 6µm and mobility is 0.7 cm²/(Vs) (Fig. 2). Resistive load values are chosen as in Fig. 4 to initially maximize the output swing of the oscillator for $C_{LOAD}=10pF$ and are then all scaled by a resistor scaling factor (RSF), which is experimentally varied from 0.1 to 5. To enhance the drive capability of a reference (10pF-1nF) capacitive load ($C_{LOAD}$) whilst minimizing power consumption from the supply ($V_{DD}$) each inverter stage in the ring oscillator is up-sized from its predecessor by a constant ratio $r=1.6$. Fig. 6 illustrates typical oscillation waveforms at the output node of the oscillators as a function of $C_{LOAD}$. Measured parameters are similar on plastic and glass substrates, and experimental results were validated with a developed Level 61 a-Si TFT SPICE model.

Power consumption scales inversely with stage load resistances (Fig. 7), dominated by on-state static current. For lower power, larger load resistances are required. Frequency is inversely proportional to the signal propagation delay through the oscillator so with fixed W/L ratios for the driver TFTs, frequency scales down with larger loads due to the larger RC time constants from the pull-up paths (Fig. 8). For decreasing output $C_{LOAD}$, the frequency increases until the 10pF range when the load capacitance becomes comparable with the gate capacitance of the first oscillator stage. Larger resistors limit the critical output swing as the pull-up paths become weaker (Fig. 9), affecting the high output level. This effect is the same as that seen for large capacitances in Fig. 6. Conversely, with smaller loads, the low output level is degraded which also degrades the output swing. Increasing $C_{LOAD}$ also significantly limits the rise time of the output (Fig. 6) which further degrades the voltage swing.

As a constant $V_{DD}$ is used, the conventional PD product should remain fairly constant with load resistor scaling (Fig. 10), but for large load resistors the metric increases due to reduced swings in the oscillator stages and hence weaker pull-down paths. The new metric $M_0$ shows qualitatively similar behavior for low pull-up resistors, however differs substantially from the inverse power-delay product for large load resistors (large RSF) (Fig. 11). Because of the reduced voltage swing at large resistances (Fig. 9), $M_0$ decreases rather than increases, leading to an optimum load resistor scaling. Maximizing this metric becomes particularly important for $C_{LOAD}$ values comparable to gate capacitances in the oscillator, and an optimum choice of resistor loads is even clearer. A complication not embedded in our metric, however, is that low resistance loads built using the doped TFT a-Si layer, though achievable, require small L/W ratios, so load resistors may significantly dominate the area occupied by the oscillator compared to the driver TFTs.

In conclusion, a design metric for TFT digital oscillators used to drive actuator/sensor/power loads which require large voltage swings has been defined. The optimum load resistance for this metric is different from that for the power-delay product due to reduced voltage swings for large and small load resistive loads.

Fig. 1: Schematic cross-section of thin-film devices

Fig. 2: I-V characteristic of a-Si TFT on 50µm polyimide

Fig. 3: Resistance characteristics of n-doped a-Si resistors (L=20µm)

Fig. 4: Ring oscillator TFT and TFR circuit

Fig. 5: Flexible oscillator test sample; inset shows ring oscillator TFTs

Fig. 6: Ring oscillator waveforms for different output loads (RSF=1)

Fig. 7: Load scaling effect: power

Fig. 8: Load scaling effect: frequency

Fig. 9: Load scaling effect: output swing

Fig. 10: Optimization of load parameters with (inverse) of conventional power-delay metric $M_{PD}$

Fig. 11: Optimization of load parameters given proposed metric: $M_o = \left( f_{OSC} \times V_{SWING} \right) / P_{SUPPLY}$