Device Optimization for Integration of Thin-Film Power Electronics with Thin-Film Energy-harvesting Devices to Create Power-delivery Systems on Plastic Sheets

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***Abstract*- Large-area electronics, through the integration of energy-harvesting devices and TFTs, can provide complete powering systems with embedded power electronics on large, flexible sheets. The performance and application range of such systems depends strongly on the characteristics of TFTs and harvesting devices. We explore device constraints and show how novel thin-film circuit topologies, and their optimization (enhanced by large-area passive components), can mitigate these constraints. Two power-inversion systems serve as vehicles for analysis.**

I. Introduction

Low-temperature deposition of thin-films can enable the formation of energy harvesting devices on large, flexible substrates. Large physical dimensions enable harvesting of substantial power. The integration of power electronics using the same thin-film technology on a single substrate could form a path for creating complete systems on plastic for addressing a wide range of powering applications. We recently reported two systems that integrate amorphous-silicon (a-Si) solar cells with power inverters built using a-Si thin-film transistors (TFTs) on flexible plastic [1,2], one based on a Class-D power-transfer stage and the other on an LC-oscillator power-transfer stage (harvesting, under indoor conditions, up to 120µW and 22mW respectively). These systems enable near-field wireless power transfer to load devices for applications such as ubiquitous plug-free charging stations [1] and self-powered sensing skins, without requiring external power sources and/or control subsystems (as in [3]). The two systems represent a range of approaches for power systems illustrating how alternate circuit topologies can address critical TFT limitations, and the ways in which TFT characteristics then set system-level performance (output power and power-transfer efficiency).

II. TFTs for Power Circuits

Though TFTs allow transformational form-factors, their device characteristics raise critical limitations for power circuits. For quantitative analysis, amorphous silicon (a-Si) TFTs are considered. These represent the best established TFT technology, though the discussions and outcomes extend to other TFT technologies (e.g. organics, oxides, etc.).

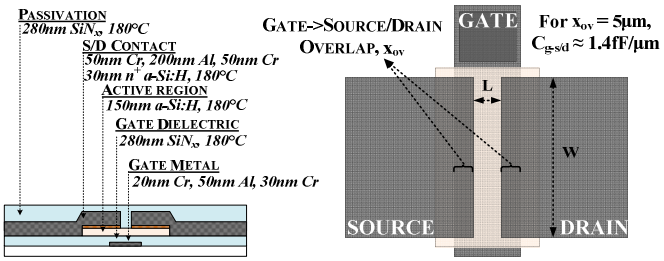


Fig. 1: Thin-Film Transistor (TFT) side and top views.

Fig. 1 illustrates the physical characteristics of our back-channel-etched a-Si TFTs. In addition to the choice of active material, of particular importance is the *gate-source/drain overlap* x_{ov} and *channel length* L, which determine the switching capacitances. Fig. 2 summarizes how the device aspects translate into electrical characteristics that give rise to critical implications for power circuits. The key points are summarized here and then illustrated in specific circuit topologies in the next section:

1. The disordered structure of a-Si results in low field-effect mobility. The on-current is thus low, which degrades the power-handling capacity of switches and amplifier stages.
2. The very low field-effect mobility of holes leads to very low-performance PMOS devices, making CMOS topologies unviable.
3. Large device features, required for processing margin in the presence of thermal expansion of free-standing flexible substrates, lead to high capacitances, which limit performance and increase switching losses.

Key a-Si TFT Properties	
Electron Mobility	1-2cm^2/Vs
Hole Mobility	<0.1cm^2/Vs
Gate Breakdown Field	>3MV/cm
TFT W/L	3600µm/6µm
Transconductance g_m at V_{gs}=V_{ds}=10V	9x10^{-5} A/V
Overlap Cap. C_{gd}/C_{gs} for overlap=5µm	5pF
Total TFT gate cap. C_{TFT}=C_{ox}+2xC_{gs}	15pF
Cutoff Frequency ft=g_m/(2πC_{TFT})	950kHz

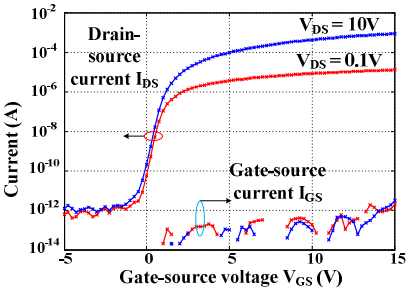


Fig. 2: a-Si TFT device properties lead to typical f_t of approximately 1MHz due to low g_m and large parasitic gate capacitances.

Given the substantial challenges posed by the active devices, a key approach in the topologies is an emphasis on passives [2]. By enabling energy storage and release (via electric and magnetic fields) capacitors and inductors play important roles in power circuits. The ability to pattern these with large physical dimensions can potentially improve their quality, offering a valuable lever in large-area electronics technologies.

III. Power Circuits

In this section, we analyze TFT characteristics in the context of power circuits. To facilitate analysis, the power-inversion system in Fig. 3 can be considered. It serves as a practical representative application, wherein a DC harvester output (e.g. from flexible solar modules) is converted to AC for an integrated system for proximity wireless-charging of loads. For generality, we analyze the power circuits referring to three sub-blocks: (1) power-transfer stages; (2) power-amplification/-processing stages; and (3) control stages.

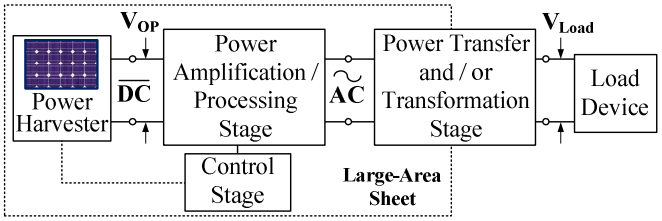


Fig. 3: Power inversion system as a representative application for thin-film power circuits.

A. Power-transfer Stages

Capacitors and inductors are vital for power conversion (i.e. impedance, voltage-/current-level transformation). Here, their analysis is pursued from the perspective of power transfer. Particularly for wireless power transfer, the topologies shown in Fig. 4 can be used. Inductive transfer offers important benefits. First, inductors offer increased robustness to proximity variations [4]. Second, they allow the transfer voltage to be chosen easily and with great flexibility. This is useful in the context of TFT technology, since, while the achievable on current is low, the gate breakdown voltage can be high (Fig. 2). As a result, power handling may be enhanced by increased voltage on the TFT-circuit side, yet allowing for potentially lower voltages as required on the load side. However, TFTs also raise important considerations with respect to the frequency of the power signal. As shown in Fig. 4, inductive transfer substantially benefits from increased frequency; the low performance of TFTs (f_t<1MHz) thus potentially poses a key challenge, though for specific topologies this may be overcome (as described below).

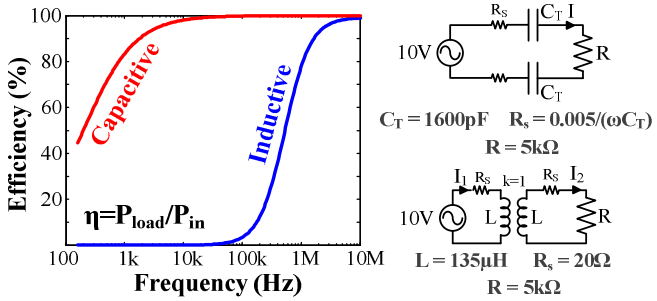


Fig. 4: Efficiency of capacitive vs. inductive power-transfer stages.

B. Power-amplification/-processing Stages

Power-amplification stages process the power signal that is ultimately delivered to the output. First, we consider a Class-D power stage, since this has the potential to achieve very high efficiency. In a Class-D stage, power processing is performed via switches, with the intention that all of the current drawn is delivered to the output. A critical challenge with TFT technology is that the absence of CMOS devices limits the ability to form high-quality switches at all of the voltage levels in the circuit (e.g. at high bias voltages, the extremely low current achievable with PMOS devices precludes efficient switching). Fig. 5 shows a Class-D power-inverter stage, which achieves effective switching using only NMOS devices [1]. This implies switching only at low bias voltages (with respect to the gate control voltage). Power inversion is thus achieved using two solar modules S1/2 (with operating voltage V_{OP}) whose polarity with respect to the output is reversed. Two NMOS power switches M1/2, each at the cathode of a solar module, alternately gate the solar module's current to achieve an AC output.

Fig. 5 shows the output power from the stage with respect to the switching frequency F_{SW}. Three regimes set by the TFT operation are identified. Initially, output power increases with F_{SW} according to $P_{OUT}=2C_T(V_{OP}-V_{LOAD})V_{LOAD}F_{SW}$. However, at some frequency ($F_{SW}\approx$10kHz) the output power saturates, because the TFT switches are unable to provide sufficient current to fully charge the transfer capacitors C_T to $\pm V_{OP}$. Continued increase of F_{SW} eventually leads to a f_t-limited regime where the TFT currents are shunted by their own capacitances rather than charging C_T. The f_t limitation in this topology makes capacitive transfer preferable (Fig. 4). As we describe in the next section, in a TFT technology, the power consumed by the switching-control circuits can be significant; the control-circuit power increases with frequency, making the transition region between the first two regimes most efficient [1].

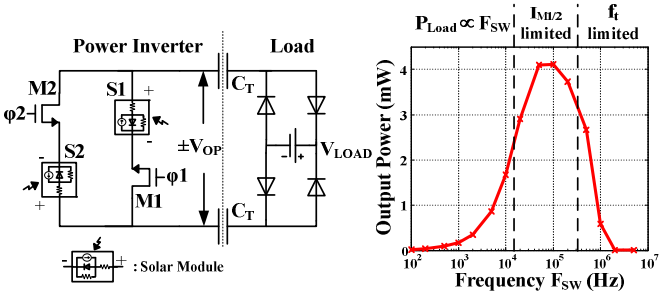


Fig. 5: Class-D power-transfer stage, achieving switching using only NMOS devices [1]. Plot shows output power scaling with frequency.

The second stage considered is a Class-A stage. In a Class-A configuration, biasing currents are consumed within the stage, and only a portion of the current drawn is delivered to the output. This implies potentially lower efficiency than the Class-D stage. However, as described below, Class-A raises several advantages for overcoming TFT limitations. Fig. 6 shows the Class-A stage considered in [2]. A key aspect of the stage is that it is a resonant circuit. This has two important implications: (1) it resonates with TFT capacitances, enabling frequencies not limited by f_t, and thus making inductors viable; and (2) it precludes the need for explicit switching control, avoiding additional overheads.

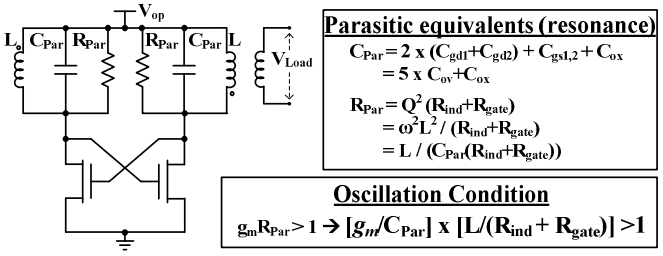
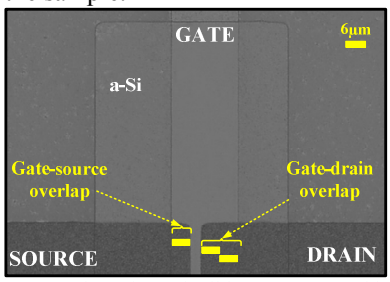


Fig. 6: Resonant Class-A power stage; resonant operation requires meeting a positive-feedback condition.

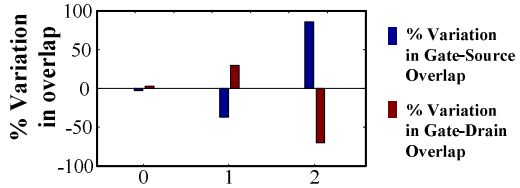
In order for the resonant stage to function, however, certain device conditions must be met; as described in [2], these conditions do not depend solely on the TFTs, and can in fact exploit favorable characteristics achievable via the

large-area passives. Fig. 6 identifies the positive-feedback condition required for resonant oscillations. The two critical terms show an explicit dependence on the TFT characteristics (g_m/C_{Par}) and a partial dependence on the characteristics of the inductors ($L/(R_{ind}+R_{gate})$), which can be formed by patterning metal spirals.

Unfortunately, g_m/C_{Par}, which results from the cross-coupled topology and depends on both the TFT overlap and gate-oxide capacitances, is in fact a more stringent parameter than f_t. Fig. 7a shows a micrograph, highlighting the physical TFT features involved. The necessity for large overlaps arises in particular for circuits processed on free-standing plastic due to substrate expansion/contraction during processing as well as built-in stresses of device films [5]. This results in a lower limit to gate-source/-drain overlap to maintain reliable alignment between mask stages during lithography. Both the minimum gate length (L=6µm) and the overlaps (x_{ov}=5-15µm) in our process are chosen based on characterization of devices deposited at 180^{0}C in order to achieve high circuit yield on foil, over an area ~60cm^2. Note, while equal gate-source/drain (S/D) overlaps are nominally designed, the actual overlaps at our shown limit are unbalanced (Fig. 7a). Fig. 7b shows the overlap variation for TFTs affected by stresses and thermal expansion at a distance from the sample center (nominal x_{ov}=10µm; positive variation indicates larger overlap). The sign of source- vs drain- overlap deviation depends on direction traversed from the center of the sample.



(a) TFT on 50µm polyimide, with all layers processed below 180 ℃.



(b) Source and Drain overlap variation across a sample due to substrate deformation.

Fig. 7: Micrograph and physical characterization on TFT on plastic.

Despite the dependence on the stringent TFT parameter, the resonant stage (Fig. 6) can in fact operate robustly thanks to the influence of the inductors in the second parameter. TFTs do still have an important impact, though, through R_{gate}. In a bottom-gate staggered TFT, a thin gate metal is used (~100nm) to ensure step coverage by the dielectric; however, this leads to large R_{gate}. Fig. 8 shows simulations and experimental data suggesting one method for diminishing the impact of R_{gate}. Patterning a large spiral and then increasing number of turns increases both R_{ind} and L, somewhat reducing the impact of R_{gate}.

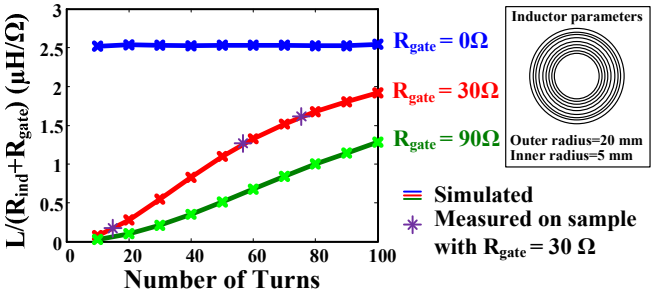
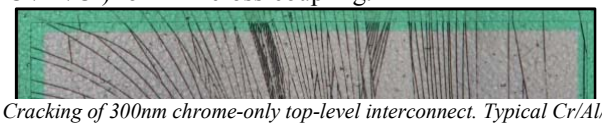


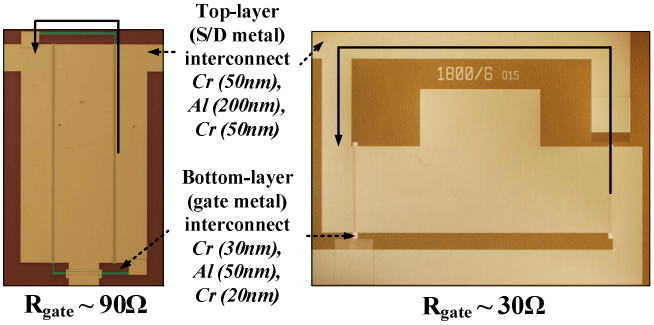
Fig. 8: Patterned inductor L/R ratio dependence on number of turns with and without effect of R_{gate}. Simulated results obtained using [6].

However, R_{gate} can also be substantially reduced through optimization of the deposited thin-films:

1. The gate metal can use an aluminium layer between chrome layers (Cr is required to prevent diffusion of Al through the gate dielectric and to improve adhesion to the substrate). This substantially lowers the sheet resistance to <0.6Ω/sq, compared to ~10Ω/sq. with solely Cr gate metal. This metal stack also substantially minimizes the impact of cracking of interconnect (Fig. 9a) due to thermal stresses during processing on plastic substrates
2. Circuit layout optimization, as illustrated in Fig. 9b, can employ thick (~300nm) top-level interconnect (also Cr/Al/Cr) for TFT cross-coupling.



(a) Cracking of 300nm chrome-only top-level interconnect. Typical Cr/Al/Cr interconnect on polyimide with minimal cracking is shown in Fig. 9b.



(b) Layout effects on gate resistance R_{gate}, with cross-coupling achieved using the bottom gate metal layer (left) or the top S/D metal layer (right).

Fig. 9: Means of optimizing R_{gate}

As a result of the circuit-device interactions, Table 1 shows typical parameter values that indicate that even though the circuit topology raises dependencies on parameters somewhat more stringent than fundamental device parameters, robust oscillations can be achieved in practice.

Table 1: Resonant circuit operational conditions due to circuit topology.

DEVICE AND PASSIVE-RELATED PARAMETERS		CIRCUIT-ENHANCED PARAMETERS	
g_m/C_{TFT} ('f_t') (rad/s)	L/R_{ind} (H/Ω)	g_m/C_{Par} (rad/s)	$L/(R_{ind}+R_{gate})$ (H/Ω)
6 x 10^6	2.7 x 10^{-6}	3 x 10^6	1.2 x 10^{-6}

In this case, the frequency is set by L and C_{Par}, rather than the TFT f_t (950kHz), enabling fairly high frequencies (>3.5MHz achieved), at which patterned inductors become viable.

C. *Control Stages*

Control stages do not process the power signals ultimately appearing at the circuit outputs, but they are required for power-processing stages, and thus impose overheads that degrade efficiency. In this analysis, we treat the losses involved in driving the power stages as control overhead, for instance switching M1/2 in the topology of Fig. 5. For the TFT technology, the absence of CMOS devices implies that the power of the switch drivers will be elevated compared to just switching losses. Nonetheless, the power consumed by the control stages scales with the load capacitance, and thus the following relation still represents an important figure of merit, M, for the power devices

$$M = \frac{I_{out}}{C_{gate-M1/2}} \propto \frac{\mu_{FET}}{L(L + x_{ov})}, \quad (1)$$

where mobility and feature-size limitations, due to low-temperature processing on flexible substrates, have been discussed previously.

For digital control, such as that required for the topology of Fig. 5, NMOS-only logic structures can be formed. For instance, the synchronous control for M1/2 is achieved in [1] using the structure of Fig. 10. The output stage of the ring oscillators is coupled via a NOR structure to achieve non-overlapping digital signals, and the alternating voltage bias of the NMOS switches is handled using level-shifting capacitors and TFT diodes. To achieve large-swing digital signals, thin-film resistors are developed, compatible with the TFT process. These are achieved using n^+ doped a-Si over an intrinsic a-Si layer. The resulting resistance is 30MΩ/sq. The NMOS-only logic style leads to conduction losses (static power). These are set by the size of load resistances (R_{STAGE}) used, which are in turn set by the load capacitances ($C_{STAGE}/C_{gate-M1/2}$) and gate delay (t_{STAGE}) required. TFT capacitances thus impact the control-circuit's conduction loss, which, for t_{STAGE} switching at the 50% point, can be modeled as

$$P_{LOSS} = \sum_{\text{N gates at logic 0}} \frac{V_{OP}^2}{R_{STAGE}} = \sum_{\text{N gates at logic 0}} \ln(2) \frac{V_{OP}^2 C_{STAGE}}{t_{STAGE}}, \quad (2)$$

For the switch drivers in Fig. 5, Fig. 10 shows control-stage loss with respect to M1/2 capacitances.

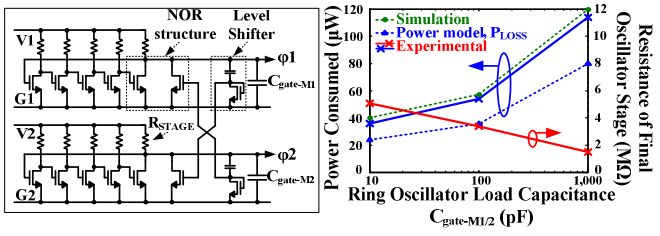
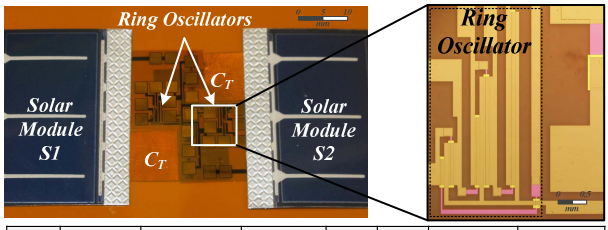


Fig. 10: Improvement of power-efficiency (at constant oscillator frequency) can be achieved through reduction of $C_{gate-M1/2}$ which allows for oscillator load resistance scaling. Power results are shown from simulation, a static power model and experimental measurements.

IV. Conclusions

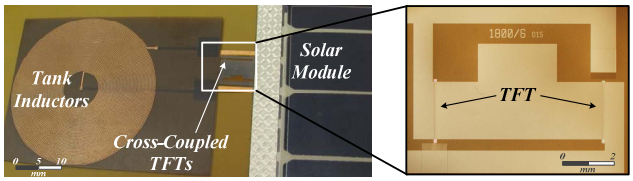
Large-area electronics makes a wide-range of highly compelling energy-harvesting devices possible. The ability to integrate TFTs raises the possibility of creating complete powering systems. However, the distinctive characteristics and limitations faced with TFTs makes the consideration of alternate topologies necessary for the power circuits. This work considered alternate topologies for power-transfer, power-amplification, and control stages. It analyzed the critical characteristics of the devices, both TFTs and passives, involved in setting the system-level performance. TFT optimizations and thin-film devices were considered, specifically in the context of achieving manufacturable power systems on flexible substrates.

Based on the analyzed approaches, two power systems for wireless load charging from solar-energy harvesting were previously reported. The achieved performance of these systems is summarized in Fig. 11 and 12 [1,2]. The oscillator-based system achieves high efficiency at high output power levels for a given size of passive thanks to its ability to operate at high frequencies, enabling high quality inductive coupling. In addition, no efficiency-reducing overheads are introduced that arise from the necessary use of control stages as in [1].



V_{OP} (V)	Solar Modules (cm²)	Power Switch Size (μm)	Transfer Capacitor (nF)	f_{OSC} (kHz)	P_{OSC} (μW)	P_{LOAD} (μW)	η (%)
8.4	100	3600/6	0.5→2	4.5	336	47→120	11 → 22

Fig. 11: Prototype of capacitive energy harvesting block with typical performance achieved [1]. Inset shows ring oscillator which generates the control signal for either M1 or M2.



Inductor size	radius= 2, 2.5, 3cm
TFT W/L	3600μm / 6μm
Max. Freq.	2.1MHz (V_{Load}=16V), 3.64MHz (V_{Load}=5V)

V_{op}	15	25
Solar Modules	180cm²	300cm²
Max. P_{LOAD}	2.6mW	20.3mW
Max. η	15.40%	22.60%

Fig. 12: Prototype of inductive energy harvesting block with typical performance above f_t shown [2]. Inset shows tank TFTs.

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