

# A Fully Self-Powered Hybrid System Based on CMOS ICs and Large-Area Electronics for Large-Scale Strain Monitoring

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## Abstract

Large-area electronics (LAE) enables diverse transducers on large, flexible substrates ( $\sim 10m^2$ ), making possible expansive sensor arrays and energy harvesting devices. We present a second-generation system for high-resolution structural-health monitoring of bridges achieved by combining LAE with CMOS ICs in a scalable architecture. It aims to enable strain sensing scalable down to cm-resolution over the large-area sheets. Compared to previous work [1], the system presents several advances, including self-powered operation with embedded energy harvesting, generalized readout and control interfaces for sensor arrays based on thin-film transistors (TFTs), and full integration of instrumentation and communication circuits for multi-sensor acquisition, digitization, and self calibration. The instrumentation subsystem achieves multi-channel strain sensing with sensitivity of  $23\mu\text{Strain}_{\text{RMS}}$ , at an energy/measurement of 148nJ and 286nJ for readout and sensor-access control, respectively. The power-management subsystem achieves 30% efficiency for power inversion and inductive power delivery using a thin-film harvesting circuit with a solar module, and 80.5% overall efficiency for generating three voltage supplies via CMOS DC-DC converters.

## System Approach

A key insight of the design is that LAE and CMOS introduce complementary advantages for power-management, sensing, and communication subsystems. Fig. 1 shows the system block diagram, which combines CMOS ICs with low-temperature-processed LAE sensors and circuits based on amorphous silicon (a-Si) ( $180^\circ\text{C}$  [2]). System scalability is achieved by introducing multiple ICs and replicating the LAE blocks over a large-area sheet; the critical limitation to scalability is the interfaces required between the two technologies. To address this, non-contact interfaces are used, with inductors and capacitors patterned on the LAE sheet and on the flex-tape IC package, as shown. This enables low-cost system assembly via sheet lamination (which we achieve with adhesive thickness  $\sim 100\mu\text{m}$ ), avoiding metallurgical bonds. The scalable interfaces thus enable hybrid CMOS and LAE architectures, exploiting the strengths of both technologies: (1) for power management, LAE enables large solar modules ( $\sim 300\text{cm}^2$ ) capable of harvesting substantial power as well as TFT power converters for AC delivery over inductive interfaces, while CMOS enables voltage regulation and DC-DC conversion for on-chip supplies; (2) for sensing, LAE enables large-area arrays of strain sensors as well as TFT circuits for sensor accessing and sensor-output modulation, while CMOS enables precision sensor readout and digitization; and (3) for communication, LAE enables interconnects for low-energy signaling over the large-area sheet, while CMOS enables self-calibrating data transceivers.

## Power-management Subsystem

Fig. 2 shows the power-management subsystem. The LAE domain consists of a thin-film a-Si solar module and a TFT power inverter, to deliver AC power to the IC over an inductive interface. Compared to capacitive transfer, this permits current coupling for higher power delivery at the IC voltage limit (3.6V). The inverter is a free-running LC oscillator, avoiding overhead from explicit control circuits. The inverter efficiency depends on inductor losses [3]; low resistance is achieved by patterning physically-large inductors on the LAE sheet (3cm radius),

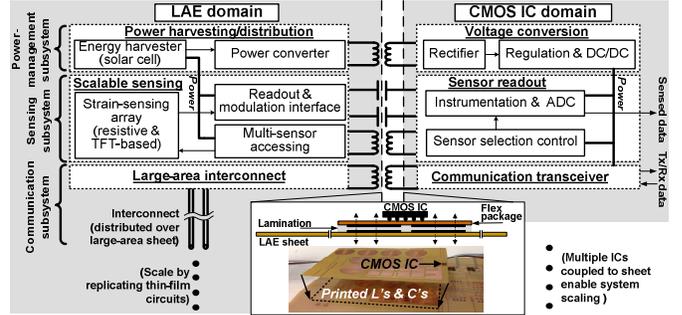


Fig. 1. Self-powered hybrid system for large-scale strain sensing.

which resonate with the TFT capacitances at 700kHz, yielding a high quality factor of  $\sim 54$ . With 25V solar modules, the power-transfer efficiency of inductive delivery is 30%, and the max. output power is 22mW, well beyond the system needs.

The CMOS domain consists of a rectifier for charging up an energy-storage capacitor  $C_{\text{STO}}$ , as well as a hysteretic low-level monitor and overvoltage-protection circuit (both using reference voltages from the on-chip bias generator) to ensure the output  $V_{\text{STO}}$  is within the functional limits. To generate the desired supplies, a request signal (REQ) is asserted, activating the low-level monitor, which then asserts an enable signal (ENb) when sufficient  $V_{\text{STO}}$  is reached. ENb activates the clock generator for three integrated DC-DC converters, creating 0.6V, 1.2V, and 2.4V supplies. The DC-DC outputs are monitored via comparators, and the output voltages are regulated by circuitry that enables the switching signals ( $\phi/2$ ) when droops are sensed. The ready signals (RDY1/2/3) are Nanded to derive an acknowledgment (ACKb).

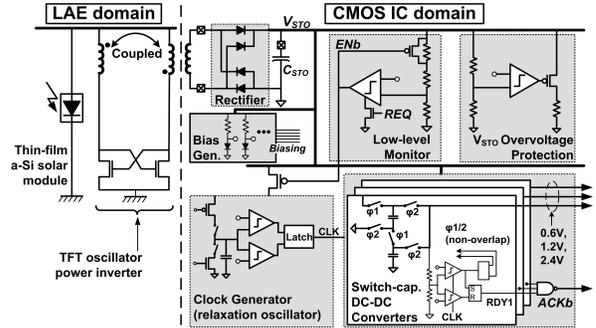


Fig. 2. Power-management subsystem with TFT power inverter.

## Sensing and Communication Subsystems

Fig. 3 shows the sensing subsystem. While biasing and readout of thin-film resistive-bridge strain sensors is supported (as in [1]), a key advancement is the readout of TFT-based sensors. Since a wide range of reported sensors are based on the physical responses of TFTs [4] (e.g., strain sensing uses mobility response [5]), the architecture can be generalized for broad sensing applications. The challenge with TFT sensors is that the output current must be modulated for readout by the IC over non-contact links. The LAE domain thus consists of a thin-film differential Gilbert-cell modulator, as shown. Individual sensors are selected by sequential enable signals (EN[i]), generated as described below. A reference sensor for each axis of strain sensing is achieved by orienting a TFT sensor orthogonally.

The CMOS domain consists of a synchronous  $G_M$ -C integrator and modulation-signal generator for sensor readout. Signal

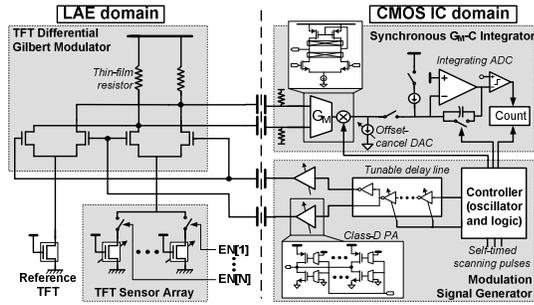


Fig. 3. Sensing subsystem for TFT-based strain sensors.

amplification and demodulation is performed by a  $G_M$  stage. An output DAC (9b) enables a user-initiated calibration phase to cancel sensor and interface offsets. Digitization is then performed via a 10b integrating ADC. For synchronization, the Gilbert-cell modulation signal is generated via a digital delay line with a tunable-drive class-D power amplifier at the output. Given the performance limits of the Gilbert-cell TFTs ( $f_T \approx 1\text{MHz}$ ), a modulation frequency of 100kHz is used.

Fig. 4 shows circuits for multi-sensor accessing. The LAE domain consists of a scan chain that generates sequential sensor-enable signals (EN[i]) via three-phase control signals (SCAN1-3) and global reset (GRST). With only NMOS devices available in a-Si, three-phase control enables a bootstrap capacitor to be used to precharge, drive, and then reset a pass transistor, which thus ensures full-swing logic levels. To generate SCAN1-3, two options are made available. First, for IC-controlled timing, the IC can provide AC modulated control signals (SCAN\_IC1-3). These are stepped up from 2.4V (IO level) to  $>6\text{V}$  (LAE-circuit level) via inductive interfaces. To maximize interface efficiency, LAE rectifiers based on nanocrystalline-silicon (nc-Si) Schottky diodes are developed; though processed at  $180^\circ\text{C}$ , these have  $>1000\times$  higher current density than the a-Si diodes in [1]. This enables small devices with low capacitances, allowing a high resonant frequency ( $\sim 3\text{MHz}$ ) to maximize the quality factor of the inductors. Second, LAE-controlled self timing is also enabled to eliminate inductive interface losses. Three LAE ring oscillators coupled with a wired-NOR at the output generate the non-overlapping signals; the resulting SCAN1-3 signals are also provided to the IC (over capacitive interfaces) and converted into pulses to generate control signals for the readout circuit.

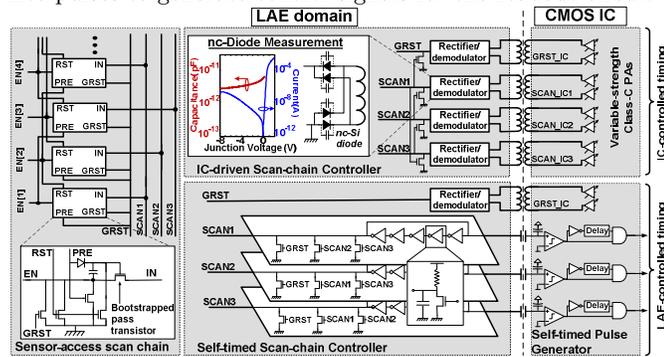


Fig. 4. Large-area sensor-array accessing circuits, consisting of a thin-film scan chain controlled by two optional methods.

The communication subsystem uses CMOS on-off-keying transceivers and employs large-area interconnect in the LAE domain for low-energy signaling [1]. Since the interconnect impedance is unpredictable, the CMOS transmitter calibrates its carrier frequency via a DCO to the resonant point by using its local receiver to sense the transmit amplitude. A dual-slope ADC is integrated in this design to enable DCO self calibration.

### Measurement Results

The system is prototyped via 130nm CMOS ICs and LAE samples fabricated on  $50\mu\text{m}$  polyimide (Fig. 5), and strain tests

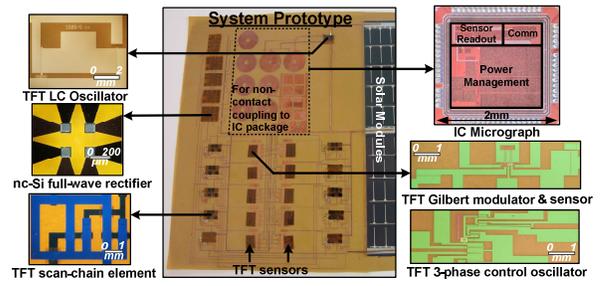


Fig. 5. Photograph of system, including 130nm CMOS IC and a-Si samples fabricated on  $50\mu\text{m}$  polyimide; strain tests use a cantilever beam in the lab.

use a cantilever beam in the lab. Fig. 6 shows oscilloscope-measured waveforms for the entire system, including power management, sensing, and communication. Fig. 7 shows a measurement summary. The sensing subsystem is characterized using both TFTs and calibrated resistors; from resistive measurement, readout noise/linearity is  $23\mu\text{Strain}_{\text{RMS}}/29\mu\text{Strain}$  (with gauge factor of 2). Results for actual strain sensing (resistive and TFT) from the beam are also shown. The energy/meas. is 148nJ and 286nJ for readout and scan-chain driving. The DC-DC converter efficiencies are shown; the overall efficiency across three DC-DCs is 80.5%, with most power from the 2.4V supply. The communication energy is 14.6pJ/b and 4.3pJ/b (Tx/Rx @ 7.5m, 2Mb/s), and 17 $\mu\text{J}$  for the carrier-frequency calibration loop.

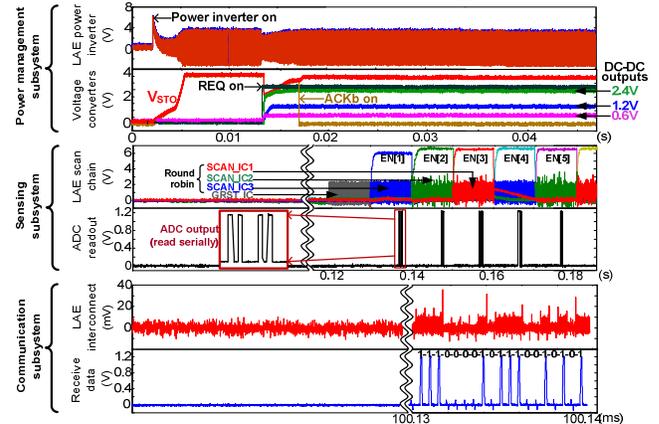


Fig. 6. Measured waveforms of prototype from oscilloscope capture.

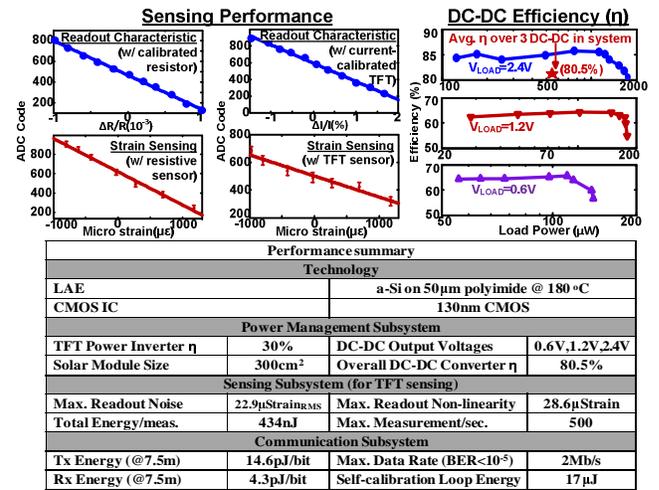


Fig. 7. Measurements, including strain tests using beam in lab.

### References

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