Large-Scale Sensing System Combining Large-Area Electronics and CMOS ICs for Structural-Health Monitoring

Yingzhe Hu, *Student Member, IEEE*, Warren S. A. Rieutort-Louis, *Student Member, IEEE*, Josue Sanz-Robinson, Liechao Huang, *Student Member, IEEE*, Branko Glišic, James C. Sturm, *Fellow, IEEE*, Sigurd Wagner, *Fellow, IEEE*, and Naveen Verma, *Member, IEEE*

***Abstract*—Early-stage damage detection for bridges requires continuously sensing strain over large portions of the structure, yet with centimeter-scale resolution. To achieve sensing on such a scale, this work presents a sensing sheet that combines CMOS ICs, for sensor control and readout, with large-area electronics (LAE), for many-channel distributed sensing and data aggregation. Bonded to a structure, the sheet thus enables strain sensing scalable to high spatial resolutions. In order to combine the two technologies in a correspondingly scalable manner, non-contact interfaces are used. Inductive and capacitive antennas are patterned on the LAE sheet and on the IC packages, so that system assembly is achieved via low-cost sheet lamination without metallurgical bonds. The LAE sheet integrates thin-film strain gauges, thin-film transistors, and long interconnects on a 50-µm-thick polyimide sheet, and the CMOS ICs integrate subsystems for sensor readout, control, and communication over the distributed sheet in a 130 nm process. Multi-channel strain readout is achieved with sensitivity of 18 $\mu\text{Strain}_{\text{RMS}}$ at a readout energy of 270 nJ/measurement, while the communication energy is 12.8 pJ/3.3 pJ per bit (Tx/Rx) over a distance of 7.5 m.**

***Index Terms*—Choppers (circuits), coupled circuits, flexible electronics, sensors, thin-film transistors.**

I. Introduction

THE explosion in embedded computing capability has led to high-value devices for sensing applications. However, the number of embedded signals of interest in emerging applications is growing rapidly, making the ability for systems to acquire signals on a proportionate scale a critical limitation. As an example, sensing for smart cities requires a high-level of instrumentation in the urban environment [1]. Structural-health monitoring (SHM) of critical infrastructure such as bridges is one such case, with the aims of avoiding catastrophic failures and optimizing maintenance investments [2]. The challenge is that reliable, early-stage detection requires sensing over large regions of the structure but with very fine spatial resolution. Current state-of-the-art technologies provide point sensing that is insufficient in scalability [3]; studies based on modal analysis and/or wave propagation (using accelerometers, ultra-sound, piezoelectrics, etc.) have shown limited damage localization capabilities with sparsely-spaced transducers [4], [5], while studies based on fiber-optic strain sensors have shown that damage even 50 cm away cannot be reliably detected [6]. This implies the need for very dense sensing.

We present a strain-sensing system that can scale to high resolution over large surfaces. This is achieved by combining large-area electronics (LAE), which enables large-scale sensor arrays and control circuits on a flexible sheet, with CMOS ICs, which enable low-energy functionality for readout, control, and data aggregation over the distributed sensors. The entire system is scalable by patterning multiple LAE sensor arrays and coupling multiple ICs through specialized interfaces. In the rest of the paper, LAE technology and the merits of combining it with CMOS are briefly described in Section II; then, scalable hybrid architectures for the subsystems are introduced in Section III, along with implementation details; finally, system prototype, measurement, and demonstration results are presented in Section IV. Conclusions are provided in Section V.

II. LAE and CMOS ICs for Large-Scale Hybrid Systems

LAE raises transformational capabilities for sensing; combining it with CMOS ICs can lead to complete systems for large-scale sensing. In particular systems require efficient functionality for sensor readout, communication, and ultimately embedded computation. This work focuses on scalable architectures that combine LAE and CMOS ICs, leveraging the strengths of both technologies to enable sensing along with these functions.

LAE is fabricated from thin films at low temperatures. Low temperature has two important benefits: 1) diverse materials can be used, enabling the formation of a wide range of transducers for sensing [7]–[10], actuation [11], and energy-harvesting [12]–[14]; and 2) plastic substrates can be used, enabling form factors that are large and conformal. With regards to large form factor, a key distinction from CMOS, which has followed the Moore's-law trend of reducing *cost per function*, is that LAE has followed a trend of reducing *cost per area*; LAE manufacturing, today driven by flat-panel display applications, achieves

Manuscript received January 20, 2013; accepted December 17, 2013. Date of publication January 10, 2014; date of current version January 24, 2014. This paper was approved by Associate Editor Ken Shepard. This work was supported in part by National Science Foundation (NSF) grants ECCS-1202168 and CCF-1218206. The work of Y. Hu and J. Sanz Robinson was supported via a Qualcomm Innovation Fellowship. IC fabrication was provided by MOSIS.

The authors are with Princeton University, Princeton, NJ 08540 USA (e-mail: yingzheh@princeton.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2013.2295979

TABLE I
SUMMARY OF COMPLEMENTARY STRENGTHS AND WEAKNESSES, OFFERED BY LAE AND CMOS FOR VARIOUS SYSTEM FUNCTIONS

	CMOS ICs	Large-area electronics
Sensing	+ precision instrumentation	+ Diverse sensor materials; large, conformal substrates
Macro-range communication	+ High-performance wireline transceivers + Wireless RF for remote communication	+ Long on-sheet interconnects (1cm-10m) for low-loss communication
Self-powering	+ Efficient power management circuits	+ Large devices for harvesting substantial power
Computation	+ >1B high-performance (deep-sub-μm scaled) and low-voltage logic gates.	- [weakness] limited voltage/feature scaled and non-complimentary transistors

processing on sheets as large as 9 m^2 at an approximate cost of \$200/m^2.

In addition to transducers, a variety of thin-film-transistor (TFT) technologies is also available in LAE. These use semiconductors based on organics [15], hydrogenated amorphous silicon (a-Si:H) [16], metal oxides [17], etc. Unfortunately, in all cases, the transistors have orders-of-magnitude lower performance and energy efficiency than those in standard crystalline-silicon CMOS ICs. State-of-the-art LAE TFTs have mobilities of 1–2 cm^2/Vs [16] (compared to 200–1000 cm^2/Vs for CMOS) and f_t's of $\sim$ 1 MHz (compared to 200–400 GHz for CMOS). Further limitations to energy efficiency are imposed by limited scalability of the gate stack (aside from experimental processes for organic TFTs [18]) and limited control of the threshold voltage, which have both led to the need for high supply voltages ($>$ 6 V) [16]. Nonetheless, demonstrating the ability to create circuits, various blocks based on TFTs have been reported, including processors, ADCs, RFID tags, etc. [19]–[21].

In this work, we focus on creating energy-efficient systems to exploit the large-scale sensing capabilities of LAE by leveraging high-performance CMOS ICs within hybrid architectures. Table I compares the complementary strengths offered by LAE and CMOS for the sensing, computation, communication, and self-powering functionality required in a system. For sensing, LAE enables diverse and expansive arrays of transducers, while CMOS enables sensing control and precise instrumentation. For communication, LAE enables long interconnects for low-energy signalling over the macro-scale distances that sensors are distributed, while CMOS enables efficient wire-line transceivers as well as high-frequency circuits for eventual wire-less communication to remote network nodes. For ultimately self-powered systems, LAE enables the formation of physically-large energy-harvesting devices for acquiring substantial power, while CMOS enables extensive power-management functionality via low-loss switches and stages. For computation, CMOS dominates, enabling VLSI based on high-performance and energy-efficient logic gates; LAE, on the other hand, suffers limited transistor scalability (leading to high capacitances, high voltages, low on-to-off currents) and lacks standard complementary (NMOS and PMOS) devices, resulting in significantly inferior logic gates. Sensing and communication in particular require integrative architectures to exploit the complementary strengths of LAE and CMOS; the next section describes the devices, circuits, and architectures developed to achieve this.

III. CIRCUITS AND ARCHITECTURES FOR HYBRID SENSING SYSTEM

The LAE technology employed in this system is based on a-Si:H TFTs, fabricated on flexible polyimide. A-Si:H is currently the dominant technology, used commercially in flat-panel display applications; the various LAE technologies, however, have similar device characteristics, making the architectural concepts largely transferable. For design simulations, we extract SPICE Level 61 models [22] from our fabricated TFTs.

The key limitation to creating hybrid LAE-CMOS architectures is the interfacing required between the two technologies. In particular, this must be achieved in a manner that is both scalable and able to maximally leverage the characteristics offered by the two technologies. Fig. 1 shows the system architecture [23]. The issue of interfacing is handled through two approaches. First, non-contact links are employed for the digital and analog signals. Inductive and capacitive antennas are patterned on both the LAE sheet and on the flex-tape packaging of the ICs (i.e., similar to RFID tags [24]), and the entire system is assembled via sheet overlay and lamination. The non-contact interfaces give two benefits: 1) on the large-area substrate, they avoid the need for metallurgical bonds, which are not available via high-volume, low-cost processes [25]; 2) they enable voltage step-up/down options between the two technologies to optimize the operational conditions required in each case. In our lab, we achieved sheet lamination with typical adhesive thickness $<$ 100 μm, enabling efficient proximity coupling. Second, to substantially reduce the total number of interface signals, particularly for controlling readout from each element of the sensor arrays, the LAE sheet integrates TFT-based accessing circuits that require a minimum number of IC control signals. The following subsections describe the circuits and architectures for the various subsystems in detail.

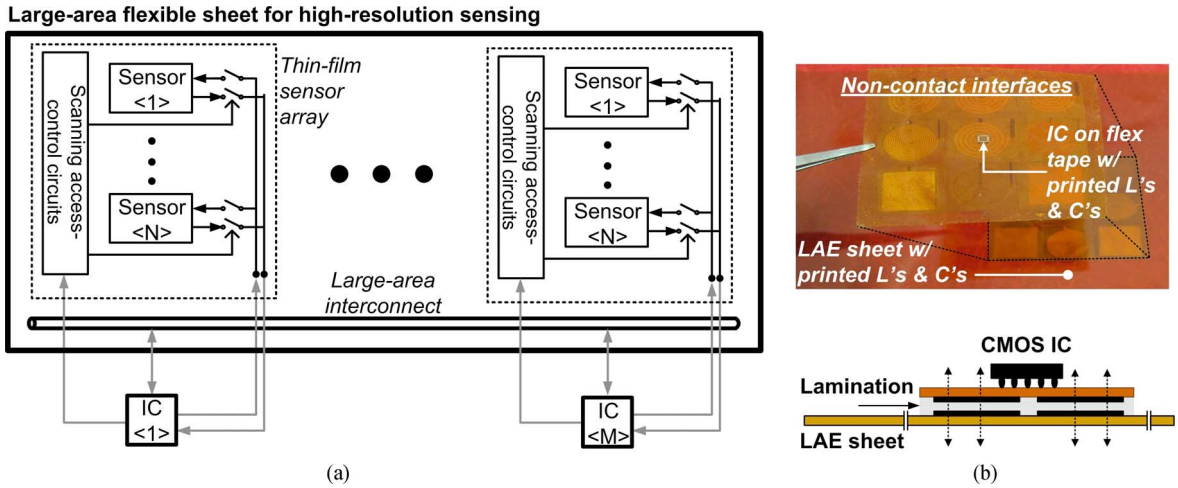


Fig. 1. (a) Scalable hybrid system concept with multiple ICs coupled to a large-area sheet; (b) non-contact interfaces for scalable system assembly, and side view of the lamination approach.

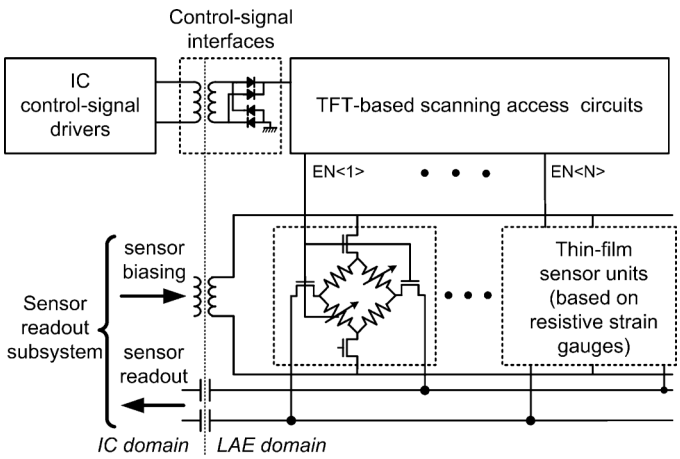


Fig. 2. Block diagram of sensor-array circuits for strain monitoring.

A. Thin-Film Sensor Array and Access Control

Fig. 2 shows a block diagram of the sensor-array circuits. These consist of individually-accessible thin-film sensor units, thin-film control-signal interfaces, TFT-based access-scanning circuits, and IC control-signal drivers.

1) Thin-Film Sensor Units: The sensor units consist of thin-film resistive strain gauges in a bridge configuration, as well as TFT access switches (Fig. 2). The bridge configuration is standard for strain monitoring applications, with reference strain gauges in each branch oriented orthogonally to enable measurement of the relative strain between two axes [26]. The individual strain gauges have a resistance that is altered under relative strain due geometric changes caused by mechanical deformation (i.e., strain $= \Delta L/L = (1/G)(\Delta R/R)$, where G is a parameter known as the gauge factor). The strain gauges are calibrated for aluminium beams and have a standard resistance of 1 kΩ (as in [26]). Large TFTs with W/L of 60,000 μm/6 μm are used for the access switches, to provide sufficiently-low on-resistance ($\sim$ 1.5 kΩ), comparable to the nominal strain-gauge resistance. The four TFTs impose a total loading of $\sim$ 700 pF on the access-scanning circuits; they thus limit the maximum speed of readout.

2) Thin-Film Control-Signal Interfaces: While the IC operates at 1.2 V, the TFT circuits need over 6 V for reasonable performance. Inductive non-contact interfaces can provide voltage step-up according to the turns ratio of the primary and secondary coils. Fig. 3(a) shows the schematic of the inductive interface, which includes a thin-film demodulator. This enables the control signal from the IC to be AC modulated for strong inductive coupling. To minimize the IC power for driving the interface, two factors are important: 1) high-Q resonant operation; and 2) low-voltage drop demodulation. The first factor exploits resonant operation of the secondary coil [27]. With strong coupling (i.e., coupling coefficient k $\sim$ 1), the impedance reflected to the driver is

$$Z_{\text{reflected}} = \frac{\omega^2 L_1 L_2}{j\omega L_2 + \frac{1}{j\omega C_{\text{diode}}} + R_{\text{s}}}. \tag{1}$$

This is higher at resonance. In particular, the quality factor of the secondary tank at resonance is $\text{Q}_2 = \omega L_2/R_{\text{s}}$, giving a reflected impedance of

$$Z_{\text{reflected}} = Q_2 \omega L_1. \tag{2}$$

This suggests that a high quality factor Q_2 is desired. With patterned inductors, this can be achieved by two approaches: 1) larger inductors can be patterned to increase the L_2/R_{s} ratio through thicker traces; and 2) a high operating frequency can be used (the operating frequency is limited by the capacitance of the demodulator, as described below). The patterned inductors adopted in our system use 18 μm thick copper, giving a typical quality factor of 15 at 1 MHz for a 3 cm diameter. The self resonant frequency is above 6 MHz. With 100 μm coupling distance, the coupling coefficient is 0.91; 0.5 cm lateral shift decreases the coupling coefficient to 0.85, exhibiting robustness against misalignment during lamination.

The second factor for reducing the IC power for driving the interface is minimizing the voltage step-up required. The power consumed by the secondary tank is given by

$$P_{\text{tank}} = I_{\text{L2}}^2 R_{\text{s}} = V_{\text{L2}}^2 \omega^2 C_{\text{diode}}^2 R_{\text{s}} = \frac{V_{\text{L2}}^2 C_{\text{diode}} R_{\text{s}}}{L_2} \tag{3}$$

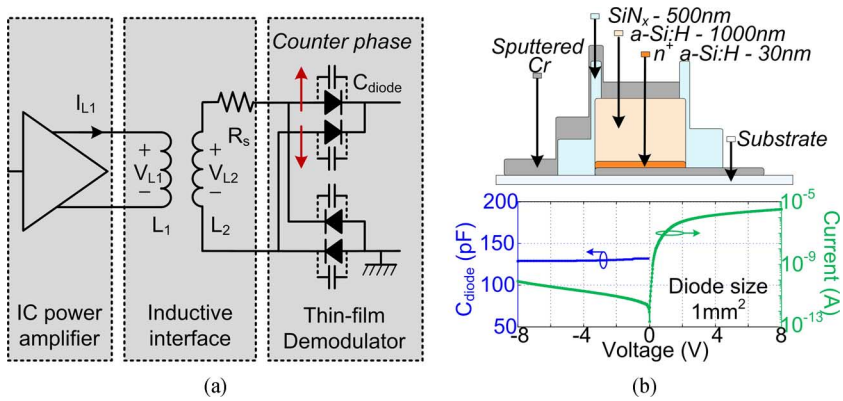


Fig. 3. (a) Inductive interface (offering voltage step-up of control signals) with thin-film full-wave rectifier structure; (b) associated a-Si:H Schottky TFD processing and measured I-V and C-V curves.

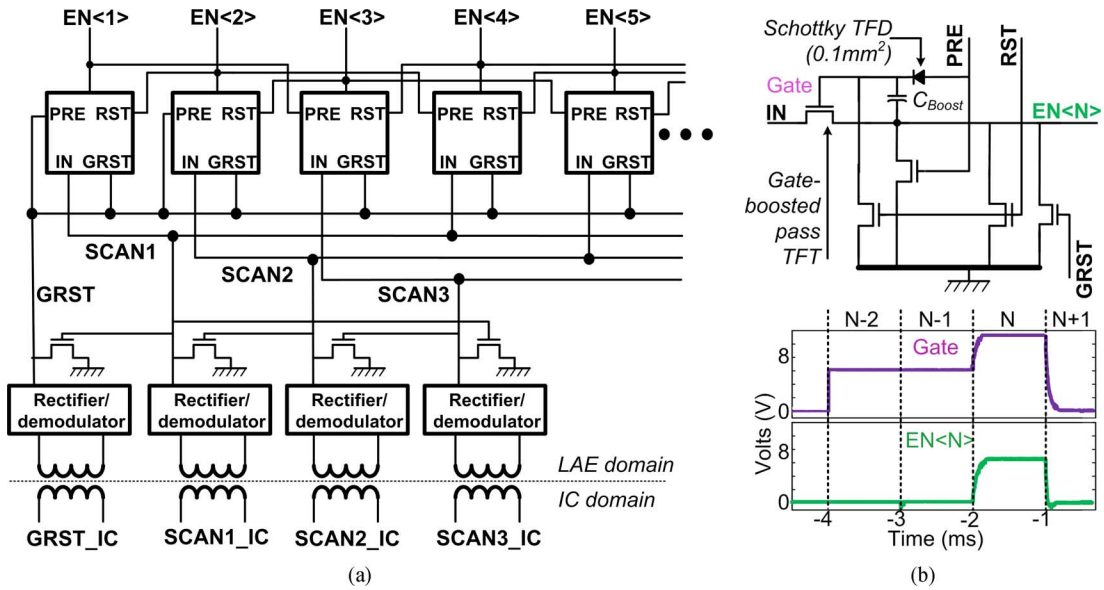


Fig. 4. (a) Thin-film LAE circuits for access control of multiple sensors; (b) schematic of a scanning element (top) and the simulated waveforms showing capacitive gate boosting for full-swing output logic levels (bottom).

implying quadratic power with respect to the voltage V_{L2}. Further, with larger voltage step-up, a higher number of turns is needed for L_2. This forces the use of thinner traces for a given diameter of the planar inductors, increasing the R_s/L_2 value. Therefore, the power consumption scales worse than quadratically with the voltage step-up. To minimize the voltage drop of the demodulators and thus reduce the voltage step-up required, we have developed thin-film a-Si:H Schottky-barrier diodes, processed at 180°C. Though thin-film diodes (TFDs) have been reported [28], the Schottky-barrier TFDs enable low voltage drop and give very good rectification characteristics (processing and measured I-V/C-V curves are shown in Fig. 3(b)). A key challenge, however, is their parasitic capacitance, which, due to AC conduction, would limit the demodulation of high input frequencies. To overcome this a full-wave rectifier topology is adopted, wherein the high-frequency signal appears at the demodulator inputs in counter phase (as shown in Fig. 3(a)). This cancels the capacitive transmission effect. The AC input frequency is now limited by the parasitic resonant capacitance introduced by the TFDs. For 87 μH inductors (3 cm diameter) and 1 mm^2 diodes (giving a capacitance of 130 pF each), the interface operates at 1.5 MHz; it has also been measured to provide good rectification well beyond 20 MHz.

3) TFT-Based Access-Scanning Circuits: Fig. 4(a) shows the scanning circuit, developed to generate sequential enable signals (EN⟨N⟩) to access the individual sensors. An important attribute is that this circuit requires just four control signals from the IC interface to enable multi-sensor accessing. GRST serves as a global reset and SCAN1–3, which are asserted in a round-robin manner, form three-phase control signals for stepping through the chain.

A key challenge with LAE TFTs is that they typically present only unipolar devices (i.e., both NMOS and PMOS transistors are not readily formed); for instance a-Si:H enables only NMOS devices. The use of three-phase control is thus critical for ensuring that full-swing logic levels (> 6 V) are preserved throughout the chain. Specifically, three-phase control enables a bootstrap capacitor to be applied to a pass transistor. Fig. 4(b) shows the circuit and simulated waveforms. The N$^{\text{th}}$ scanning element receives a precharge signal (PRE) from the

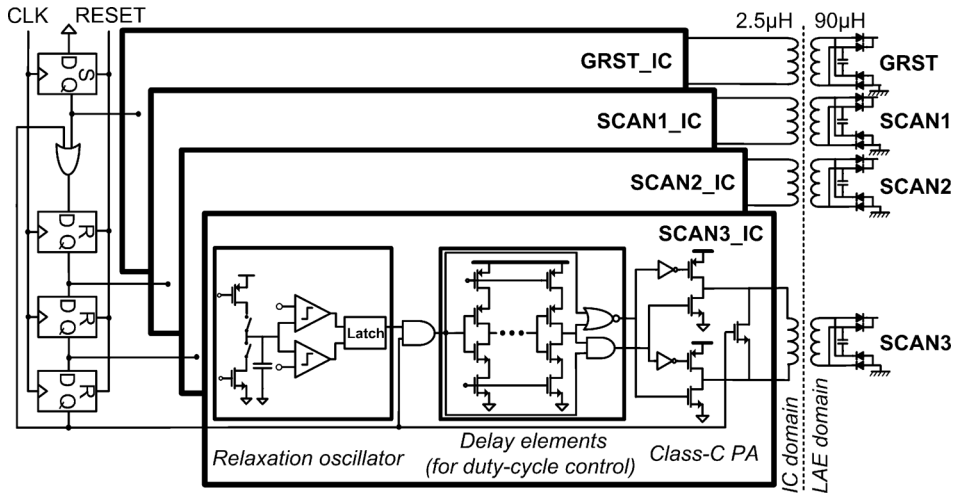


Fig. 5. IC control-signal drivers for scanning access control.

$\mathrm{N}-2$ element to precharge its bootstrap capacitor through a Schottky-barrier TFD. Then, two phases later, its input (IN) is asserted, generating output enable ($\mathrm{EN}\langle\mathrm{N}\rangle$) through the pass transistor. Finally, a reset signal (RST) is received from the $\mathrm{N}+1$ element, discharging both the output and bootstrap capacitor. All TFTs used in the scanning circuit have a $\mathrm{W/L}$ of 500 μm/10 μm.

4) IC Control-Signal Drivers: Fig. 5 shows the CMOS IC circuit that generates AC modulated control signals for the three-phase scanning circuits. The GRST and round-robin SCAN1–3_IC signals are generated by a shift-register loop. AC modulation is achieved via four relaxation oscillators. Separate oscillators enable tuning to the individual resonant frequency of each high-Q interface so that slight parasitic shifts can be overcome. Each output stage includes a Class-C power amplifier (PA) to drive the inductive interface. The use of a sub-50% current duty cycle in the PAs substantially improves the power efficiency for the achievable impedance values of the interface inductors (<100 μH at 3 cm diameter). In order to generate the reduced duty cycle, a delay element based on current-starved inverter stages is used.

To optimize the duty cycle (d) of the PAs, both conduction and switching losses must be considered. To minimize conduction loss, it is desirable that the PA devices be on only when their voltage is small, or conversely when the voltage across the primary inductor is large. The voltage across the primary inductor (shown in Fig. 6(a)) is given by

$$V_{\mathrm{L1}} = V_{DD}\cos\frac{2\pi}{T}t \tag{4}$$

while the instantaneous current (also shown in Fig. 6(a)), which can be derived from the effective switch resistance of the PA stage $\mathrm{R}_{sw,eff}$ and the voltage across this (i.e., $\mathrm{V}_{DD}-\mathrm{V}_{\mathrm{L1}}$), is given by

$$I_{\mathrm{L1}} = \frac{V_{DD}}{R_{sw,eff}}\left(1-\cos\frac{2\pi}{T}t\right)$$
$$\text{for } \frac{T}{2}(i-d) < t < \frac{T}{2}(i+d) \text{ where } i = 0,1,2\ldots. \tag{5}$$

Integrating the product of these gives the output power

$$P_{\mathrm{out}} = \frac{\int_0^T V_{\mathrm{L1}} I_{\mathrm{L1}}\,dt}{T} = \frac{{V_{DD}}^2}{R_{sw,eff}}\left(\frac{1}{\pi}\sin\pi d - \frac{1}{4\pi}\sin 2\pi d - \frac{1}{2}d\right). \tag{6}$$

With the power consumed by the PA given by

$$P_{\mathrm{consumed}} = \frac{\int_0^T V_{DD} I_{\mathrm{L1}}\,dt}{T} = \frac{{V_{DD}}^2}{R_{sw,eff}}\left(d - \frac{1}{\pi}\sin\pi d\right) \tag{7}$$

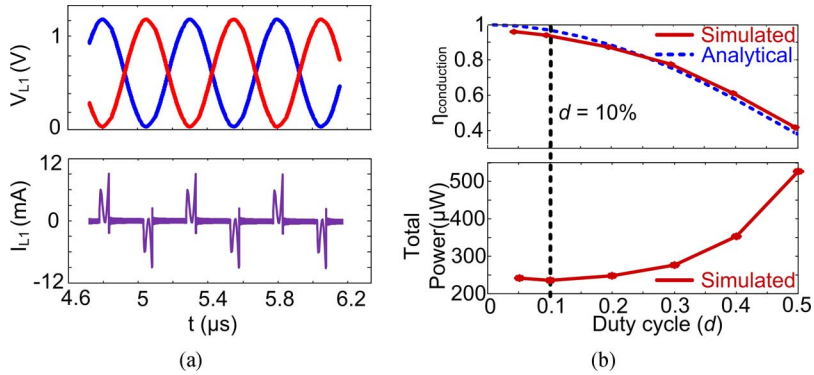
the efficiency of the duty-cycled PA due to conduction loss is thus given by

$$\eta_{\mathrm{conduction}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{consumed}}} = \frac{\frac{1}{\pi d}\sin\pi d - \frac{1}{4\pi d}\sin 2\pi d - \frac{1}{2}}{1-\frac{1}{\pi d}\sin\pi d}. \tag{8}$$

Decreasing the duty cycle (d) will cause $\eta_{\mathrm{conduction}}$ to approach to 1; the analytically-derived and simulated $\eta_{\mathrm{conduction}}$ is shown in Fig. 6(b). However, decreasing d requires increasing the width of the PA devices in order to maintain the average inductor current required for generating the output-voltage amplitude that is desired for the interface. This means that the device widths must be increased roughly at a rate $\propto 1/d$. This causes the resulting switching loss to increase, opposing the efficiency improvement from reduced conduction loss. As a result, the total power consumption can increase, as shown in Fig. 6(b). Based on these factors, an optimal duty cycle of 10% is chosen.

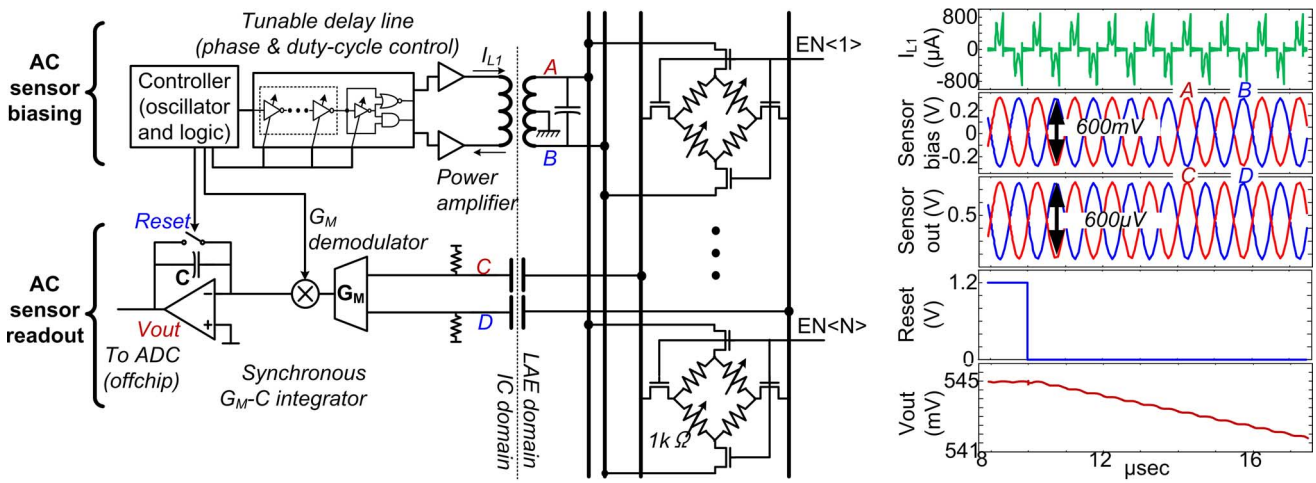
B. Sensor Readout

Fig. 7(a) shows the sensor-readout circuit. It consists of two synchronized signal paths: 1) AC sensor biasing; and 2) AC sensor readout. The sensor-biasing path consists of a pulsed PA that is optimally duty cycled (similar to Section III-A.4). In order to then properly position the pulses driving the PA so that the output sensor-biasing waveform is phase aligned with the readout path, a tunable delay line is used. The waveforms are shown in Fig. 7(b). Unlike the control-signal drivers, however, the secondary coil of the sensor-biasing path is center-tapped



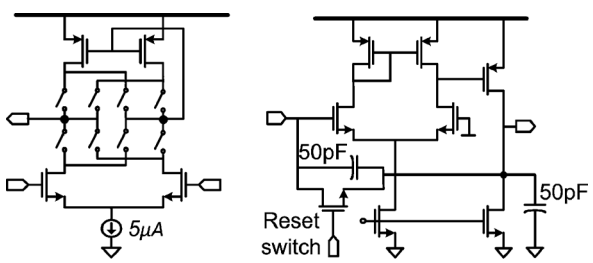
(a) (b)

Fig. 6. (a) Simulation waveforms of voltage and current across the primary inductor L_1; (b) $\eta_{\text{conduction}}$ and total power consumption (including both conduction and switching losses) versus duty cycle d.



(a) (b)

Fig. 7. (a) Multi-sensor readout circuits for thin-film resistive strain-gauge bridges; (b) simulation waveforms.



(a) (b)

Fig. 8. (a) Synchronous G_M stage with chopper demodulation; (b) integrator based on two stage op-amp.

and grounded. This mitigates the generation of large common-mode signals at the sensor-bridge outputs. The AC-modulated differential sensor output is then acquired via a capacitive interface, to impose minimal loading on the sensor bridge at the frequency used. The modulation frequency is chosen to be high enough to minimize loses in the inductive interface and low enough to avoid source-drain AC conduction due to the capacitance of disabled TFT access switches, which give a high-pass cutoff frequency of $\sim$ 1.5 MHz. The modulation frequency is therefore set to be 200 kHz.

Demodulation and readout of the sensor output is performed via a synchronous G_M-C integrator. For demodulation, the G_M stage uses switches at its output (as shown in Fig. 8(a)), which require that the sensor-biasing signal be phase aligned, as described above. Demodulation in this manner has two advantages for noise mitigation. First, $1/f$ noise is reduced by upconversion at the output to the modulation frequency. Second, AC error signals due to RC mismatch through the branches of the thin-film resistive-sensor bridge occur 90° out of phase (i.e., orthogonal to the modulation signal). This can be seen in the equation of the differential sensor output (which assumes the branches differentially exhibit ΔR perturbation):

$$\begin{aligned} V_{\text{sensor\_out}} &= V_{\text{out1}} - V_{\text{out2}} \\ &= \left(\frac{R//\frac{1}{j\omega C}}{R//\frac{1}{j\omega C} + (R+\Delta R)//\frac{1}{j\omega(C+\Delta C)}} \right. \\ &\quad \left. - \frac{(R+\Delta R)//\frac{1}{j\omega C}}{R//\frac{1}{j\omega C} + (R+\Delta R)//\frac{1}{j\omega C}} \right) V_{\text{sensor\_bias}} \\ &\approx \frac{\Delta R}{2R} V_{\text{sensor\_bias}} + \frac{j\omega R \Delta C}{4} V_{\text{sensor\_bias}}. \end{aligned} \tag{9}$$

Here ΔR is the resistive change of the sensor due to strain, and ΔC is the parasitic capacitive mismatch. The approximation is valid when $R \ll 1/j\omega C$, which is satisfied for the measured parasitic capacitor value ($\sim$ 1 pF) at the modulation frequency ($<$ 1 MHz). Since the second term, which is generated from the

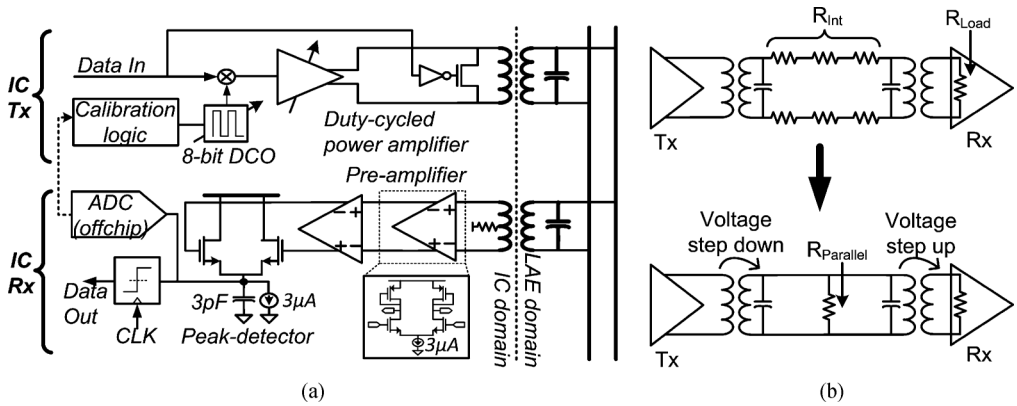


Fig. 9. (a) Transceiver circuits for communication among distributed ICs using large-area interconnects; (b) stepped signaling levels with inductive interfaces.

parasitic capacitive mismatch, is orthogonal to the first term, it is rejected after demodulation. For the biasing current used (5 μA), the remaining output noise current PSD of the G_M stage is 1.2 pA/$\sqrt{\text{Hz}}$.

Following demodulation, the signal is integrated using the two-stage op-amp circuit shown in Fig. 8(b). An integration capacitor of 50 pF is used in feedback, along with a reset switch, which defines the integration interval. Since the op-amp is not required to have high bandwidth, a compensation capacitor of 50 pF is included at the output node, making it the dominant pole to achieve stability with low power. The op-amp consumes less than 15 μW during integration. Finally, the integrated signal is then digitized by an off-chip ADC.

C. Transceiver for Macro-Range Communication

Fig. 9(a) shows the transceiver for communication over large-area interconnects for the distributed ICs; with multiple ICs on large-area buses, multiple access protocols, such as token ring, can be implemented to avoid data collision [29]. Previous efforts to exploit large-area interconnects have used pulsed signals and have been limited by the interconnect impedance [30]. For strong coupling over the non-contact links, we use AC signaling based on on-off-keying (OOK) modulation. The receiver chain thus includes preamplifiers and a differential-pair peak detector, to acquire the OOK envelope, followed by a regenerative comparator. Synchronization and multiple access between transceivers can thus be achieved by digital baseband processing.

By maximizing the interconnect impedance, signaling at the resonant frequency helps substantially, reducing the Tx power consumption and maximizing the Rx SNR. The challenge is that generally, the precise impedance of the interconnect network is unpredictable. To overcome this, a calibration loop is adopted. The local receiver, which is also coupled to the interconnect network, enables the Tx signal to be self-sensed. Consequently, the OOK modulation frequency can be optimally set to the resonant point via an on-chip digitally-controlled oscillator (DCO). This is achieved by digitizing the output from the peak detector (using the off-chip ADC), and applying a gradient-descent algorithm to arrive at the maximal signal amplitude.

In addition to resonant signaling, optimization of the Tx and Rx signal levels through the use of inductive coupling improves power and SNR. As shown in Fig. 9(b), Tx power is dominated by losses due to the resistance of the long interconnect, rather than resistive losses within the receiver. To minimize interconnect losses, which at resonance can be modelled as a parallel resistance, voltage step down is employed at the transmitter interface. On the other hand, to maximize the Rx SNR, voltage step up is employed at the receiver interface, since the resistive loss there is very small. The nominal signal amplitudes are 2 mV for the interconnect and 4 mV for the receiver.

TABLE II
SYSTEM PERFORMANCE SUMMARY.

Technology	IC: 130nm CMOS, LAE: a-Si (on 50μm polyimide)		
Readout Subsystem		**Communication Subsystem**	
Noise	17.9μStrain$_{RMS}$	Tx Energy/bit (@7.5m)	12.8pJ
Energy/measurement	270nJ	Rx Energy/bit (@7.5m)	3.3pJ
Max. Nonlinearity	20.7μStrain	Max. Data Rate	2Mb/s
Max. Measurement/sec.	500	DCO Tuning Range	9.5 – 25 MHz

IV. System Test Results

The silicon IC is fabricated in 130 nm CMOS from IBM (Fig. 10(a)), and the LAE components are fabricated in house on 50-μm-thick polyimide foil (Fig. 10(b)). The TFTs are based on a-Si:H, which we process in house at low-temperature (180°C) [16]; Fig. 11 shows a schematic TFT cross section and typical I-V curves measured. The LAE interconnect as well as interface inductors and capacitors are patterned with 10-μm-thick copper. An overall performance summary of the system is given in Table II.

A. Thin-Film Sensor-Array and Access-Control Tests

Fig. 12 shows measured waveforms of the thin-film access-control circuits. The 1.2 V, AC-modulated control signals from the prototype IC (SCAN1–3_IC) are stepped up to 6 V and rectified. Round-robin assertion of the stepped up SCAN1–3 signals generates the sequential enable signals (EN⟨N⟩). It can be seen that the output level is preserved thanks to the bootstrapping approach described in Section III-A.3.

The modulation frequency of the IC control signals is 1.5 MHz, and the total power consumption of the IC drivers is 1.3 mW. The measured efficiency of the PAs is 80% at the

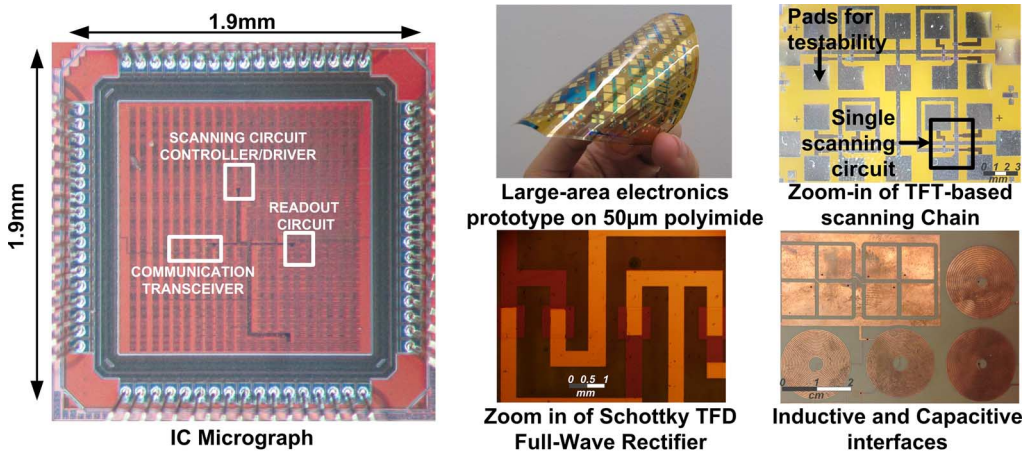


Fig. 10. (a) Micrograph of the 130 nm CMOS IC; (b) Large-area electronics components are fabricated on 50 μm-thick polyimide foil.

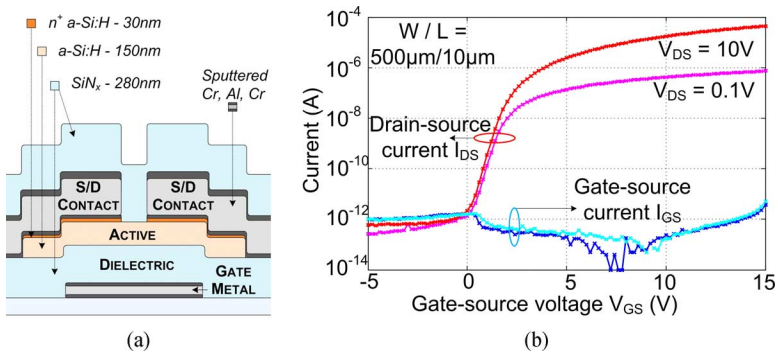


Fig. 11. (a) Amorphous silicon TFT cross section; (b) measured TFT I-V curves ($\mathrm{W/L} = 500\ \mu\mathrm{m}/10\ \mu\mathrm{m}$).

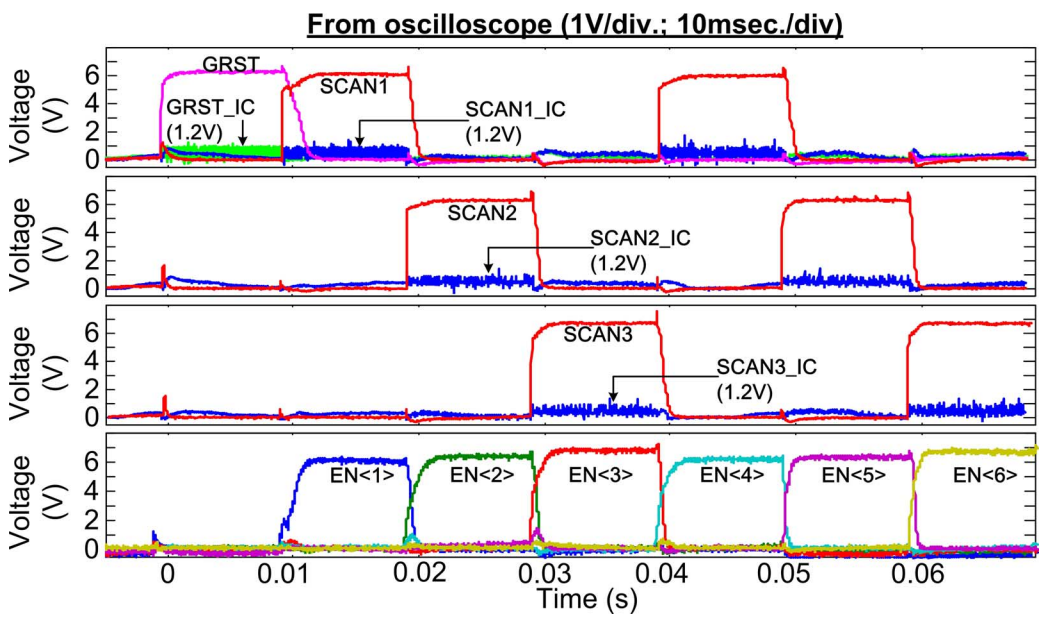
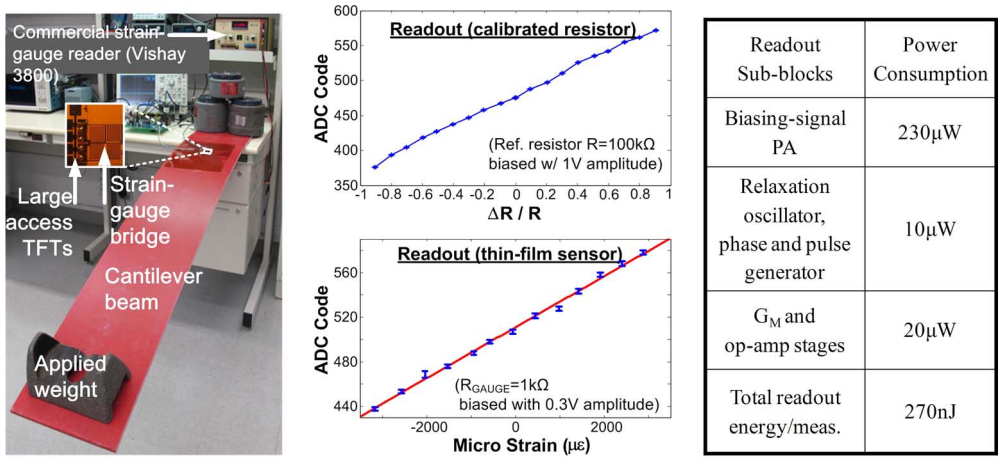


Fig. 12. Measured waveforms (oscilloscope capture), showing LAE access-circuit outputs from AC-modulated IC control signals.

chosen duty cycle of 10% (as described in Section III-A.4). The maximum frequency of the scanning circuit is 500 Hz, limited by the load capacitance ($\sim$ 700 pF) of the TFT sensor-access switches. This gives a total energy per measurement of 2.6 μJ for the access-scanning circuit.

B. Sensor Readout Tests

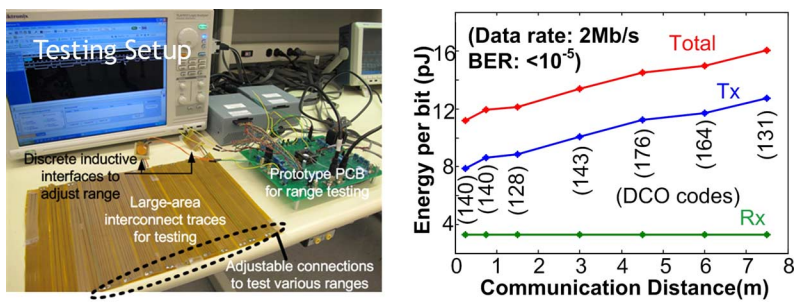
To characterize the readout subsystem, tests were performed using both a calibrated resistor and the LAE strain sensors. Fig. 13(a) shows the strain-measurement setup in the lab,



Readout Sub-blocks	Power Consumption
Biasing-signal PA	230μW
Relaxation oscillator, phase and pulse generator	10μW
G_M and op-amp stages	20μW
Total readout energy/meas.	270nJ

(a) (b) (c)

Fig. 13. Readout circuit (a) test setup on cantilever beam, (b) test result with calibrated resistor and thin-film strain sensors, (c) power breakdown of readout sub-blocks .



(a) (b)

Fig. 14. Transceiver (a) test setup, (b) measurements of energy per bit (with the selected DCO codes shown) for a communication distance up to 7.5 m.

where the LAE sensors were bonded to a 180 cm cantilever beam which was loaded with known weights. Reference strain sensors, read by a commercial system (Vishay 3800), were also bonded for comparison. Fig. 13(b) shows the measured readout curves from the prototype (for the calibrated resistor and thin-film strain sensors). The x-axis shows the strain (i.e., ratio of length deformation to nominal length), measured using reference sensors read out via the Vishay 3800. The maximum non-linearity is 20.7 μStrain and the readout noise is 17.9 $\mu\text{Strain}_{\text{RMS}}$.

The measured power for the sub-blocks is given in Fig. 13(c): 230 μW for the biasing-signal PA; 10 μW for the relaxation oscillator, phase-control delay line, and duty-cycle pulse generator; and 20 μW for the G_M and op-amp stages. The total integration time per measurement is 500 μs, and at the 500 Hz measurement frequency, the total readout energy is 270 nJ/measurement.

C. Transceiver Measurement

To characterize the communication subsystem, the special test setup shown in Fig. 14(a) is used. A sheet of LAE interconnects in a serpentine layout was fabricated with solderable connections on the edges. This enables configurations of various lengths to perform range testing. Tx and Rx ICs, controlled by a specially-constructed test board, were then interfaced via inductive interfaces. Fig. 14(b) shows the measured energy per bit, for both the transmitter and receiver, with respect to communication distance, all measured at a rate of 2 Mb/s. At a distance of 7.5 m, the transmitter consumes 12.8 pJ/bit while the receiver consumes 3.3 pJ/bit, with a BER $< 10^{-5}$.

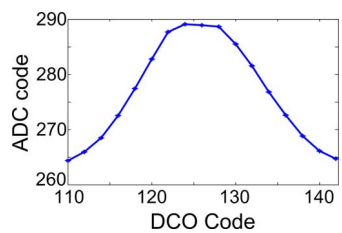


Fig. 15. An example of modulation-frequency self-calibration based on local receiver sensing to find the resonant point.

Annotations on Fig. 14(b) show the optimal DCO value that was chosen for each interconnect length. Fig. 15 shows the digitized output of the receiver peak detector during a typical DCO calibration sweep (i.e., with respect to the DCO code). For the measured interconnect lengths, the optimal DCO frequency ranges from 14.5 to 19 MHz.

V. Conclusions

This paper discusses the design and architecture for a hybrid sensing system that combines LAE and CMOS ICs. In order to leverage the complementary strengths offered by LAE and

CMOS, functionality for the sensing, instrumentation, communication and computation subsystems need to be carefully assigned between the two technologies. With LAE having the advantages of diverse sensing and macro-range communication (thanks to large-area interconnects), and CMOS ICs having the advantages of high-efficiency for instrumentation, computation, and signaling, a hybrid system combines the benefits of both technologies.

Scalability of the system is then a primary concern, limited by the interfacing required between the technologies. This is overcome via two main approaches. First non-contact interfaces between LAE and CMOS ICs are used to enable system assembly via sheet lamination (by patterning inductor and capacitor antennas on the LAE sheet and the flex-tape IC packages). Second, specialized LAE control circuits are designed to minimize the number of signals required from the ICs to control the large LAE sensor arrays.

The system achieves multi-channel strain readout with sensitivity of 18 $\mu\text{Strain}_{\text{RMS}}$ at an energy per measurement of 270 nJ for readout and 2.6 μJ/measurement for the sensor access-control circuits, while the communication energy is 12.8 pJ/3.3 pJ per bit (Tx/Rx) for a distance of 7.5 m.

REFERENCES

[1] A. Maeda, "Technology innovations for smart cities," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 6–9.

[2] B. Glisic, D. Inaudi, and N. Casanova, "SHM process as perceived through 350 projects," in *Proc. SPIE Smart Structures and Materials*, Mar. 2010, vol. 7648, pp. 1–14.

[3] J. P. Lynch and K. J. Loh, "A summary review of wireless sensors and sensor. Networks for structural health monitoring," in *The Shock and Vibration Dig.*, 2006, vol. 38, pp. 91–128.

[4] F. Casciati, M. Domaneschi, D. Inaudi, A. Figini, B. Glisic, and A. Gupta, "Long-gauge fibre-optic sensors: A new approach to dynamic system," in *Proc. 3rd Eur. Conf. Structural Control*, Jul. 2004, pp. 3–5.

[5] S. Doebling, C. Farrar, and M. Prime, "A summary review of vibration-based damage identification methods," in *The Shock and Vibration Dig.*, 1998, vol. 30, pp. 91–105, 2.

[6] T. Wipf, B. Phares, J. Doornink, L. Griemann, and D. Wood, *Evaluation of Steel Bridges (Volume I): Monitoring the Structural Condition of Fracture-Critical Bridges Using Fiber Optic Technology*, Center for Transportation Research and Education, Iowa State University, 2007.

[7] T. Someya, B. Pal, J. Huang, and H. E. Katz, "Organic semiconductor devices with enhanced field and environmental responses for novel applications," *Mater. Res. Soc. Bull.*, vol. 33, pp. 690–696, 2008.

[8] I. Graz, M. Kaltenbrunner, C. Keplinger, R. Schwïdiauer, S. Bauer, S. Lacour, and S. Wagner, "Flexible ferroelectric field-effect transistor for large-area sensor skins and microphones," *Appl. Phys. Lett.*, vol. 89, no. 073501, 2006.

[9] D. He, V. Nausieda, K. Ryu, A. Akinwande, V. Bulovic, and C. Sodini, "An integrated organic circuit array for flexible large-area temperature sensing," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 142–143.

[10] L. Zhou, S. Jung, E. Brandon, and T. Jackson, "Flexible substrate micro-crystalline silicon and gated amorphous silicon strain sensors," *IEEE Trans. Electron Devices*, vol. 53, no. 2, 2006.

[11] M. Takamiya, T. Sekitani, Y. Kato, H. Kawaguchi, T. Someya, and T. Sakurai, "An organic fet sram for braille sheet display with back gate to increase static noise margin," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006, pp. 1060–1061.

[12] M. Stordeur and I. Stark, "Low power thermoelectric generator-self-sufficient energy supply for micro systems," in *Proc. 16th Int. Conf. Thermoelectrics*, Aug. 1997, pp. 575–577.

[13] N. S. Shenck and J. A. Paradiso, "Energy scavenging with shoe-mounted piezoelectrics," *IEEE Micro*, vol. 21, no. 3, pp. 30–42, 2001.

[14] L. Huang, W. Rieutort-Louis, Y. Hu, J. Sanz-Robinson, S. Wagner, J. C. Sturm, and N. Verma, "Integrated all-silicon thin-film power electronics on flexible sheets for ubiquitous wireless charging stations based on solar-energy harvesting," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 198–199.

[15] K. Kim and C. Song, "Low voltage pentacene thin film transistors employing a self-grown metal-oxide as a gate dielectric," *Appl. Phys. Lett.*, vol. 88, no. 233508, 2006.

[16] B. Hekmatshoar, K. Cherenack, A. Kattamis, K. Long, S. Wagner, and J. C. Sturm, "Highly stable amorphous-silicon thin-film transistors on clear plastic," *Appl. Phys. Lett.*, vol. 93, no. 032103, 2008.

[17] T. Hirao, M. Furuta, T. Hiramatsu, T. Matsuda, C. Li, H. Furuta, H. Hokari, M. Yoshida, H. Ishii, and M. Kakegawa, "Bottom-gate zinc oxide thin-film transistors (ZnO TFTs) for AM-LCDs," *IEEE Trans. Electron Devices*, vol. 55, no. 11, 2008.

[18] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, pp. 745–748, 2007.

[19] K. Myny, E. Veenendaal, G. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 284–291, Jan. 2012.

[20] H. Marien, M. Steyaert, E. Veenendaal, and P. Heremans, "Analog building blocks for organic smart sensor systems in organic thin-film transistor technology on flexible plastic foil," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1712–1720, 2012.

[21] Y.-C. Tarn, P.-C. Ku, H.-H. Hsieh, and L.-H. Lu, "An amorphous-silicon operational amplifier and its application to a 4-bit digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1028–1035, 2010.

[22] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdalac, "SPICE models for amorphous silicon and polysilicon thin film transistors," *J. The Electrochem. Soc.*, vol. 144, no. 8, pp. 2833–2839, 1997.

[23] Y. Hu, W. Rieutort-Louis, J. Sanz-Robinson, K. Song, S. Wagner, J. C. Sturm, and N. Verma, "High-resolution sensing sheet for structural-health monitoring via scalable interfacing of flexible electronics with high-performance ics," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 120–121.

[24] H. Pristauz, "RFID chip assembly for 0.1 cents?," *OnBoard Technol.*, pp. 46–49, Sep. 2006.

[25] J. Fjelstad, *Flexible Circuit Technology*, 3rd ed. Delhi, India: BR Publishing, 2006.

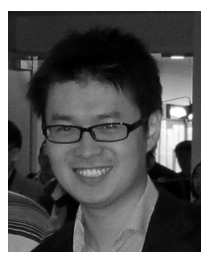
[26] *Full-Bridge for Bending or Axial Tension, Transducer Quality*, Omega [Online]. Available: http://www.omega.com/ppt/pptsc.asp?ref=SGT_Full-Bridge_Diaphragm&Nav=pree02a

[27] M. W. Baker and R. Sarpeshkar, "Feedback analysis and design of RF power links for low-power bionic systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 28–38, 2007.

[28] K. Myny, S. Winckel, S. Steude, P. Vicca, S. Jonge, M. J. Beenhakkers, C. W. Sele, N. A. J. M. van Aerle, G. H. Gelinck, J. Genoe, and P. Heremans, "An inductively-coupled 64 b organic RFID tag operating at 13.56 MHz with a data rate of 787 b/s," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 290–291.

[29] T. Sheldon, *Encyclopedia of Networking and Telecommunications*. New York, NY, USA: McGraw-Hill, 2001.

[30] L. Liu, M. Takamiya, T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, T. Kuroda, T. Someya, and T. Sakurai, "A 107 pJ/b 100 kb/s 0.18 μm capacitive-coupling transceiver for printable communication sheet," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 292–293.



Yingzhe Hu (S'11) received the B.S. degrees in both physics and microelectronics from Peking University, Beijing, China, in 2009, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2011, where he is currently working towards the Ph.D. degree.

His research interests include thin-film circuit and CMOS IC hybrid sensing system design and analog and mixed signal design for sensing applications.

Mr. Hu was a recipient of a 2013 Qualcomm Innovation Fellowship, the Gordon Wu award at Princeton University, and the SRP award of ISSCC 2013.

Warren S. A. Rieutort-Louis (S'11) received the B.A. (Hons.) and M.Eng. degrees in electrical and information engineering from Trinity College, Cambridge University, Cambridge, U.K., in 2009, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012. He is currently pursuing the Ph.D. degree at Princeton University, where his research interests include thin-film materials, processes, devices and circuits for large-area electronic systems, as well as the development of hybrid thin-film/CMOS systems.

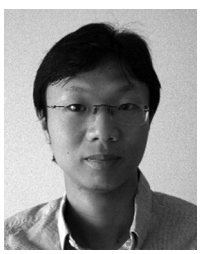
He is a Graduate Teaching Fellow in the Princeton McGraw Center for Teaching and Learning.

Mr. Rieutort-Louis is the recipient of an IBM Ph.D. Fellowship and the Andlinger Center Maeder Fellowship in Energy and the Environment.

Josue Sanz-Robinson received the B.Eng. degree in electrical engineering (Hons.) from McGill University, Montreal, Canada, in 2010 and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012. He is currently working towards the Ph.D. degree in electrical engineering at Princeton University.

His research focuses on amorphous/nanocrystalline silicon rectifying diodes and sensors for flexible large-area electronic systems.

Mr. Sanz-Robinson was a recipient of a 2013 Qualcomm Innovation Fellowship.



Liechao Huang (S'11) received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2010 and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012, where he is currently pursuing the Ph.D. degree.

His research interests include thin-film circuit design for power, radio and sensing interfaces, CMOS analog and mixed signal design for sensing interfaces and power management and hybrid system design combining thin-film circuits and CMOS ICs.

Mr. Huang was the recipient of a 2010–2011 Princeton Fellowship.

Branko Glišic received his degrees in civil engineering and theoretical mathematics at University of Belgrade, Serbia, and the Ph.D. at the EPFL, Switzerland.

After eight years' experience at SMARTEC SA, Switzerland, where he was involved in numerous SHM projects, he is now an Assistant Professor in the Department of Civil and Environmental Engineering of Princeton University, Princeton, NJ, USA. His main areas of interest are SHM methods, advanced sensors based on fiber-optics, large-area electronics and conductive polymers, SHM data management, and smart structures. He introduced SHM in classrooms as regular undergraduate and graduate courses at Princeton University.

Prof. Glišic was awarded 2013 SHM Person of the Year Award by the editors and associate editors of *Structural Health Monitoring: An International Journal* and along with his collaborators he won the First Place at the 7th Princeton Innovation Forum with his research on sensors based on large-area electronics. He is author or co-author of more than 100 published papers, short courses on SHM, and the book *Fibre Optic Methods for Structural Health Monitoring*. He is a member the Council of ISHMII, editor-in-chief of the ISHMII's newsletter *Monitor*, voting member of ACI committee on SHM, and member of several other professional associations, including IABMAS, ASCE, and more.

James C. Sturm (S'81–M'85–SM'95–F'01) received the B.S.E. degree in electrical engineering and engineering physics from Princeton University, Princeton, NJ, USA, and the M.S.E.E and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1981 and 1985, respectively.

He was with Intel Corporation as a Microprocessor Design Engineer as well as with Siemens, Munich, Germany. He has been with the Faculty of Princeton University since 1986, where he is currently a Professor of electrical engineering and PRISM Director. In 1994–1995, he was a von Humboldt Fellow at the Institüt für Halbleitertechnik, University of Stuttgart, Germany. He has worked in the fields of silicon-based heterojunctions, 3-D integration, silicon-on-insulator, optical interconnects, TFT's, and organic light-emitting diodes. His current research interests include silicon–germanium–carbon and related heterojunctions on silicon, SOI, and 3-D integration, large-area electronics, flat-panel displays, organic semiconductors, and the nanotechnology–biology interface.

Prof. Sturm is a member of the American Physical Society and the Materials Research Society. Formerly, he was a National Science Foundation Presidential Young Investigator. He was the recipient of ten awards for teaching excellence from both Princeton University and the Keck Foundation and was the recipient of the President's Distinguished Teaching Award at Princeton in 2004. In 1996 and 1997 he was the Technical Program Chair and General Chair of the IEEE Device Research Conference, for which he is now a charter trustee. He served on the organizing committee of IEDM (1988–1992 and 1997–1999), having chaired both the Solid-State Device and Detectors/Sensors/Displays committees. In 2005, he was named the William and Edna Macaleer Professor of Engineering and Applied Science. He also has been a symposium organizer for the Materials Research Society and on the SOS/SOI, EMC, and several other conference committees. He was the organizing Chair for ISTDM 2006.

Sigurd Wagner (SM'78–F'00) received the Ph.D. degree from the University of Vienna, Vienna, Austria, in 1968.

He was a Postdoctoral Fellow with Ohio State University, Columbus, OH, USA. From 1970 to 1978, he was with the Bell Telephone Laboratories working on semiconductor memories and heterojunction solar cells, and from 1978 to 1980, he was Chief of the Photovoltaic Research Branch of the Solar Energy Research Institute (now NREL) in Golden, CO, USA. Since 1980, has been Professor of electrical engineering, Princeton University, Princeton, NJ, developing materials, processes, and components for flexible large-area electronics, electrotextiles, and electronic skin. Currently, he is working on backplanes using amorphous and nanocrystalline silicon on plastic and steel foil substrates; elastomeric interconnects and circuit boards; flexible permeation barriers and gate dielectrics; and functional cells for flexible electronics.

Dr. Wagner is a Fellow of the American Physical Society. He was the recipient of the Nevill Mott Prize "for his groundbreaking research, both fundamental and applied, on amorphous semiconductors as well as chalcopyrites" in 2009.

Naveen Verma (S'03–M'09) received the B.A.Sc. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2009, respectively.

Since July 2009, he has been an Assistant Professor of electrical engineering at Princeton University, Princeton, MA, USA. His research focuses on advanced sensing systems, including low-voltage digital logic and SRAMs, low-noise analog instrumentation and data-conversion, large-area sensing arrays based on flexible electronics, and low-energy algorithms for embedded inference, especially for medical applications.

Prof. Verma was a recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, 2008 ISSCC Jack Kilby Paper Award, 2012 Princeton Innovation Forum 1st Prize, 2012 Alfred Rheinstein Princeton Junior Faculty Award, 2013 NSF CAREER Award, and 2013 Intel Early Career Award.