An ASIC for Readout of Post-Processed Thin-film MEMS Resonators by Employing Capacitive Interfacing and Active Parasitic Cancellation

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Abstract

Thin-film MEMS bridges as micro-resonators have proven attractive for various sensing applications (acceleration, mass, chemical, pressure, etc.) by using frequency shift as a basis for sensing [1]. Low-temperature processing of amorphous silicon (a-Si:H) enables low-cost fabrication of high-Q MEMS bridges having excellent compatibility with CMOS post processing. However, the a-Si:H bridges have weak motional conductances [2]. Parasitic feed-through capacitances, both due to the device structure and routing, can easily drown out the resonant behavior. This paper proposes a non-contact MEMS interfacing and readout system in standard CMOS which enables robust integration while substantially rejecting the effects of parasitic feed-through capacitance.

Fig. 1 illustrates the system based on a CMOS IC and a thin-film a-Si:H MEMS bridge, fabricated at 175°C having the structure and equivalent electrical circuit shown. The system addresses two key aspects. First, by enabling fabrication and interfacing of the MEMS directly on top of the IC passivation layer, the IC serves as a standard readout platform for bridges. Simplified interfacing between the IC and MEMS is achieved through capacitive coupling across the chip-top passivation, by using the CMOS top-layer metal and a post-processed thin-film metal layer on top of the passivation; this enables robust integration and the potential for substantially reduced parasitics [3]. Second, the IC employs phase-synchronous admittance readout to overcome the effects of the parasitic feed-through capacitance C_P. For typical bridges [e.g., length (L): 80μm, width (W): 25μm, thickness (T): 2μm, gap (G): 0.2μm], the motional parameters (extracted from measurement) are R_M=610kΩ, L_M=5H, and C_M=0.61fF. Due to the large R_M, even small practical values of C_P (~1pF) can make the high-Q resonant admittance undetectable electronically. Phase-synchronous readout increases sensitivity to the resistive motional admittance at resonance while rejecting the parasitic capacitive admittance.

Fig. 2 shows the readout-circuit. The MEMS resonator is biased through a direct bond with 6V DC (not sensitive to parasitics). A triangle wave (VSW=2.2Vp-p) is generated via an on-chip function generator and applied to the MEMS. This results in two currents: (1) an intended current I_M through the motional R_ML_MCM; and (2) a parasitic current I_CP through the parallel feed-through capacitor. The two currents are combined and converted to a voltage through the small resistor R_READ (<100Ω), giving V_IN (=V_M+V_CP). A small value R_READ has negligible impact on the phases of V_M (I_M) and V_CP (I_CP) with respect to the applied voltage (V_SW). The readout circuit relies on these phases to reject the effect of C_P and emphasize the resonant behavior of R_ML_MCM. At resonance, the effects of L_M and C_M cancel, and V_M (set by R_M) is in phase with V_SW. On the other hand, V_CP (set by C_P) is 90 degrees out of phase. A chopper clock CHOP, which is in phase with V_SW, is generated and used to demodulate V_IN at the output of a transconductance amplifier. With V_M in phase, a corresponding DC component is generated and provided to the integrator, while, with V_CP out of phase, the corresponding DC component is nulled. In fact, this approach not only isolates the R_ML_MCM admittance, but further enhances its resonant peak. In particular, off resonance, the admittance reduces in magnitude, but also rapidly deviates.
out of phase by 90 degrees thanks to the high $Q$. This causes both $V_{M}$ and $V_{CP}$ to be nulled. By exploiting magnitude and phase, a large integrator peak can be achieved at resonance compared to off resonance. The resonant point is then detected by sweeping the function generator’s frequency.

Fig. 3 shows the circuit for the function generator. High frequency resolution and dynamic range is required. It is observed that (1) the MEMS resonator has a sharp peak due to high $Q$ ($\sim 500$), and (2) high sensing dynamic range implies large frequency shifts. A small form factor for the system precludes an LC oscillator. A digitally-controlled relaxation oscillator is thus employed. The phase-noise is minimized by using switchable current sources of large value, as well as a large charging/discharging capacitor for setting the $V_{SW}$ voltage. The oscillator’s central frequency can be adjusted via the chosen central frequency. Such a resolution is sufficient for digital control ($D_{9:0}$) is incorporated for sweeping the charging/discharging capacitor for setting the $V_{SW}$ voltage.

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Such a resolution is sufficient for robustly capturing the resonant peak for $Q$’s of $\sim 1000$.

Figure 3: Digitally-controlled oscillator and simulated phase noise.

Fig. 4 shows the transconductor and integrator circuits. The transconductor consists of a pre-amplifier and modulator. With a small $R_{READ}$ chosen for phase preservation, $V_{IN}$ has small amplitude ($\sim 10 \mu V$). The pre-amplifier thus provides a gain of $10V/V$ and the modulator provides a gain of $600 \mu V/V$. The integrator is based on a capacitive-feedback op-amp. Since the feed-through signal ($V_{CP}/I_{CP}$ in Fig. 2) exhibits positive and negative steps, the transconductor and integrator are designed for accurate step response, with $\sim 4 ns$ settling time, to ensure feed-through signal nulling. Digitization is performed via a 10-b ADC incorporated into the op-amp integrator. After integration of the transconductor current, a fixed current source discharges the op-amp capacitor, and a counter, triggered by a comparator, measures discharge time.

Figure 4: Transconductor and integrator (ADC) circuits.

Measurements Results

The read-out IC is implemented in an IBM 130nm CMOS technology, and a-Si MEMS resonators are fabricated in house at 175°C (die photographs shown in Fig.5). The measurement setup is designed to evaluate the readout system with multiple MEMS bridges of different parameters. For this, a MEMS sample on glass, with multiple bridges, is in a vacuum chamber (under 900mTorr pressure) and interfaced to the CMOS test PCB through cabling.

Reference: