Integrating and Interfacing Flexible Electronics in Hybrid Large-Area Systems

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***Abstract*— An approach to creating large-area systems is described that combines flexible thin-film electronic sensor surfaces with complementary metal–oxide–semi–conductor (CMOS) integrated circuits (ICs). Complete systems are built by lamination of multiple layers, consisting of thin-film subsystems and CMOS ICs on a passive flexible substrate. A flexible passive backplane provides in-plane interconnections. Via-type interconnections between stacked layers are made by inductive or capacitive coupling. Steps and testing techniques, from devices and circuits to fully integrated hybrid systems, are illustrated.**

***Index Terms*— Flexible electronics, integration, noncontact, systems, thin film, wireless.**

I. Introduction

LARGE-AREA electronic systems are on the way to becoming part of the natural human environment. When made flexible, they can function as electronic skin or electronic wallpaper. Growing interest in large-scale or wearable form factors for sensors has greatly increased demand for electronic systems that can span physically large areas conformably, scalably, and at low cost. Soft and flexible electronic technologies often based on thin-film semiconducting materials (amorphous silicon, organics, and metal oxides) are emerging as key candidates for realizing systems for such form factors. These semiconductors can be processed at low temperatures. This raises the ability to pattern arrays of sensors and associated active circuits over a span of meters on a wide variety of plastic, glass, metal, and even paper substrates.

Despite the inherent and long-standing attraction of flexible human-size electronics, no industrial commercially successful technology has evolved to date. In the authors' opinion, the cause of this delay is the absence of an integrated approach to the realization of a broadly applicable technology, with the high performance that today's electronic environment demands. The goal of our program is to advance practical architectures, circuits, and fabrication methods required for such a technology. In our opinion, a successful flexible electronic system technology must marry the advantages of large-area thin-film technology with the advantages of advanced complementary metal–oxide–semiconductor (CMOS) technology. This paper describes one aspect of our work toward realizing such systems: a widely usable technique for aligning and interconnecting subsystems for their physical integration. Subsystems are integrated via sheet-by-sheet lamination on a passive flexible backplane.

This interconnection technique seeks to resolve two challenges. One is the need for integrating one, or several, of a diversity of circuit and subsystem modules, for example, sensor arrays. This challenge is addressed first. The second challenge is developing a robust technique for the overlay alignment of devices and circuits on plastic substrates, which, however, are not dimensionally stable. The robustness against misalignment is discussed in Section V.

A particular advantage of large-area electronics is the ability to form diverse transducers with high spatial resolution and large expanse. In addition to sensors, thin-film semiconductors also offer the possibility of energy harvesters, and when combined with high-performance CMOS circuits, complete self-powered flexible systems can thus be built.

Inevitably, as we head toward full systems integrating a myriad of such capabilities, the number of components to be assembled scales considerably. Table I illustrates some of these components and highlights representative technologies used to fabricate them on flexible (or rigid) substrates. The number of components and the ability to integrate them are now becoming a key challenge to the practical viability of electronics on conformable substrates as the basis for a system technology for large-scale sensing.

A multitude of approaches to tackle this integration challenge have been proposed, some of which are highlighted in Fig. 1. The holy grail of flexible electronics has long been considered to be the ability to monolithically pattern all the components and functions required for a system onto a single (flexible) substrate as in Fig. 1(a). To that end, prototype systems have been built such as [11] and [12]. While this assembly method may seem attractive as it follows the successful example of monolithic integration of microelectronic circuits, ultimately the scaling up of this approach to large areas and diverse functionality is likely to prove unwieldy. Fully integrated assembly is primarily excluded by

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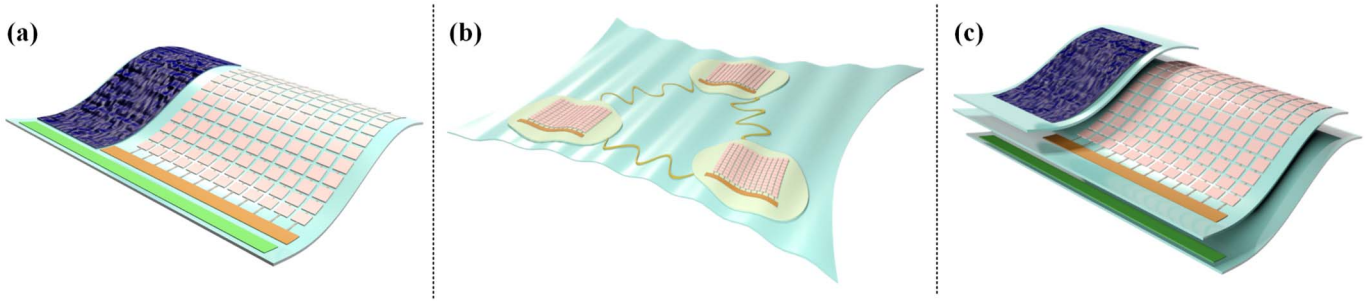

Fig. 1. Three different approaches to achieving integration of functionality to create flexible electronic systems. (a) Monolithic integration of all the components on a single sheet. (b) Components on localized multifunctional more rigid islands. (c) Separation of subsystems onto multiple functional planes.

TABLE I
COMPONENTS REQUIRED FOR LARGE-SCALE SENSING SYSTEMS

Component	Sample technologies
Sensors	Visible light (a-Si [1]…), X-Ray [2], Temperature [3], Pressure (PZT [4]), Acoustic, Moisture, Chemical [5]
Energy Harvesting	Solar (a-Si, organic…), Piezoelectric [6], Thermal [7]…
Energy Storage	Thin-film batteries [8]
Display	Active matrices of amorphous or microcrystalline silicon/Organic/Metal oxide thin-film transistors Liquid-crystal/Organic light-emitting diode/Electronic ink displays
Communication	RF transceiver, Thin-film radio [9]
Instrumentation and Computation	*Thin-film* Analog-digital converters [10], Amplifiers, Oscillators, Rectifiers *Non-thin-film* CMOS integrated circuits
Passives	Interconnects, Capacitors, Inductors

the range of functions that a large-area electronic system will meet: from sensing over large surfaces with slow thin-film devices and circuits to the fast control, computation, and communication that only CMOS circuits can provide. Also, large-area systems are heading toward integrating multiple sensing functions. Examples are included in Table I. These will require the ability of manufacturing and interconnecting of stacked layer structures that may combine different material systems. Monolithic integration will result in limited diversity and low yield, implying limited application scope and high cost.

An alternate approach shown in Fig. 1(b) relies on the creation of localized modular functional islands, on top of a large flexible or stretchable substrate. This approach has most commonly been taken in the *stretchable* electronic domain as a means of protecting active devices and circuits from mechanical strain when substrates are highly deformed or stretched [13]–[17]. When only *bending* is desired, the mechanics become similar to that of flip-chips on flexible substrates [18]. However, covering a large area with flexible chips by pick and place is too costly on the area scale of large electronic surfaces. On the other hand, processing high-performance circuits over large areas is also too costly when high-temperature materials must be integrated on low-temperature substrates (e.g., microcrystalline silicon on plastic [19]) or processed over large surfaces (e.g., microcrystalline silicon on steel foil [20]). Moreover, coplanar integrated circuits (ICs) that are more rigid than the substrate become susceptible to the mechanical, and hence electrical, weakness of interconnects at their transitions between the rigid circuit island and the deformable or stretchable substrate [21]. While engineered substrates can mitigate the transition from hard to soft [22], such substrates are likely to substantially raise cost.

For building flexible systems, we propose a contrasting approach, which shall be explored in depth in this paper, in which components up to subsystems are separated into multiple functional layers rather than combined in a single plane. The approach is shown in Fig. 1(c). It eases the integration challenge by replacing monolithic in-plane integration with a form of 3-D integration. In this approach, different component modules of a flexible system are manufactured in different thin-film technologies, and CMOS ICs are interfaced using chip-on-flex or chip-on-board techniques. This approach enables the modularization of functions and system customizability for modular mass production. The key challenge now becomes how to make robust yet simple interfaces between the different layers of this skinlike architecture. Section II lays out the argument for designing interfaces that facilitate the inclusion of CMOS ICs. Section III discusses the techniques required for realizing such interfaces and illustrates the benefits of noncontact interfaces, while Section IV explores in detail the design of these noncontact interfaces. Section V explores practical system testing provisions used for intermediate testability during system construction. Section VI highlights the example prototype systems we have realized using this architecture and the procedures for performance testing at steps during hybrid system integration. Section VII explores the cost prospects for large-area electronic systems.

II. THIN-FILM/CMOS HYBRID SYSTEMS

Thin-film materials used in creating flexible electronics typically include amorphous-silicon (a-Si), organic, and metal–oxide–semiconductors, insulators, and conductors.

TABLE II
COMPLEMENTARY STRENGTHS OF THIN-FILM AND CMOS TECHNOLOGIES

Attribute	CMOS	Thin-Film
Sensors	*Only small, sparse sensing capability*	**Many diverse sensors patternable on large flexible substrates**
Energy Harvesting	**Efficient power management circuits**	**Physically large harvesters for substantial power**
Energy Storage		**Flexible, thin-film batteries (moderate capacity)**
Display	**Able to drive large displays**	**Ability to pattern large displays based on TFT technology**
Communication	**High performance wireless and wireline transceivers**	**Low-loss interconnects**
Instrumentation / Computation	**High performance, highly energy efficient CMOS transistors for computation and instrumentation**	*Low-performance transistors only*

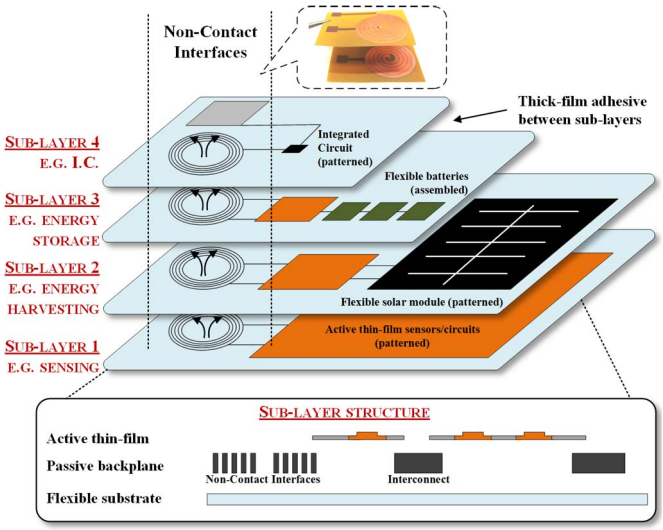

Fig. 2. Skinlike architecture making use of multiple sublayers. Sublayer 1 may be an array of TFTs that sense strain in the underlying substrate.

Decades of research into these materials have led to the ability to create a plethora of reliable and commercially viable energy harvesters, sensors, and active electronic devices such as transistors and diodes. In general, the electronic performance of these materials is very low when compared with the single-crystal silicon used in conventional CMOS ICs. The performance of CMOS makes it indispensable for performing highly sensitive readout from sensors, substantial computation and control over the data, or critical power-management functions on harvested energy. Table II highlights the contrasting strengths of the two technologies, emphasizing the need for the hybrid integration of scalable flexible thin-film electronics with CMOS.

III. SKINLIKE ARCHITECTURES

Fig. 2 shows the concept of our skinlike approach to assembling modular electronic systems, which consists of multiple sublayers, each accomplishing a subset of functions. At the present stage of development, each sublayer consists of a passive interconnect backplane, onto which components are either *directly patterned* (for flexible-compatible components, e.g., thin-film solar modules, thin-film active devices, etc.) or *assembled* (for nonpatternable components, e.g., discrete thin-film batteries, ICs, etc.).

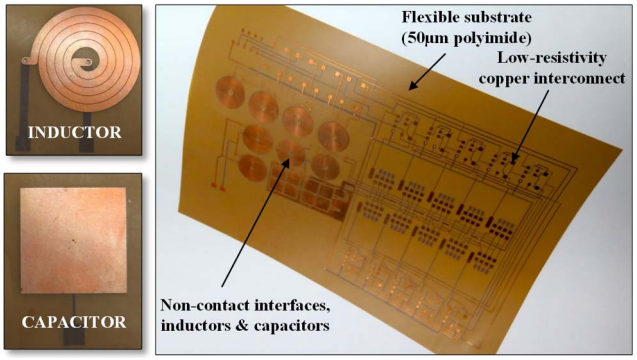

Fig. 3. Sample passive copper backplane onto which components can be patterned or assembled.

In order to create a complete system, multiple such sublayers are combined. The flexibility and bending characteristics of these sublayers, beyond conventional bending tests, need to be considered. This involves identifying optimal placing of components by their functionality. Strain sensors, for example, of the strain-sensing sheet should be placed in particularly strain-sensitive positions close to the top or bottom surface of the laminated package. Other components should be positioned in particularly strain-insensitive positions. For example, reference strain sensors, or temperature sensors that might also be sensitive to strain and thus susceptible to crosstalk, could be placed in a mechanically neutral plane.

A key to integration and modularity is the use of noncontact electrical interfaces between the system sublayers; these interfaces are capacitive or inductive. Such interfaces obviate the need for direct via-type metallic contacts over large areas and substantially facilitate sheet-to-sheet alignment. Along with such interfaces, a complementary focus for enabling scalable hybrid systems is the architectural design for keeping the number of physical interfaces to a minimum [23].

For the few components that may require ohmic interfaces, these can be achieved through anisotropic conductive film, or in the case of CMOS ICs, using chip-on-flex technology [18].

The overall system can then be assembled by applying adhesive to the sublayer sheets, aligning them, and laminating the whole stack to obtain a complete system.

A. Properties of the Passive Backplane

Fig. 3 shows an example of a flexible passive backplane and blowups of patterned coupling inductor and capacitor. Copper traces are made on 50-μm-thick polyimide substrates. The traces are used to create both in-plane interconnects as well as passives (capacitors and inductors), including those required for the noncontact interfaces between sublayers.

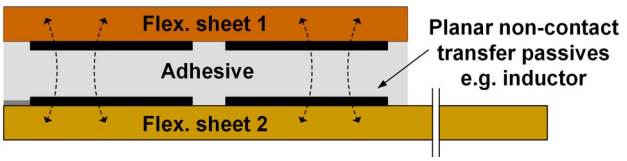

Fig. 4. Schematic cross section of noncontact interfaces. The ratio of passive's diameter to adhesive thickness is on the order of 500.

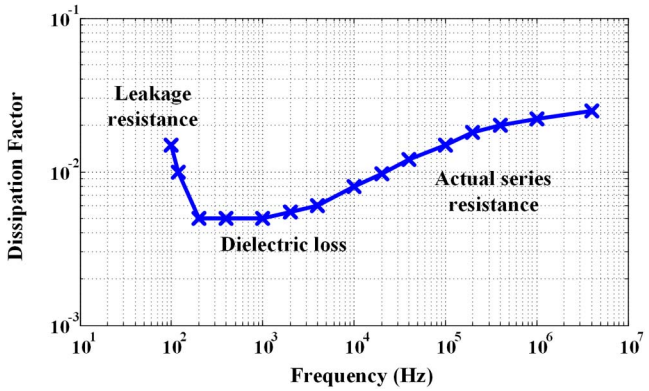

Fig. 5. Measured dissipation factor frequency response for a 3 cm × 3 cm copper capacitor with a ∼50-μm-thick adhesive as dielectric, exhibiting three regions of nonidealities.

Patterned of 30-μm-thick copper, the traces have a sheet resistance of 2 mΩ/square.

In the cases that require discretely packaged components such as commercial thin lithium–ion batteries [24], the 3M 9703 z-axis conductive adhesive used provides a contact resistance of less than 0.03 Ωcm^2.

IV. Noncontact Interfacing Between Sublayers

The use of noncontact interfaces for the transfer of both power and signals between sublayers substantially simplifies system assembly. However, typically both power and signals will require appropriate modulation for transmission over noncontact interfaces (e.g., power harvested might be dc, and signals generated might be baseband). As we describe below, both for the interfaces themselves and the modulation circuits, passives, such as copper inductor and capacitor plates (shown in Fig. 3), play a key role. Fig. 4 shows the typical cross section of a noncontact interfaces across two sublayers, separated by an adhesive, typically 50-μm thick.

A. Design of Capacitive Interfaces

A typical 3 cm × 3 cm capacitive interface constructed as in Fig. 4 achieves a measured capacitance of 180 pF (hence ∼20 pF/cm^2), with a measured dissipation factor due to nonidealities in the adhesive dielectric of 0.005–0.02 in typical signal frequencies of interest. This dissipation factor has a frequency dependence that is typical of nonideal capacitor behavior as shown in Fig. 5, showing three regions likely attributable to leakage resistance, dielectric dissipation, and actual series resistance [25]. In practice, the effect of this loss mechanism is low, and the capacitors behave nearly ideally.

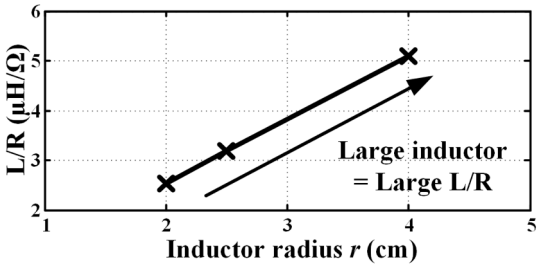

Fig. 6. Measured points and line fit demonstrate scaling of L/R ratio as a function of inductor radius. Large radii are obtainable on large flexible sheets.

B. Design of Inductive Interfaces

Many considerations go into the design of inductors for the sublayer interfaces. Three key parameters can be optimized: 1) inductance (L); 2) parasitic resistance (R); and 3) self-capacitance (C). A unique benefit that can be leveraged to optimize these is that that the planar spiral inductors can occupy substantial surface given the overall size of flexible skins.

The inductance L scales in proportion to the radius of the inductor r and the square of the number of turns N

$$L \propto N^2 r.$$

The resistance R also scales as a function of the square of the number of turns, given that the overall trace length scales with Nr and the trace width with r/N

$$R \propto \rho N^2/t$$

where ρ is the trace resistivity (70 nΩm in our inductors) and t is the trace thickness. This results in the ratio L/R, to first order, simply being proportional to the radius of the inductor, for a given passive technology (the importance of this ratio is shown in Section V). This relation is shown in Fig. 6 for measured flexible copper inductors.

For a given area, a maximum achievable inductance can be conservatively estimated assuming a turn width that is equal to four times the copper thickness on the passive backplane and a turn spacing pitch that is equal to twice the amount of the thickness of the copper. For a 3-cm inductor diameter, this results in an inductance of approximately 50 μH, and a series resistance of ∼25 Ω.

Unlike for the planar capacitors, the resistive loss mechanism associated with the inductive interface is substantial and causes a strong frequency dependence in the power transfer efficiency. This is shown in Fig. 7, for an ac signal across sample copper inductors (∼15 cm^2), taking into account parasitic losses in the inductor [26].

C. Sensitivity to Passive Misalignment/Proximity Variations

An important advantage of interfacing with large-area inductors and capacitors is their low sensitivity to overlay in-plane misalignment. This addresses the second challenge mentioned in Section I and aids in maintaining coupling under even substantial bending. Taking the coupling to proportionally decrease the relative loss of area overlap provides estimates of

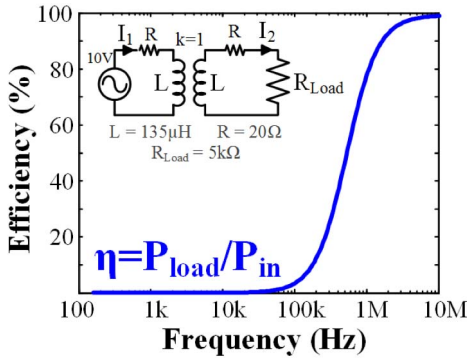

Fig. 7. Power transfer efficiency η for inductive interfaces [26].

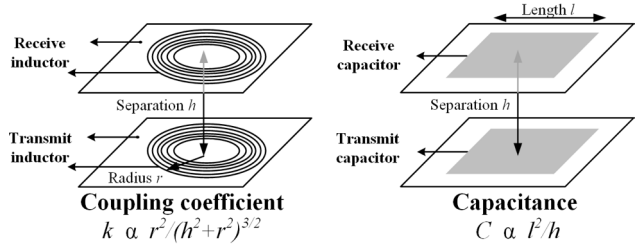

Fig. 8. Inductive coupling results in stronger robustness to proximity variations than capacitive coupling.

the loss of inductance and capacitance. When the centers of two circular planar inductors with radius r are misaligned by a distance d, their overlap area A changes from its perfectly aligned value of A_0 as $A/A_0 \cong 1-2d/\pi r$. When the centers of square capacitor plates with sides of length l are misaligned by a distance d, their overlap area changes as $A/A_0 = 1-d/l$ for lateral and as $A/A_0 \cong 1-2d/l$ for diagonal displacement. In other words, inductors and capacitors of centimeter size can tolerate misalignment of the order of a millimeter. This low sensitivity to misalignment greatly facilitates system assembly via lamination of subsystems on plastic sheets.

A key benefit of using inductive interfaces, in the near field, is that they are more robust against proximity variations than capacitive interfaces. The mathematical dependence of the ideal coupling coefficients as a function of distance [27] is shown in Fig. 8.

The inductive coupling coefficient is proportional to $r^2/(h^2+r^2)^{3/2}$. In our present configuration, $r \cong 250 \times h$. Therefore, the inductive coupling coefficient is approximately proportional to $1/r$ and is essentially independent of h. On the other hand, because the capacitance does vary with $1/h$, it depends strongly on variations of proximity. The impact of this height dependence for inductors is demonstrated in Section V.

V. Demonstrations of Thin-Film Systems With Noncontact Interfaces

The choice of suitable passives for specific interfaces is critical and principally dictated by the ac performance of thin-film active devices, mainly thin-film transistors (TFTs) and thin-film diodes (TFDs). Nominally, the operating frequencies are limited by the intrinsic cutoff frequencies (f_t) of the transistors. f_t drops with increasing parasitic device capacitance, which can be large. f_t values for three predominant thin-film technologies are shown in Table III.

TABLE III
Typical Transistor Cutoff Frequencies

Semiconducting Material	Typ. Cutoff Frequencies (f_t)
Amorphous silicon TFT	~ 1-2 MHz
Organic (e.g. DNTT) TFT	~ 1-2 MHz
Metal oxides (e.g. ZnO) TFT	~ 5-10 MHz
Crystalline silicon CMOS (130nm)	> 150 GHz

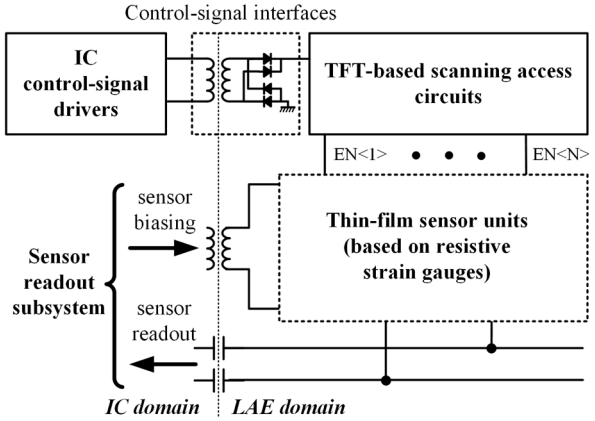

Fig. 9. Strain-sensing system incorporating inductive signal transfer from a CMOS chip to a large-area flexible sheet. High-frequency signals are rectified by high-frequency TFDs. In this system, sensor readout is performed over a single capacitive interface [28].

Comparing the values in Table III with Fig. 7, it is clear that the comparatively low cutoff frequencies of the TFTs could make inductive power transfer unviable. Nevertheless, it may prove desirable to leverage the ability of inductors to decouple the load voltage from the transmitter voltage, which enables voltage/current step-up/step-down across interfaces. This can help address differences in circuit voltage levels and/or enhance power transmission in the face of current limitation in the thin-film devices [26].

To illustrate the appropriate passives to use in hybrid system interfaces, we now present a number of developed systems for the purpose of *signal* or *power* transfer.

A. Signaling Interfaces

We have recently demonstrated both capacitor and inductor-based noncontact interfaces for signal transfer between a CMOS IC and a large-area flexible sheet.

Fig. 9 shows the blocks of a strain-sensing system that makes use of inductive interfaces for transfer of control signals (ac-modulated digital signals) from a CMOS IC to a large-area sheet [28]. Such an interface is useful here since a larger number of turns on the secondary coil allow voltage stepup of the low-voltage IC signal to voltage levels more suitable for thin-film circuits (>5 V). As described earlier, the inductive interface requires the use of high-frequency drive signals. In order for those to be rectified and used by the low-frequency TFT-based scanning access circuits, we develop amorphous-silicon thin-film Schottky diodes.

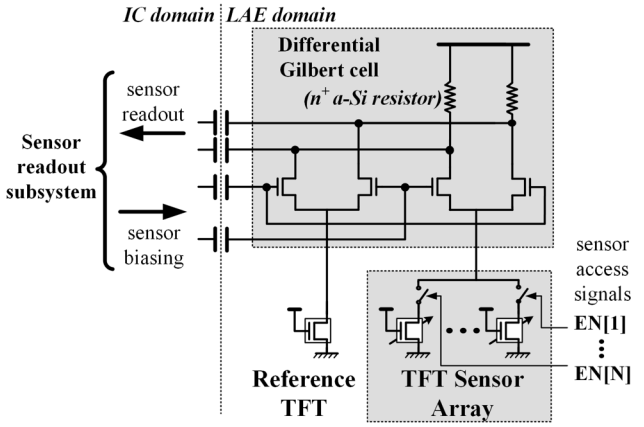

Fig. 10. Strain-sensing system incorporating capacitive biasing and readout from a thin-film sensor array. Capacitive interfaces are used as a result of the low-frequency operation requirements of the TFTs [29].

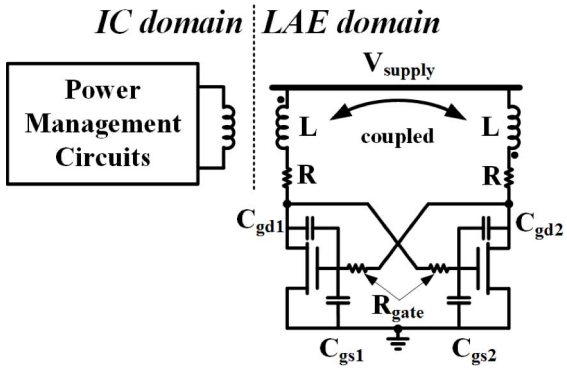

Fig. 11. Large-Area Electronics to CMOS power transfer system over an inductive interface, making use of an LC oscillator. TFT parasitics are resonated out by the inductors allowing high-frequency operation [31].

To minimize power consumption on the IC, the inductive interface is operated at resonance (a few megahertz), with high frequencies being more desirable in order to minimize inductive losses. The large intrinsic capacitance of the diodes, however, determines the resonant frequency of the inductive interface. To reduce the effect of this, we also develop nanocrystalline silicon diodes that exhibit $\sim 5\times$ lower capacitance for a given current, enabling a higher interface operating frequency and reducing power consumption of the IC control signal drivers by an order of magnitude [28], [29].

A second demonstrated strain-sensing system makes use of the strain response of TFTs. Capacitor-based interfaces are used for sensor biasing and sensor readout as shown in Fig. 10 [29]. In this sensing system, the dc current output from a strain-sensing TFT is modulated by an ac signal from a CMOS IC, and subsequently passed back over another capacitive interface to the IC for processing. The modulation frequency used in this circuit is limited, as described, by the cutoff frequency of the TFTs and is thus operated at approximately 100 kHz.

B. Power-Transfer Interfaces

We have demonstrated systems that make use of both capacitors [30] and inductors [31] for noncontact power transfer. For the latter, in response to the challenge of using inductors with thin-film devices, we recently demonstrated a thin-film circuit topology (an LC oscillator shown in Fig. 11) that uses inductors to resonate out capacitive TFT device parasitics, and hence enables the operation of TFT circuits at frequencies that make inductive transfer efficient [31]. This approach has proven particularly useful for transfer of *power* between sublayers.

In the design of the resonant oscillator circuit, the previous section emphasized a key metric to optimize, namely, the ratio of inductance to parasitic resistance (L/R). For example, in the LC oscillator, we demonstrated that in order for oscillations to be sustained, a critical circuit condition must be met [31]

$$\frac{g_m}{C_{\text{Par}}} \times \frac{L}{R} > 1 \tag{1}$$

where C_{Par} is a quantity related to the parasitic TFT capacitances and g_m is the TFT transconductance. As shown earlier, the area of the inductor is the determining factor in increasing the L/R ratio. Making inductors as large as physically possible thus turns out to be critical to overcoming the performance limits set by the typically low electrical performance of thin-film active devices, notably the low charge carrier mobility (embodied in the low TFT transconductance).

A manufacturing challenge that remains to be addressed in the design of inductors is that the thickness of the backplane copper traces (30 μm) is very large compared with the thickness of the active thin films ($\sim$1 μm). This could lead to step coverage challenges. Reducing inductor trace thickness increases resistance, and thus requires increasing inductance by the same factor in order to maintain system performance [see (1)] [31]. An alternative is to employ higher frequencies, but this is practically limited by the active thin-film devices. Thus, this becomes a strong motivator for moving to higher mobility thin-film material systems such as metal oxides, which can support signals of higher frequencies. Raising the charge carrier mobility μ will effectively reduce the value of L that is needed for oscillation [see (1)] and for efficient inductive power transfer. Adopting oxide semiconductors, for instance, could enable a reduction by a factor of 10 in backplane conductor thickness. In addition to step coverage concerns, patterning components using 30-μm-thick passive copper is likely to impact the mechanical properties of the entire large-area system [18]. A reduction of copper thickness, enabled by higher TFT carrier mobility, would thus make the entire system more mechanically flexible. The mobility-versus-inductance tradeoff equally applies to other forms of in-plane interconnect metallization such as polymer thick film.

We also investigate the effect of separation between inductors. For large separation distance h between inductors, Fig. 12(a) shows the relatively slow initial decline in coupling predicted by the theoretical coupling coefficient, in this specific case between two 2-cm-radius inductors. Fig. 12(b) shows this trend as measured for the LC oscillator power management system described in [31]. The normalized power transfer efficiency between the transmitting coil and the receiving coil is seen to decrease in a manner similar to the

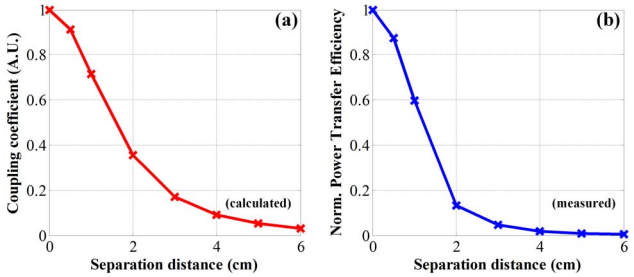

Fig. 12. (a) Computed coupling coefficient and (b) measured normalized power transfer efficiency versus distance for an inductive power transfer system with $R = 2$ cm, as described in [31].

computed coupling coefficient. Overall, this low dependence on small separation variations greatly simplifies the assembly of multiple sublayers, as it obviates the need for precise control of adhesive thicknesses between the layers.

VI. Practical System Testing

Having described the typical interfacing mechanism we use in our system designs, we illustrate some practical implementations for intermediate steps in the building of complete systems. Many steps are combined with subsequent experimentation on devices and circuits. For example, we interconnect devices on a TFT array to various circuits, evaluate these, and use the results for verifying device and circuit models.

Devices and circuits are first fabricated on rigid glass substrates. These are robust in testing and experimentation, and importantly serve as fiduciary products when we need to distinguish between inherent device/circuit performance characteristics and changes caused by fabrication on flexible substrates. Fig. 13(a) illustrates both substrates. In most cases, we observe identical electrical performance whether processing the circuits on glass or on 50-μm free-standing polyimide (Kapton E) substrates, even though substantial mechanical deformation occurs during processing (expansion/contraction of substrate during depositions, flattening of deformed sample for lithography/etching, mechanical flexing during assembly, etc.).

In our case, the maximum size of monolithic active thin-film circuits is determined by the substrate size that can be processed in the plasma-enhanced deposition system for amorphous-silicon TFTs; it is 7.5×7.5 cm^2. All the circuits, on both glass and flexible substrates, are provided with many 2×2 mm contact pads for external testing. We use a number of contact metal combinations for probing or for soldering pads. In amorphous-silicon TFTs, the top metal for interconnect and pads is typically chrome, onto which additional layers of chrome and gold or chrome and platinum (usually 30 and 250 nm, respectively) may be sputtered or evaporated. Both of these combinations allow for excellent electrical and mechanical connections using conventional lead solder, even at temperatures below 250 °C.

Circuits with fewer than 10 connections usually can be tested in individual blocks, by directly connecting supplies and pattern generators. To test circuits and sensor arrays of medium complexity, it is often easiest to break out all the connections to an external printed circuit board (PCB), using soldering as shown in Fig. 13(b), followed by control and readout using data acquisition cards. Fig. 13(c) shows how wire bonding can also be used to break out, from both glass samples and from ICs, onto a PCB; the IC is supported on an oxidized silicon wafer carrier, to fan out the tight pitches of the IC to a more appropriate PCB spacing.

Fig. 13(d) highlights the next level of integration experiments. We have developed a pin array that enables testing of all the devices and circuits of a sample. This array consists of 400 spring loaded pins [32], soldered through hole on a PCB. These are distributed over a 7.5 cm $\times$ 7.5 cm area in a predetermined pattern, matching probing pads patterned on the substrate with thin-film circuits, and routed to external headers. The pins are manually compressed onto the substrate through the use of the four pictured screws/nuts. When interfaced with external data acquisition boards, the pin array subsequently allows us to test and interconnect a large number of working circuits and devices through software control, and to then integrate several functions. With this setup, we have demonstrated circuits with simultaneous operation of over 250 TFTs on glass.

Fig. 13(e) shows the integration with a passive backplane, which closely demonstrates the approach described in Section II. Working circuits on plastic are identified and laminated onto a passive copper backplane, which is patterned with conductors and inductors/capacitors, to form a working strain-sensing system. Connection to the active circuits is typically achieved using the aforementioned unidirectional conductive adhesive tape. Using this method, we have demonstrated a number of systems. The first is a large-area strain-sensing system described earlier [29], which integrates a-Si TFT-based strain sensors, TFT scan chains, and access control circuits. During testing, strains of at least 0.1% are applied to the sensors and circuits without device failure; this is without making special provisions for putting the nonsensing elements in the neutral bending plane. In addition, energy-harvesting circuits supply power wirelessly from solar modules using inductor-based oscillators. As described, modulators/demodulators provide ac rectification of input signals and off-sheet transfer of measurements from the strain sensors. We have also demonstrated a gesture-sensing system [33], which integrates amorphous-silicon oscillators and scan-chain circuits on sheet. The sensed signals are provided to readout CMOS ICs, with the interconnection being performed using noncontact patterned interfaces.

VII. Cost Prospects of Flexible Large-Area Systems

Our overall approach to hardware fabrication is to build modular subsystems that can be integrated to then form unit cells of complete systems. Making use of capacitive and inductive coupling, these cells can be replicated and interconnected by simple tiling, to cover surfaces of arbitrary size. A generic unit cell will be drawn on a standard menu of subsystems, materials, and fabrication processes that are combined to meet the needs of a specific application.

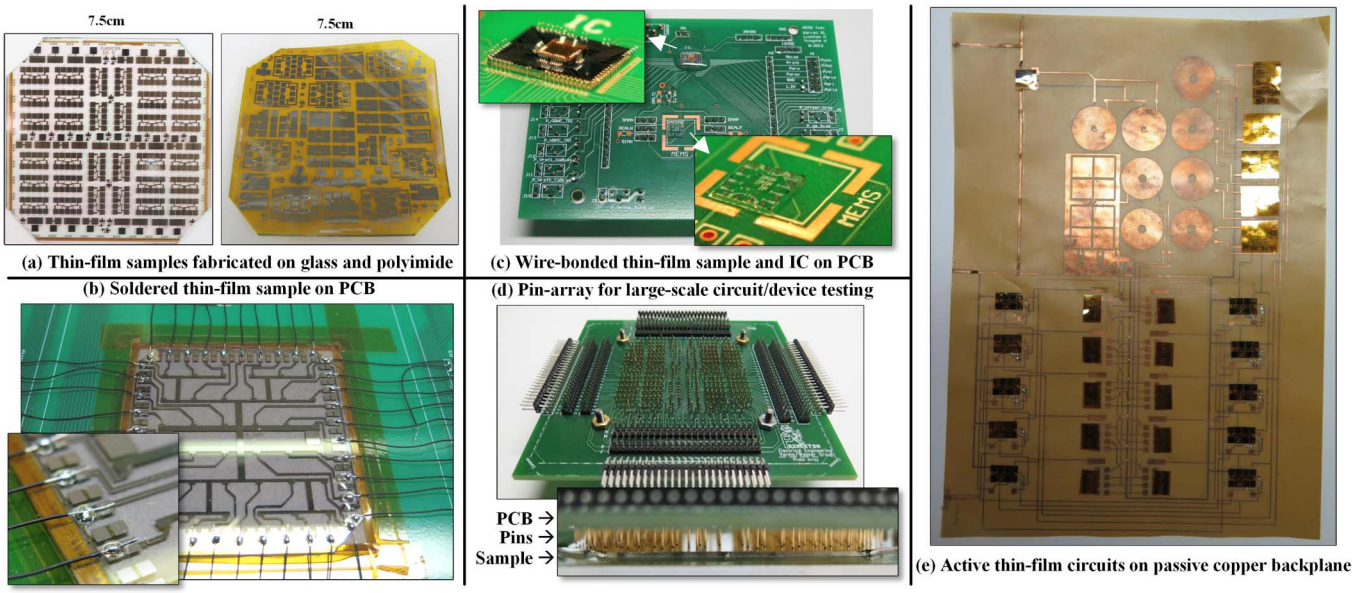

Fig. 13. Illustrative examples of provisions for practical system testing, leading up to integrated systems on flexible substrates. (a) a-Si or ZnO thin-film amplifier samples are fabricated on 7.5 cm × 7.5 cm glass and polyimide substrates, using the same fabrication process for both substrates, at temperatures lower than 180 °C. (b) Gold or platinum–gold metallization allows the direct soldering of wires to the thin-film samples, in this case, a light-sensing array. (c) For smaller pitch contacts, wire bonding to a chrome or gold metallization layer is used to interface to a larger test board with exposed copper traces, pictured here is an a-Si Microelectromechanical systems sample on glass. (d) For circuits with a large number of connections, a spring-loaded pin array is used to break out headers on the edge of a PCB. (e) Path to the integration described in this paper with active circuits on polyimide bonded to a copper backplane using unidirectional conductive adhesive. Pictured is a strain-sensing sheet that integrates sensors, access control circuits, modulators, and demodulators, all in thin-film technology.

An important question is what the size of such a generic unit cell should be to integrate the required functionality and to facilitate diverse uses? Its size will depend on electrical performance and manufacturability. From the electrical system's point of view, the unit cell will contain one CMOS IC that controls a thin-film subsystem spread over a surface area A. The two electrical parameters that may determine the area A are power consumption and signal-to-noise ratio.

As an illustration, for digital signals, the energy W is consumed for charging and discharging interconnect capacitances C to voltages V, with $W_C = CV^2$. At frequency f, the ensuing power consumption P is $f \cdot C \cdot V^2$. The density of sensors (or sensor pitch) is set by the application. With each IC interfacing with sensors distributed over the area A, the average energy for accessing a sensor will increase as A increases, due to the resulting increase in average capacitance. For analog signals (sensor outputs), the signal/noise ratio will also become a dominant concern as A increases, due to the increased possibility of stray coupling before signal amplification in the CMOS IC. We foresee using local instrumentation amplifiers made in thin-film technology to serve clusters of sensors. In this hierarchy of sensors/amplifiers/CMOS, the unit cell can be made large if the bandwidth of sensor signals is small enough with respect to the bandwidth of the thin-film amplifiers and the speed of the thin-film circuits used for sensor accessing (e.g., scan-chain circuits). This is often the case for sensors responding to human activity (a few kilohertz). Our experience to date suggests that the unit cell size will range from 0.1 to 1 m^2. If on-sheet thin-film energy-harvesting topologies are adopted, reducing the power consumption will also enable reducing the physical size of the harvesters. Unit cells manufactured by either batch or roll-to-roll fabrication can be made on substrates that are larger than one cell. Today's batch processes for fabricating active-matrix liquid-crystal displays (AMLCDs), including their TFT backplanes, can handle glass substrates with surfaces of up to nearly 10 m^2.

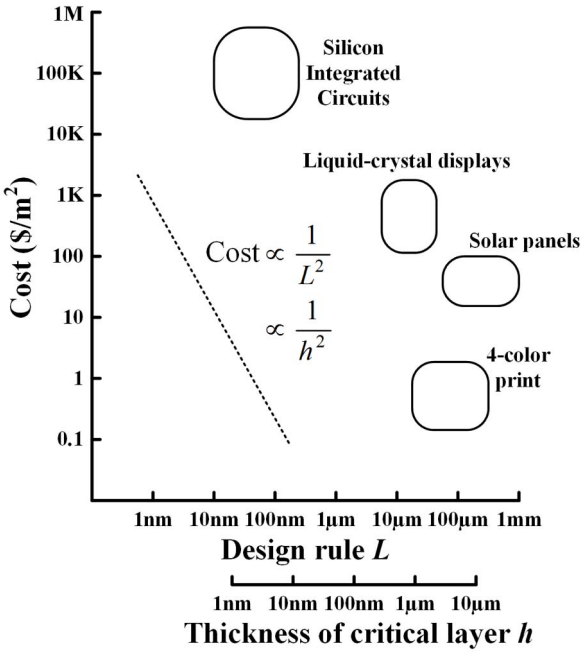

Fig. 14. Cost per square meter of planar products plotted against size of the smallest feature L and the smallest thickness of the critical device layer (e.g., gate dielectric) h.

Experience of the passive flexible electronic industry suggests that cost will play a dominant role in the introduction of large-area flexible electronic systems. In this respect,

the cost experience of active planar electronics over the past 20 years is encouraging. Since the mid-1990s, the cost of (AMLCDs) has dropped from ∼U.S. $10 000 to ∼U.S. $100/m^2, and the cost of thin-film solar panels from ∼U.S. $500/m^2 to less than U.S. $100/m^2 [34]. The AMLCD cost reduction by a factor of ∼100 was achieved without fundamental changes in materials and manufacturing technologies. Substantial further cost reduction will be achieved by the introduction of new technologies, for example, the additive printing of device materials. The cost of large-area systems will be determined by factors similar to those that determine cost of the technologies shown in Fig. 14. The large-area thin-film part of such systems will tend to costs closer to those of high-quality print, perhaps to one-tenth of today's AMLCDs, i.e., ∼U.S. $10/m^2. The CMOS circuits will be hybrid integrated at a spatial density of 1–10/m^2. A realistic guide to the cost of a packaged IC is the present cost of smart cards, which is U.S. $1–U.S. $3 per card. Therefore, one can foresee eventually reaching a systems cost in the several U.S. $10/m^2 range. This cost will enable the lining of entire automobile exteriors and interiors, or decorating the walls and ceilings of living rooms with wallpaper-like large-area electronic systems.

VIII. Conclusion

A large-area flexible electronic system technology is described, which relies on the hybrid integration of large thin-film circuits with CMOS ICs. One important aspect of such systems is the layering by lamination of subsystems-on-flex modules on a large passive backplane. In-plane interconnections are made via the passive backplane. Vertically, bottom to top, the subsystems are interconnected without using hard-wired connections. Instead, they are coupled either capacitively for signal transmission or inductively for signal or power transmission. These inductive or capacitive interfaces can be quite tolerant to variations in overlay alignment and of surface relief or adhesive thickness. The interconnection technique presented in this paper will make an important contribution to the success of flexible large-area electronic systems.

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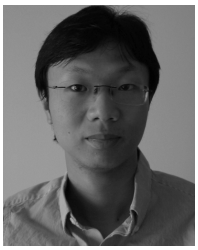

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