Impact of bending on flexible metal oxide TFTs and oscillator circuits

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Abstract **—** Thin-film circuits on plastic capable of high-frequency signal generation have important applications in large-area, flexible hybrid systems, enabling efficient wireless transmission of power and information. We explore oscillator circuits using zinc-oxide thin-film transistors (ZnO TFTs) deposited by the conformal, layer-by-layer growth technique of plasma-enhanced atomic layer deposition. TFTs on three substrates—glass, 50-μm-thick freestanding polyimide, and 3.5-μm-thick spin-cast polyimide—are evaluated to identify the best candidate for high-frequency flexible oscillators. We find that TFTs on ultrathin plastic can endure bending to smaller radii than TFTs on commercial 50-μm-thick freestanding polyimide, and their superior dimensional stability furthermore allows for smaller gate resistances and device capacitances. Oscillators on ultrathin plastic with minimized parasitics achieve oscillation frequencies as high as 17 MHz, well above the cutoff frequency f_T. Lastly, we observe a bending radius dependence of oscillation frequency for flexible TFT oscillators and examine how mitigating device parasitics benefits the oscillator frequency versus power consumption tradeoff.

Keywords *— oxide thin-film transistor (TFT), plasma-enhanced atomic layer deposition (PEALD), TFT circuits, thin-film/CMOS hybrid systems, flexible electronics, large-area electronics (LAE).*

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1 Objective and background

Large-area electronics (LAE) offers unprecedented capabilities as a technology for sensing. This is because its characteristic low-temperature processing enables compatibility with a variety of flexible substrates and materials for forming diverse transducers. While a broad set of sensors have been demonstrated,[1–4] creating full sensing systems with exclusively low-temperature compatible components remains challenging because of the low performance of circuits made of most thin-film semiconductors. Full LAE sensing systems can be achieved effectively with a hybrid approach in which silicon-CMOS ICs are coupled with LAE components [thin-film transistor (TFT) circuits, sensors, large-area passive inductors and capacitors, thin-film solar cells, batteries, etc.].[5–7] In our approach, we circumvent lengthy fabrication processes and low yield of monolithic system integration by fabricating large-area subsystems with different functionalities on separate polyimide sheets, which are then laminated together to form a single flexible system. This lamination method is made robust by the use of non-contact inductive or capacitive interfaces for wireless data and power transfer between subsystems, as illustrated in Fig. 1.

The ease of assembly that inductive and capacitive coupling offers provides yet another motive for raising the bandwidth of TFT circuits: raising the frequency increases the power efficiency of such non-contact LAE interfaces.[8] Raising circuit bandwidth calls for raising the field-effect mobility of the TFTs from which the circuits are made. TFTs made of amorphous hydrogenated silicon (a-Si), when processed at plastic-compatible temperatures, have field-effect mobilities of ~0.5 $cm^2 V^{-1} s^{-1}$, which restricts the frequency of oscillator circuits made of a-Si TFTs to ~2 MHz.[8,9] We address this challenge for ultra-flexible applications by (i) employing zinc oxide (ZnO) with electron mobility of ~10 $cm^2 V^{-1} s^{-1}$ as the TFT channel material, (ii) using atomic-layer deposition (ALD) as the ZnO growth technique, with a polyimide-compatible growth temperature of 200 °C, and (iii) growing on ultrathin (~3.5 μm) polyimide foil that remains fixed to a temporary carrier during TFT processing. Two important advantages of the ensuing dimensional stability of the plastic substrate are a high device yield over large surface areas and the ability to reduce parasitic overlap capacitances. An additional advantage for working on plastic substrates is provided by the ALD growth, which is highly conformal and hence quite tolerant to surface roughness, which again raises fabrication yield.

With this technology, we then employ a resonant circuit topology that permits the oscillator to operate above the TFT's cutoff frequency, f_T, because the TFTs are designed with high unity power gain frequency f_{MAX}. High TFT f_{MAX} can be achieved if TFT parasitics, particularly gate resistance and gate-source/drain overlap capacitance, can be minimized,

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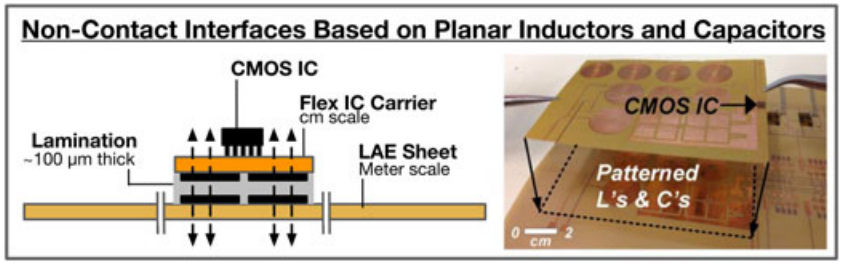

FIGURE 1 — Cross-sectional schematic (left) and photo (right) of inductive and capacitive non-contact interfaces between subsystem sheets in LAE hybrid systems.[5]

which results in high-frequency (~17 MHz) oscillations on plastic. To our knowledge, the presented circuits represent the fastest oscillators fabricated directly on ultrathin (<5 μm) plastic at temperatures entirely ≤200 °C.

In this paper, we describe layer growth, device fabrication, and circuit design and performance on ultrathin flexible polyimide foil and evaluate bending behavior of devices and circuits.

2 ZnO TFTs on plastic substrates

2.1 Substrate materials

In our work, we use three types of substrates: glass, freestanding polyimide (50 μm thick), and ultrathin (3.5 μm thick) spin-coated polyimide. We use glass substrates for the purposes of initial device and circuit validation. Between the flexible plastic substrates, each has its advantages: freestanding 50-μm-thick polyimide can be incorporated more readily into roll-to-roll processing lines, but spin-coated 3.5-μm-thick polyimide exhibits superior dimensional stability and opens up a new range of applications calling for ultrathin, ultra-flexible, or conformal materials. We investigate the effects of bending on TFTs on both of these plastic substrates.

Glass substrates are 1.1-mm-thick Corning 1737 glass that are cleaned in a hot, sonicated Micro-90 (International Products Corp., Burlington, NJ, USA) solution before gate metal deposition. Freestanding polyimide substrates are cut to size from a roll of industry-grade 50-μm-thick DuPont Kapton-E, cleaned in the same manner as glass substrates, and outgassed for 8 h under vacuum at 200 °C before metallization. To prepare spin-coated polyimide substrates, a single layer of HD Microsystems PI2611 is spin-coated onto a silicon carrier wafer with native oxide (as in Pappas[10] and Li and Jackson[11]), cured for 3 h in an N_2 environment at 350 °C, and lastly outgassed for 2 h under vacuum at 200 °C before metallization. Its final thickness (set by the spin speed of 4000 rpm) is approximately 3.5 μm. For both plastic substrates, fabrication proceeds directly on the bare polyimide surface, without a barrier layer.

Freestanding (non-bonded) 50-μm-thick polyimide substrates are temporarily laminated to a glass substrate during lithography and expand and contract significantly during the fabrication process. In Fig. 2, we see an example of this deformation: two TFTs on the same substrate are designed to have 10-μm gate-source/drain overlaps on each side but show very different alignments of the source and drain metal pads (yellow) over the gate metal line (gray) at the end of fabrication. The TFT on the left, which is located in the center of the sample, has relatively equal gate-source/drain overlaps, but the TFT on the right, which is on the right side of the sample, is severely misaligned. To avoid this problem and ensure uncompromised TFT yield across the full sample, the gate-source/drain overlap dimension X_{OV} is typically kept to 15 μm for TFTs on freestanding polyimide substrates. The same result is observed in a-Si TFTs.[12] This large X_{OV} imparts a significant overlap capacitance $C_{OV} = C_{GD} = C_{GS}$, which will be discussed later.

Unlike TFTs fabricated on freestanding polyimide substrates, TFTs on spin-cast 3.5-μm-thick polyimide do not expand or contract measurably during fabrication because they are rigidly affixed to a carrier wafer. For this reason, this TFT alignment dimension, the gate-source/drain overlap X_{OV} (and again, the $C_{OV} = C_{GD} = C_{GS}$) can be three times smaller, for example, 5 μm, matching the overlap dimension and capacitance on glass.

After processing, TFTs on 3.5-μm polyimide substrates must additionally be delaminated from the carrier. A border in the polyimide is defined with a razor blade, and the entire film is slowly peeled off the carrier along the direction of channel length. Introducing deionized water between the film and the silicon carrier makes this removal significantly easier.

2.2 ZnO/Al_2O_3 TFT materials and fabrication

We choose ZnO as our active semiconductor material because it offers high mobility while requiring less stoichiometric experimentation and control than ternary and quaternary oxides. We use plasma-enhanced atomic layer deposition (PEALD) because (i) it is compatible with the temperature range for flexible substrates, (ii) it is a technique that results in highly conformal films that can robustly cover rough plastic surfaces, and (iii) it provides an exceptional degree of control over layer thicknesses.[13] This last point is significant because the ZnO layer thickness in our TFTs is just 20 nm.

Al_2O_3 serves as an effective gate dielectric that can withstand large electric fields (7 MV cm^{-1}), and because of the PEALD deposition, it also forms a conformal coating over rough substrates and large gate metal steps. We also use Al_2O_3 as our back-channel passivation material, because it

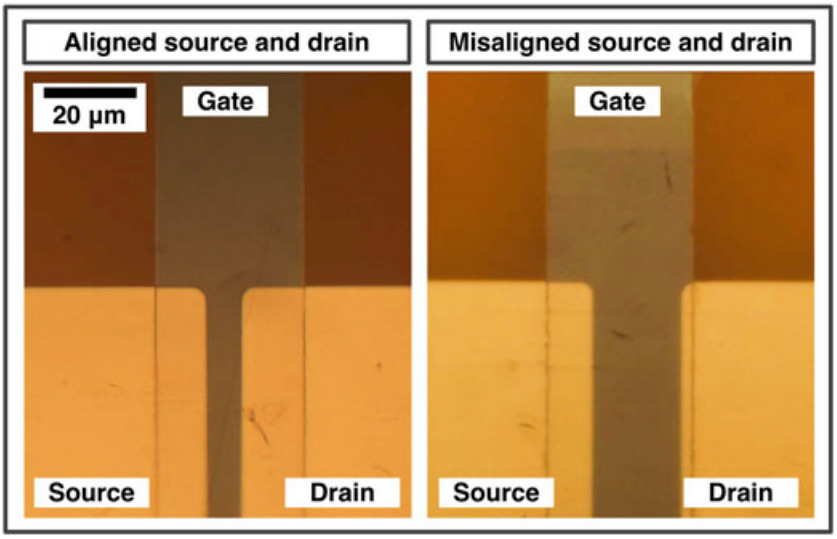

FIGURE 2 — Because of expansion and contraction of the polyimide substrate during processing, gate-source/drain overlaps X_{OV} on freestanding 50-µm-thick polyimide must be made large. Even 10-µm overlaps are problematic, resulting in well-aligned devices (left) and poorly aligned devices (right) in different parts of the same sample.

results in TFTs with minimal threshold voltage shift and negligible hysteresis. The three oxide layers (dielectric, active, and passivation) are deposited in a single run, without breaking vacuum.[14]

We fabricate bottom-gate non-self-aligned ZnO TFTs over 7.5-cm × 7.5-cm areas, depositing the Al_2O_3 gate dielectric, ZnO active layer, and Al_2O_3 passivation layer over a bottom gate in a custom PEALD system based on Mourey *et al.*[13] In each deposition cycle, metal organic precursor (diethylzinc or trimethylaluminum) diffuses into the reaction chamber in vapor form and adsorbs to the substrate surface. The metal organic is oxidized when a capacitive RF plasma of weak oxidant gas (nitrous oxide or carbon dioxide) is struck, which results in approximately a monolayer of zinc or aluminum oxide. The plasma power density is 0.1 W cm^{-2}, and the deposition temperature is 200 °C. A low power density results in transistors with low hysteresis, and elevated (although still plastic compatible) temperature helps to prevent multilayers of metal organic precursor from condensing on the substrate surface. Temperatures above 200 °C result in reduced mobility (~60%), while temperatures below 200 °C appear to have slightly higher (5–10%) mobility, but also increased variation over the substrate area, but could be pushed lower to enable a wider range of plastic substrates. After PEALD steps, additional processing steps deposit the source and drain metals, define the active area, and deposit interconnect metal. Figure 3 shows the device cross-section and top view and specifies layer thicknesses. The gate-source/drain overlap dimension X_{OV} is indicated in red. The top view at right shows that source, drain, and gate pads are capped with an additional 50-nm Cr, 100-nm Au top-metallization layer for low-resistance interconnects between TFTs.

Table 1 gives a comparison of parameters and dimensions between TFTs on glass, freestanding 50-µm polyimide, and 3.5-µm delaminated polyimide and shows small differences in mobility and threshold voltage. Figure 4 shows typical ZnO TFT I–V transfer curves and shows that devices fabricated on ultrathin polyimide are comparable with devices fabricated on glass.

Figure 5 shows a photo of a delaminated 3.5-µm polyimide foil with ZnO TFTs.

2.3 Strain limitations of ZnO TFTs on thick and thin flexible polyimide substrates

To establish the bending limits of TFTs on flexible substrates under strain, TFTs were bent into cylinders of decreasing radius in both convex (with the TFT on the outer surface of the substrate) and concave (with the TFT on the inner surface of the substrate) configurations, with the TFT channel length perpendicular to the axis of the cylinder, as shown in Fig. 6. The convex configuration corresponds to the application of tensile strain, while the concave configuration corresponds to the application of compressive strain. For tensile (convex) bending, TFTs were bent around metal drill bits. For compressive (concave) bending, custom plastic half-pipes were laser cut to ensure that the thin TFT layers would not be abraded by contact with a drill bit surface, and TFTs were curled inside the half-pipes. Current–voltage sweeps were performed before and after the strain was applied to the TFTs: the TFTs were measured initially, bent to the desired radius, flattened, and then measured again. The TFT *W*/*L* was 500 µm/5 µm (Table 1).

2.3.1 Bending ZnO TFTs on freestanding polyimide

Thin-film transistors on 50-µm-thick, freestanding polyimide foil exhibit electrical changes when bent around cylinders of decreasing radius in both tension and compression. The percent change in mobility and threshold voltage as a function

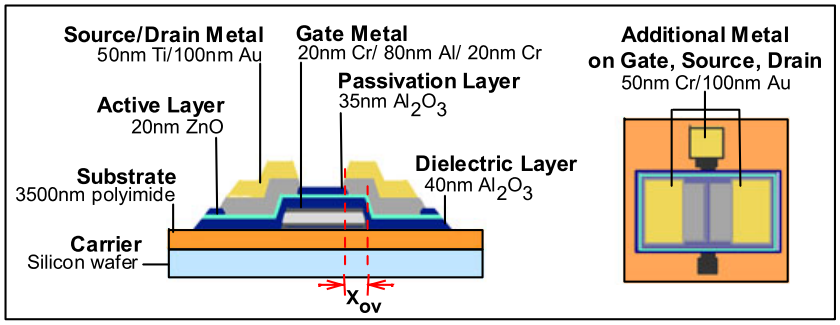

FIGURE 3 — Cross-section and top view of ZnO TFT fabricated on an ultrathin 3.5-µm spin-cast polyimide substrate. ZnO TFTs fabricated on freestanding 50-µm polyimide have a similar structure but are not attached to a carrier wafer and have thinner gate metal. ZnO TFTs on 1737 Corning glass have an identical structure but without a carrier wafer.

TABLE 1 — TFT parameters on glass and PI substrates.

	Glass	50 µm PI	3.5 µm PI
μ ($cm^2\,V^{-1}\,s^{-1}$)	13.4 ± 2.0	8.3 ± 1.1	11.3 ± 1.2
V_T (V)	2.0 ± 0.4	2.9 ± 0.2	2.2 ± 0.3
C_{GD}/W (fF μm^{-1})	10	30	10
R_{gate}/W ($\Omega\,\mu m^{-1}$)	0.07	0.04	0.07
W (µm)	500	500	500
L (µm)	5	5	5
X_{OV} (µm)	5	15	5

Mobility and threshold voltage are extracted from the saturation portion of the I_D–V_{GS} curve at V_{DS} = 6 V for 15 devices for each substrate.
PI, polyimide; TFT, thin-film transistor.

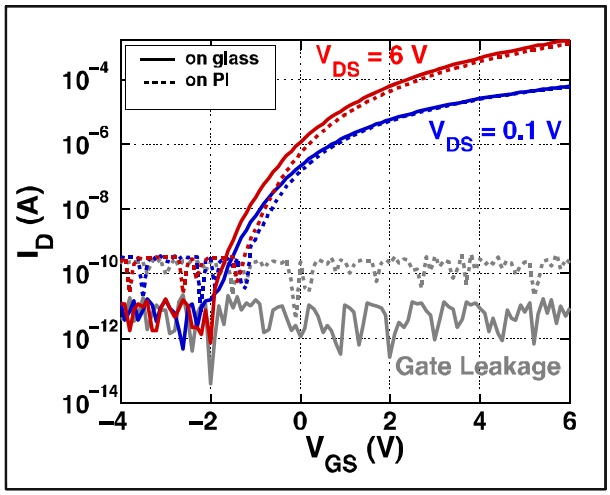

FIGURE 4 — TFT transfer characteristics for V_{DS} of 0.1 and 6 V for devices on glass (solid) and 3.5-µm polyimide (dashed) after delamination.

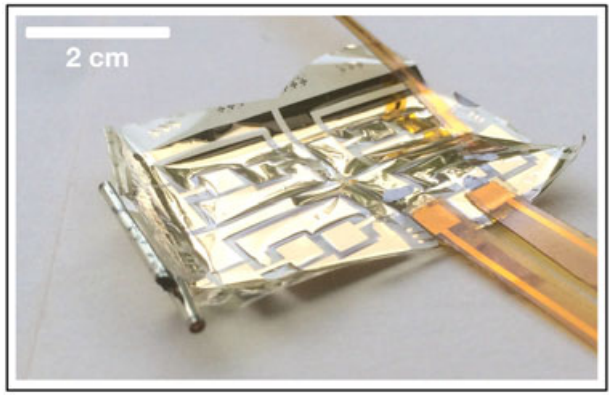

FIGURE 5 — ZnO TFTs on 3.5-µm-thick polyimide delaminated from silicon carrier. Flexible laminated connectors to off-sheet inductors are also shown.

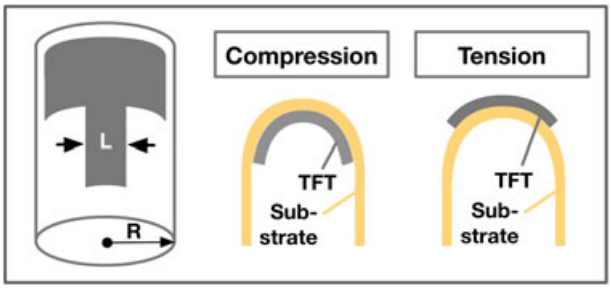

FIGURE 6 — Schematic indicating (leftmost) bending direction and (right) cross-sectional views of compressive and tensile strain configurations.

of inverse bending radius (= curvature) is plotted in Fig. 7. We see that the mobility steadily reduces in both tensile (blue) and compressive (red) cases and that the threshold voltage increases slightly, even at large bending radii. Even at a bending radius of 3.5 mm in compression, mobility has reduced by about 30% from its initial value. Surprisingly, mobility decreases for both tensile and compressive strain. At the smallest radii (a range of 2–3 mm), the gate dielectric suddenly fails, and catastrophic gate leakage results in total device failure.

Because the TFT is grown on a compliant substrate, the strain should be estimated via Eq. 1[15]:

$$\epsilon_{\text{top surface}} = \left(\frac{d_f + d_s}{2R}\right)\left(\frac{1 + 2\eta + \chi\eta^2}{(1 + \eta)(1 + \chi\eta)}\right) \qquad (1)$$

where d_f, d_s are the film and substrate thicknesses, R is the bending radius, $\eta = d_f / d_s$ (the ratio of film-to-substrate thicknesses), and $\chi = Y_f / Y_s$ is the ratio of the Young's moduli of the film and the substrate. Assuming that the TFT thin-film layers

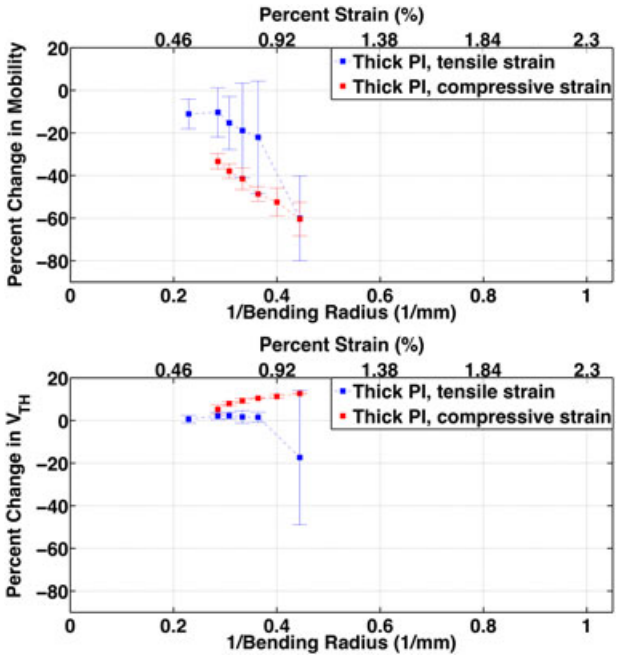

FIGURE 7 — Percent change in mobility (top) and threshold voltage (bottom) from initial flat values after application of tensile (blue) and compressive (red) strain for ZnO TFTs on 50-µm freestanding polyimide. Mobility degradation is notable even at a bending radius of 3 mm. For each bending radius and each strain configuration, four TFTs were tested.

have total thickness 300 nm and Young's modulus 100 GPa, and using 5 GPa as the Young's modulus for the polyimide substrate,[12] the TFTs break catastrophically between 0.7% and 1.1% strain in compression and tension, although they show signs of degradation much earlier.

Microscope images of TFTs that failed in tension (left) and compression (right) are shown in Fig. 8 and suggest that physical damage for bending the TFTs on thick polyimide results in electrical degradation and ultimate device failure. We observe that the transparent 40-nm-thick gate dielectric cracks and flakes off in the immediate vicinity of the 100-nm gate metal step (gray line). In many areas of the sample, the gate metal itself shows significant cracking. These observations indicate that for robust flexible TFTs on freestanding polyimide, the gate metal thickness must be reduced even though this results in increased gate resistance. In these images, we see again the alignment challenge with TFTs on freestanding polyimide, which limits the value of the gate-source/drain overlap X_{OV} to 15 µm.

2.3.2 ZnO TFTs on ultrathin spin-cast polyimide

Ultrathin spin-cast substrates offer distinct advantages for flexible TFTs. For the same bending tests performed in Section 2.3.1, TFTs on ultrathin spin-cast substrates exhibit very little change in mobility or threshold voltage even down to bending radii of 1 mm in both tension and compression, as shown in Fig. 9.

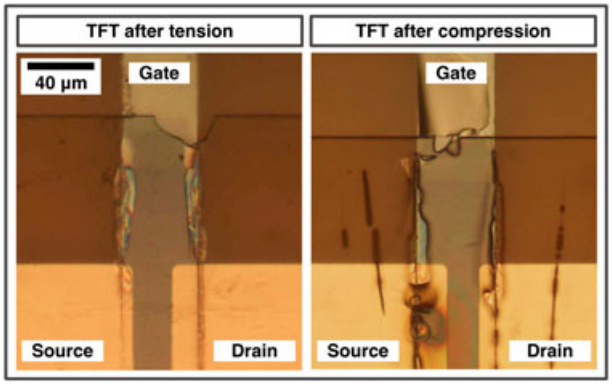

FIGURE 8 — ZnO TFTs on 50-µm-thick freestanding polyimide after applying tensile strain (left) and compressive strain (right). In both cases, we observe that the transparent oxide layers crack and begin to flake off, particularly along the gate metal step.

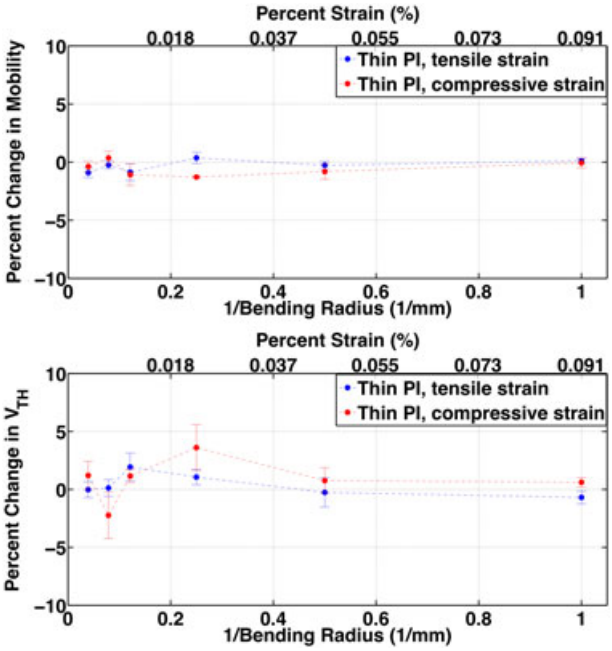

FIGURE 9 — Percent change in mobility (top) and threshold voltage (bottom) after application of tensile (blue) and compressive (red) strain for ZnO TFTs on 3.5-µm polyimide change very little down to a bending radius of 1 mm. Each data point corresponds to five TFTs.

Strained TFTs furthermore show no visual signs of fatigue. For this reason, we are able to employ a gate metal up to 120 nm thick for TFTs on spin-cast substrates without limiting the bending capability of the TFTs. As discussed previously, the absence of material contraction/expansion during processing also allows TFTs on spin-cast substrates to maintain an X_{OV} of 5 µm, as on glass, without alignment difficulties affecting yield.

Because the ultrathin substrates are 3.5 µm thick, the substrate thickness is only about 10× thicker than the total TFT layer thickness. This reduces the strain experienced by the whole structure. Via Eq. 1, the strain corresponding to a 1-mm bending radius is only ~0.09%, so it is not surprising that the electrical parameters of the TFT are relatively constant.

Below this radius, testing becomes challenging. "Folding" the substrate on top of itself, directly across a TFT, causes a sharp (but undefined) bending radius ≤500 µm (Fig. 10). The TFT characteristics remain unchanged, however, after release of the fold (Fig. 11), demonstrating the clear superiority of ultrathin substrates for applications in which the substrates must be deformed.

3 High-frequency TFT oscillator design

3.1 Resonant oscillator topology for high-frequency TFT circuits

Resonant oscillator circuits are essential to the hybrid LAE architecture because they generate high-frequency oscillations required for efficient non-contact inductive or capacitive interfaces between different functional sheets within a system (Fig. 1). High-frequency operation of LAE circuits is typically limited by low TFT transconductance g_m and large gate-source/drain and gate-channel capacitances C_{GS}, C_{GD}, and C_{GCh} resulting from micron-scale X_{OV} and L. To overcome these obstacles, we use high-quality planar inductors enabled by LAE[9] to resonate out large TFT capacitances in a resonant inductive–capacitive (LC) oscillator circuit. In this way, TFT oscillators operating above f_T can be robustly achieved. In this work, we use the cross-coupled LC oscillator topology, pictured in Fig. 12. L_{ind} and R_{ind} refer to the inductance and resistance of the planar inductor, *TFT1* and *TFT2* are two equally sized ZnO TFTs (sizing as before, $W/L = 500\,\mu m/5\,\mu m$, $X_{OV} = 5\,\mu m$), V_{SUPPLY} is the DC supply voltage, V_{OUT} is the node at which the output is measured, R_{gate} is the TFT gate resistance, and $C_{GD1,2}$, $C_{GS1,2}$, and C_{GCh} are the TFT overlap capacitances and the gate-to-channel capacitance.

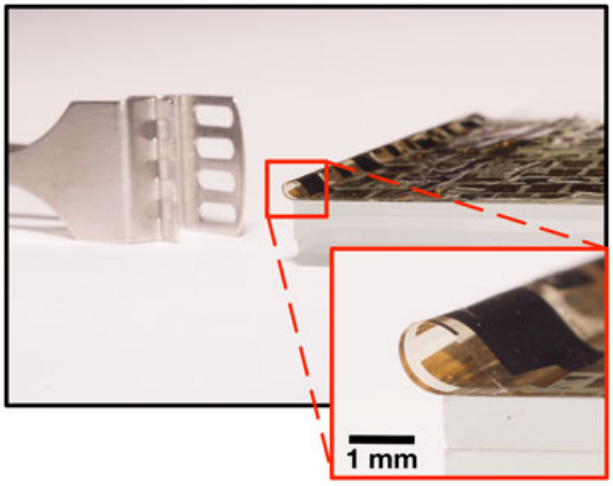

FIGURE 10 — ZnO TFTs on 3.5-µm-thick delaminated polyimide folded over itself with TFTs on the inside experience a ≤500-µm bending radius but little electrical change. Inset shows fold radius close up.

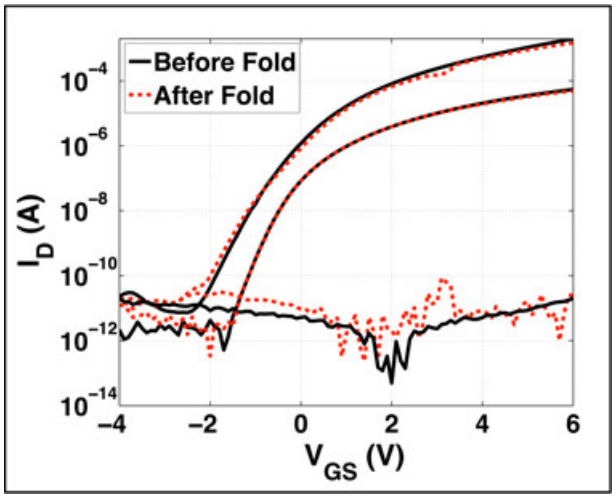

FIGURE 11 — TFT transfer characteristics before (black) and after (dashed red) folding in half in compressive configuration. Fold corresponds to a ≤500-µm bending radius. Top to bottom: I_D for $V_{DS} = 6$ V, $V_{DS} = 0.1$ V, and I_G.

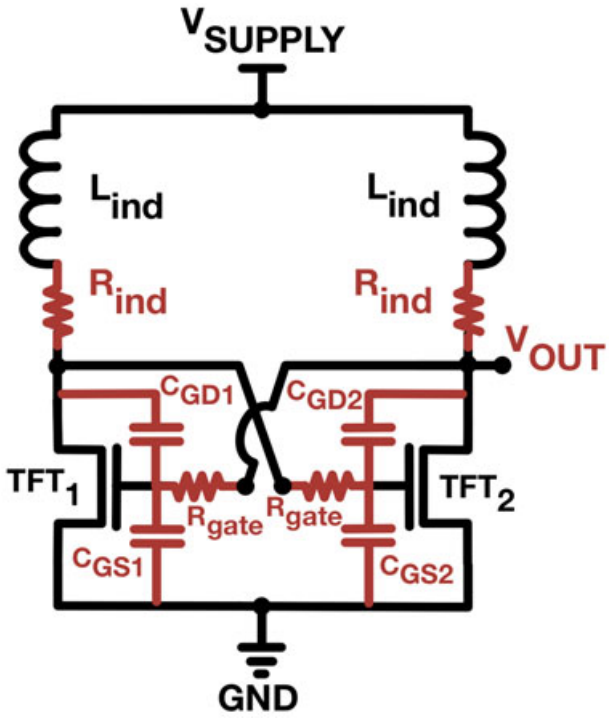

FIGURE 12 — Schematic of the cross-coupled LC oscillator topology, with relevant parameters labeled. Parasitic quantities are drawn in red.

If the positive feedback condition of this circuit is satisfied,

$$g_m R_{TANK} = \frac{\left(\mu C_{GCh}\frac{W}{L}(V_{GS} - V_T)\right)L_{ind}}{C_{Par}\left(R_{ind} + R_{gate}\right)} > 1, \qquad (2)$$

where g_m is the TFT saturation transconductance, then the circuit will oscillate at a frequency f_{osc} set by the inductance of the planar inductor L_{ind} and the C_{par} of the circuit:

$$f_{osc} = 1/\left(2\pi\sqrt{L_{ind}C_{par}}\right), \quad (3)$$

where C_{par}, due to Miller capacitances, is dominated by TFT overlap capacitances:

$$C_{par} = 2\times(C_{GD1} + C_{GD2}) + C_{GS1,2} + C_{GCh} \approx 5\times C_{OV} + C_{GCh} \quad (4)$$

For a given TFT geometry and fabrication process, positive feedback is made easier by either (i) boosting V_{SUPPLY} and thereby boosting transconductance g_m or (ii) increasing the size of the inductor L_{ind}. Boosting V_{SUPPLY} results in increased power consumption, while increasing L_{ind} increases area and reduces the oscillation frequency (according to Eq. 3). Hence, careful circuit design and TFT materials improvement have important impacts on system-level metrics. In the following section, we focus on design of the oscillator parameters that impact the feedback condition (Eq. 2) and frequency f_{osc} (Eq. 3).

3.2 Optimization of TFT f_{MAX} for oscillations beyond f_T

Mobility μ and device capacitances C_{GS}, C_{GD}, and C_{GCh} are most prominent in setting the TFT's cutoff frequency, f_T, the frequency at which current gain is unity: $f_T = g_m/2\pi(C_{GD} + C_{GCh} + C_{GS})$. This motivates using ZnO for high g_m and minimizing gate-source/drain overlap size and channel length, all to 5 µm in this work, which as discussed is achievable on glass and spin-cast polyimide substrates but not on freestanding polyimide. At $V_{GS} = V_{DS} = 9$ V, we have measured that our ZnO TFTs on glass substrates ($W/L = 500$ µm/5 µm, $X_{OV} = 5$ µm) have $f_T = 12.9$ MHz.

As discussed, resonant circuit topologies enable the oscillator frequency f_{osc} to exceed f_T if the condition for positive feedback (Eq. 2) is met at small inductance L_{ind}. However, an additional TFT limitation imposes a caveat: f_{MAX}, the TFT's unity power gain frequency, must exceed this resonant oscillation frequency f_{osc}, or oscillations will not occur. f_{MAX} is expected to exhibit a strong dependence on R_{gate}:

$$f_{MAX} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi f_T C_{GD} R_{gate} + \frac{R_{gate}}{r_o}}}, \quad (5)$$

Thus, R_{gate} is a new focus for TFT optimization, which is typically not critical for digital circuit delay or for the cutoff frequency f_T. Our standard TFT process for digital applications has a 100-nm-thick sputtered chrome gate with ~3 Ω/sq sheet resistance. This was reduced to 0.3 Ω/sq by sandwiching an aluminum layer up to 80 nm thick between Cr bottom and top layers, increasing the overall gate thickness to 120 nm. Capping the Al layer with ≥20 nm of Cr prevents sharp hillocks from forming during 200 °C PEALD deposition; hillocks can puncture the thin 40-nm Al_2O_3 gate dielectric and create electrical shorts. For this bottom-gate process, keeping the total gate metal thickness ≤120 nm ensures adequate step coverage by the 40-nm gate dielectric across the 7.5-cm × 7.5-cm substrates. At this thickness, although the dielectric to gate thickness ratio is 1:3, the conformal ALD deposition of the oxide materials ensures that there are zero gate-to-source/drain shorts. Because Al is more ductile than Cr, this composite gate material has the added advantage of preventing the gate metal from cracking under strain on ultrathin polyimide substrates.

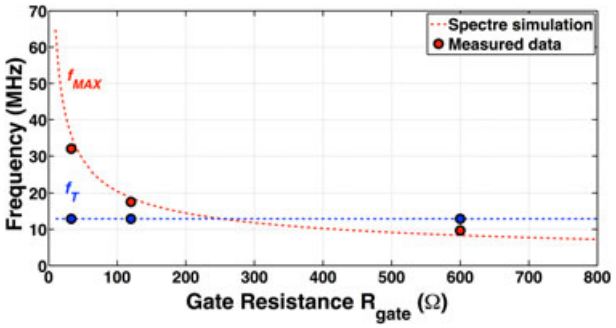

FIGURE 13 — ZnO TFT f_{MAX} (red) depends on gate resistance R_{gate}. Measured and simulated f_T also shown (blue). Measurements taken on glass.

To illustrate how important R_{gate} reduction is to raising f_{MAX}, Fig. 13 shows the measured f_{MAX} of ZnO TFTs having three different gate resistances in red (f_{MAX} values predicted by Spectre simulation based on a Level-61 SPICE model for our ZnO TFTs are also shown). f_T values from measurement and simulation are plotted on top in blue and as expected do not exhibit a dependence on gate resistance. With the reduced C_{GD}, C_{GS}, and R_{gate} specified in this paper, we measure f_T of 12.9 MHz and f_{MAX} of 35 MHz at a bias condition of $V_{GS} = V_{DS} = 9$ V on glass substrates.

Note that $g_m R_{TANK}$ (Eq. 2) depends inversely on the sum of $R_{gate} + R_{ind}$. Because oscillators presented here employ low-resistance planar copper inductors, $R_{gate} + R_{ind} \approx R_{gate}$, and hence, R_{gate} optimization has powerful consequences.

4 Results: demonstrated oscillator circuits

4.1 ZnO TFT-based oscillator on plastic

Using ZnO TFTs on 3.5-µm polyimide with optimized f_{MAX} (reduced R_{gate} and high f_T), we construct the cross-coupled LC oscillators described in Section 3.1. To approach the frequency limitation (f_{MAX}) set by the TFTs, we employ a range of planar spiral inductors with varying values of L_{ind}, all with low-resistance (low R_{ind}) 25-µm-thick copper traces. Inspection of Eq. 2 and Eq. 3 indicates that reduction of R_{gate} and C_{par} allows the positive feedback condition (Eq. 2) to be met with reduced L_{ind} values, which then results in higher oscillation frequencies (Eq. 3). L_{ind} was reduced in discrete increments by replacing larger spirals with smaller ones until oscillation was no longer observed. Figure 14 shows the oscilloscope-measured output waveform of a cross-coupled

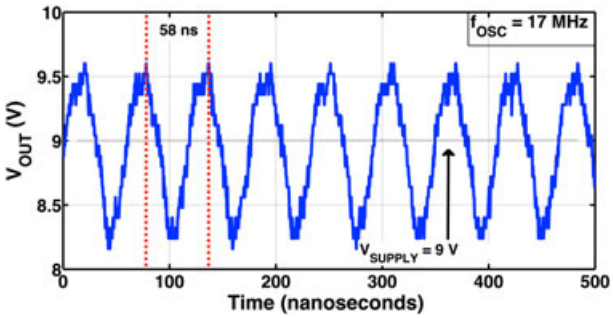

FIGURE 14 — Output waveform of ZnO TFT oscillator on a 3.5-µm polyimide substrate.

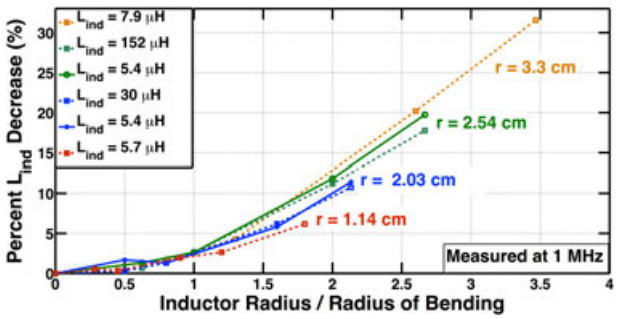

FIGURE 16 — Bending planar spiral inductors on plastic significantly impacts inductance value, which impacts f_{OSC}.

oscillator on a 3.5-µm polyimide substrate with L_{ind} = 3.7 µH. At V_{SUPPLY} of 9 V, the circuit oscillates at f_{OSC} = 17 MHz, which significantly above the f_T of 12.9 MHz.

We measured the oscillation frequency while bending the plastic substrate into a cylinder, with the TFT channel length perpendicular to the direction of axis of the cylinder, as in Fig. 6, and with TFTs on the outside of the cylinder (corresponding to tensile strain). The change in oscillation frequency as a function of bending radius of the TFTs in the circuit is provided in Fig. 15. When the entire oscillator (TFTs and inductors) is bent to the same radius, the frequency changes measurably. However, when the inductors are flattened, but the TFTs remain bent, the oscillation frequency returns to its unbent value.

This behavior is explained as follows: the inductance L_{ind} of the planar inductors decreases as its bending radius increases, as shown in Fig. 16. This causes the oscillator frequency to shift upwards upon bending. Inductors with very different inductances but identical outer radius (i.e., different numbers of turns) have nearly identical bending behavior, which suggests that inductor geometry plays a role in this effect. For the inductor used in the oscillator measured while bending in Fig. 15, we see a 10% reduction in inductance at an inverse bending radius of 0.08 inverse millimeters. Equation 3 predicts a 5% increase in oscillation frequency as a result of a 10% inductance decrease, which is exactly the result we see in Fig. 15. This change in oscillation frequency as a function of bending radius is important to consider in large-area flexible systems employing resonant LC oscillators.

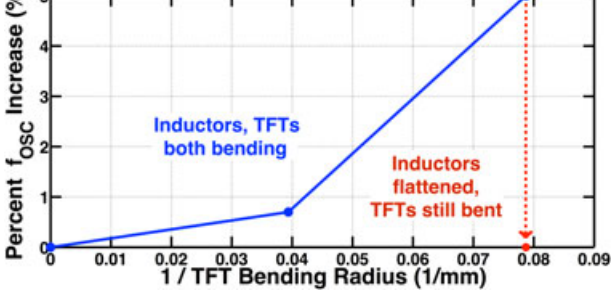

FIGURE 15 — Bending oscillators impacts oscillation frequency through the inductor, not the TFT (TFTs are in tension; red point corresponds to unstrained inductor). In this circuit, L_{ind} = 152 µH, V_{SUPPLY} = 6.3 V, and unbent f_{OSC} = 2.2 MHz.

5 Oscillation frequency and power consumption

Because oscillator frequency can be increased at the cost of increased power consumption (by increasing V_{SUPPLY} to increase g_m), it is useful to look at power consumption and frequency together. Figure 17 shows the maximum oscillation frequency we could achieve at a given level of power consumption for cross-coupled oscillators constructed from reduced-R_{gate} ZnO TFTs on glass, high-R_{gate} ZnO TFTs on glass, and reduced-R_{gate} ZnO TFTs on 3.5-µm polyimide. As seen, the use of ZnO TFTs with low R_{gate} in our cross-coupled oscillators leads to a substantial frequency–power improvement. The frequency/power consumption tradeoff for flexible oscillators is worse than glass substrate counterparts, because of a higher effective R_{gate} (52 Ω instead of 33 Ω) imparted by parasitic interconnect resistances outside of the TFTs in this circuit. With improved interconnects, we expect the results for oscillators on polyimide to approach the result for glass.

6 Conclusions

In this work, we evaluated ZnO TFTs on plastic substrates to identify the best material choices for fast, flexible oscillators in LAE non-contact interface circuits. Using PEALD ZnO for highly conformal films with excellent thickness control, we built TFTs with mobilities of ~10 $cm^2 V^{-1} s^{-1}$ on glass, 50-µm-thick freestanding polyimide, and 3.5-µm-thick spin-cast

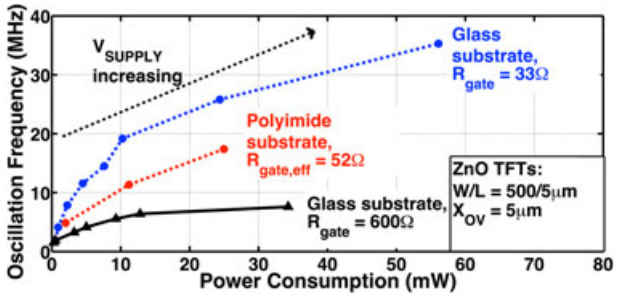

FIGURE 17 — Power–frequency comparison. For a given R_{gate}, oscillator frequency and power consumption are both increased by boosting V_{SUPPLY} to raise g_m (to more easily satisfy the positive feedback condition of Eq. 2) and then reducing L_{ind} to increase oscillation frequency (via Eq. 3).

polyimide substrates. TFTs on 3.5-µm-thick spin-cast polyimide substrates have advantages over TFTs on 50-µm-thick freestanding polyimide. In compressive and tensile bending tests, while TFTs on 50-µm-thick freestanding polyimide show electrical and physical deterioration at ~3-mm bending radii, TFTs on 3.5-µm-thick spin-cast polyimide substrates can withstand bending to <1-mm radii without showing significant degradation of mobility or threshold voltage. TFTs on 50-µm-thick freestanding polyimide also exhibit poor dimensional stability during processing and hence require three times larger (15 µm) gate-source/drain overlaps than TFTs on glass for high yield during lithographic alignment, while TFTs on 3.5-µm-thick spin-cast polyimide can maintain the same overlap dimension used on glass (5 µm) because they are affixed to a rigid carrier substrate and cannot expand and contract during processing. This smaller overlap dimension corresponds directly to a smaller parasitic TFT capacitance.

For these reasons—robustness to bending and ability to minimize device parasitics—we made ZnO TFT oscillator circuits on 3.5-µm-thick spin-cast polyimide. These oscillators employ a resonant cross-coupled LC topology and can be optimized for high f_{MAX} by reducing X_{ov} and R_{gate}. TFT oscillators on 3.5-µm-thick spin-cast polyimide exhibit maximal oscillation frequency of 17 MHz, well above the TFT f_T, and exhibit a power–frequency advantage over high-R_{gate} counterparts on glass. Oscillators are also evaluated while bending, and an increase in frequency is observed with decreasing bending radius. The increase in frequency corresponds exactly to the measured reduction in inductance of the planar inductors used. The observed change in oscillation frequency as a function of bending radius is important to consider in large-area flexible systems employing resonant LC oscillators.

Acknowledgments

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References

1 S. C. B. Mannsfeld *et al.*, "Highly sensitive flexible pressure sensors with microstructured rubber dielectric layers," *Nat. Mater.*, **9**, 859–864 (2010). DOI:10.1038/nmat2834.
2 M. Melzer *et al.*, "Wearable magnetic field sensors for flexible electronics," *Adv. Mater.*, **27**, 1274–1280 (2015). DOI:10.1002/adma.201405027.
3 D.-H. Kim *et al.*, "Epidermal electronics," *Science*, **333**, 838–843 (2011). DOI:10.1126/science.1206157.
4 S. Bauer *et al.*, "25th Anniversary Article: a soft future: from robots and sensor skin to energy harvesters," *Adv. Mater.*, **26**, 149–162 (2014). DOI:10.1002/adma.201303349.
5 N. Verma *et al.*, "Enabling scalable hybrid systems: architectures for exploiting large-area electronics in applications," *Proc. IEEE*, **103**, No. 4, 690–712 (2015). DOI:10.1109/JPROC.2015.2399476.
6 T. Someya *et al.*, "Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes," *Proc. Natl. Acad. Sci. U. S. A.*, **102**, No. 35, 12321–12325 (2005). DOI:10.1073/pnas.0502392102.
7 E. Beyne "3D system integration technologies," *2006 International Symposium on VLSI Technology, Systems, and Applications*, 1–9 (2006) DOI: 10.1109/VTSA.2006.251113.
8 W. Rieutort-Louis *et al.*, "A complete fully thin-film PV harvesting and power-management system on plastic with on-sheet battery management and wireless power delivery to off-sheet loads," *IEEE J. Photovoltics*, **4**, No. 1, 432–439 (2013). DOI:10.1109/JPHOTOV.2013.2285959.
9 Y. Hu *et al.* "High-resolution sensing sheet for structural-health monitoring via scalable interfacing of flexible electronics with high-performance ICs," *VLSI Symp. Circuits*, 120-121 (2012) DOI: 10.1109/VLSIC.2012.6243819.
10 C. G. Pappas, "Towards a 100,000 TES focal plane array: a robust, high-density, superconducting cable interface," *IEEE Trans. Appl. Supercond.*, **25**, No. 3, 1–5 (2015). DOI:10.1109/TASC.2014.2379092.
11 H. U. Li and T. N. Jackson, "Oxide semiconductor thin film transistors on thin solution-cast flexible substrates," *IEEE Electron Device Lett.*, **36**, 35–37 (2015). DOI:10.1109/LED.2014.2371011.
12 I.-C. Cheng *et al.*, "Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates," *J. Soc. Inf. Disp.*, **13**, No. 7, 563–568 (2005). DOI:10.1889/1.2001213.
13 D. A. Mourey *et al.*, "Fast PEALD ZnO thin-film transistor circuits," *IEEE Trans. Electron Devices*, **57**, 530–534 (2010). DOI:10.1109/TED.2009.2037178.
14 Y. V. Li *et al.*, "Trilayer ZnO thin-film transistors with *in situ* Al_2O_3 passivation," *IEEE Electron Device Lett.*, **34**, 1400–1402 (2013). DOI:10.1109/LED.2013.2283337.
15 S. Wagner *et al.*, Flexible flat panel displays, G. P. Crawford (ed.) Hoboken, NJ: John Wiley & Sons (2005), p. 7 DOI: 10.1002/0470870508.ch14.

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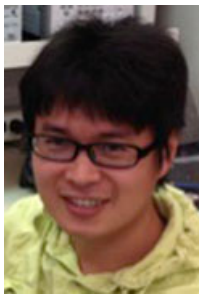

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