Hybrid Large-Area Systems and their Interconnection Backbone (Invited Paper)

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ABSTRACT

Hybrid systems combine Large-Area Electronics (LAE) with high-performance technologies (e.g., silicon CMOS) [1]. With architectural concepts for hybrid systems broadening to match the range of emerging applications, this paper examines modular approaches for multi-sheet, multi-technology integration. It identifies the interfaces required as a critical backbone. For interfaces associated with various system functionalities (sensing, processing, powering), specific approaches are surveyed and analyzed, taking from insights derived from several previous experimental demonstrations of complete hybrid systems.

Keywords

Large-area electronics, hybrid systems, thin-film transistors.

1. INTRODUCTION

Through five decades of Moore's-Law scaling, computation is available to us on an immense scale. This is in large part thanks to a platform technology for realizing computational functions, namely silicon (Si) CMOS. Having a platform technology has enabled the formulation of principled design approaches as well as focused engineering efforts directed at these. This, in turn, has led to sustained advancements of both the entire technological stack and the resulting applications.

However, even with the great number of diverse applications we have today, it is likely that the application space where computation offers potential for impact is even broader. In this paper, we imagine the possibility of applying computation to *all forms of physical signals*. Signals that exist all around us and indeed within us (on/inside our bodies, in the spaces we work and play, within the infrastructure we rely on, etc.) are likely of high importance to us; the application of computation to these can enable systems of correspondingly high value. What limits this today is that, unlike computation, we do not have an established platform technology for sensing the broad-range and large-number of physical signals of relevance. In this paper we focus on perhaps the first potential platform technology for creating extensive and diverse interfaces to the physical world, namely Large-Area Electronics (LAE).

Below, we describe some attributes of LAE. Though transformational for creating large numbers of distributed, form-fitting sensors and energy harvesters, we note that LAE is inadequate for creating complete systems, which need various additional functionalities. We go on to describe the model of hybrid systems, taking a modular approach, wherein various LAE functionalities are combined with other required system functionalities, implemented using high-performance technologies (namely, Si CMOS). Then, we explore the primary challenge that emerges with hybrid systems, namely interfacing the various functionalities realized by the different technologies. We survey various circuit and architectural solutions that have recently emerged, and also look at algorithmic concepts for enhancing these. Finally, we provide some conclusions.

2. LARGE-AREA ELECTRONICS (LAE)

Large-area electronics (LAE) is a technology based on processing thin-films at low temperatures (<200C, compared to >1000C for Si CMOS). Low-temperature processing enables compatibility with a wide range of materials, providing a basis for diverse transducers for sensing and energy harvesting, as well as their direct fabrication on substrates such as glass, plastic, paper, etc. Further, the associated materials and their processing methods (e.g., deposition of the thin-films) can be achieved over large-area substrates, today reaching over $10m^2$. Figure 1 provides a brief visual survey showing the types of sensors and form factors, i.e., large-area flexible sheets, that have been achieved.

Though low-temperature processing enables compelling attributes for creating sensors, sensing *systems* require the integration of numerous other functionalities (instrumentation, computation, power management, communication). To realize these, circuits based on transistors are needed. Though thin-film transistors (TFTs) are possible, unfortunately, low-temperature processing results in these having orders-of-magnitude lower performance and energy efficiency than typical Si-CMOS transistors. For illustration, Table 1 provides a comparison of key metrics for Si-CMOS transistors and amorphous-silicon (a-Si) TFTs (the current workhorse LAE technology in flat-panel display applications).

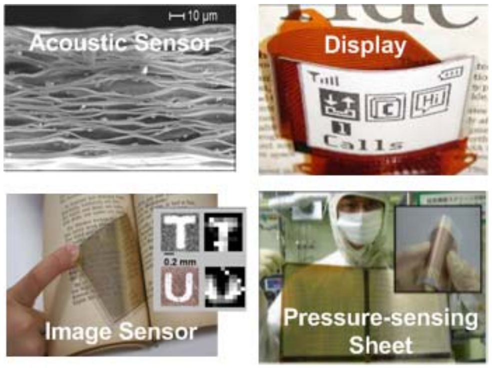

Figure 1. Survey of sensor types and form factors achieved in LAE.

For this reason, there is increasing focus on *hybrid systems* [1], which combine LAE with high-performance technologies (e.g., Si CMOS), in order to realize complete systems. Though the integration of two complementary technologies presents a compelling path forward, and suggests, at least on a high level,

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Table 1. Comparison of Si-CMOS and LAE (thin-film) transistors.

	a-Si TFT	c-Si CMOS (130nm)
Mobility (μ_e/μ_h)	2.0/0.05 cm^2/Vs	1000/500 cm^2/Vs
$t_{dielectric}$	280 nm	2.2 nm
V_{DD}	6 V	1.2 V
$C_{GD}/_{GS}$	3.3 fF/μm	0.34 fF/μm
f_T	1 MHz	150 GHz

how functionality should be distributed, the critical challenge lies in interfacing the technologies. This is especially true as the scale of systems increases. Next, we describe a modular approach to creating hybrid systems, and survey the key interfacing technologies required. As we detail, these will raise the need for selective functions implemented using TFT circuits.

3. MODULAR HYBRID SYSTEMS

The modular approach to hybrid systems presented is derived from experiences experimentally demonstrating several hybrid systems, including the following: (1) a self-powered strain-sensing sheet for structural monitoring via densely-distributed strain gauges [2]; (2) a three-dimensional human-gesture-sensing sheet via large-area capacitance-sensing electrodes [3]; (3) a multi-speaker voice sensing and separation sheet via a large-aperture microphone array [4]; (4) a form-fitting EEG sensing and processing array via distributed thin-film low-noise amplifiers [5]; (5) a large-area image sensing and detection surface via photo-sensors and embedded classifiers [6]; and several others.

3.1 Functionality and Dimension Scalability

Generally, we recognize two ways in which applications are driving system scaling. The first is scaling of functionality and the second is scaling of physical dimensions. In fact, these two are intimately related; specific *functionalities* required within the system are mapped selectively to specific technologies within the hybrid architectures, and the technologies determine the *physical dimensions*. For instance, high-performance functions are delegated to centralized Si-CMOS die; energy-harvesting functions are delegated to LAE over dimensions dictated by power requirements; and sensing functions are delegated to LAE over dimensions dictated by the distribution of information signals.

To address scaling of functionality and dimensions, we focus on the modular, multi-sheet integration approach shown in Figure 2 [7]. This represents a generalization of the hybrid-system concept, where a separation of functionalities is employed not only between Si-CMOS and LAE, but also between various functionalities within LAE when the type and physical dimensions are dissimilar. We note that generally such a separation of functionalities raises interfacing complexities (in terms of energy, performance, assembly). However, given the range of functionalities envisioned in future hybrid systems, such modularity could prove critical from a fabrication perspective and highly preferred from a design perspective. As an example, from a fabrication perspective, even when the materials for two functionalities are the same, their processing may be dissimilar (e.g., a-Si TFTs and a-Si solar cells), or even when the dimensions for two functionalities are the same, their materials and processing may be dissimilar (e.g., a-Si TFT backplanes and organic LED front planes, in flat-panel displays). Thus, a modular, multi-sheet approach presents a path forward for hybrid systems, and yet raises an important focus on the interfacing between sheets.

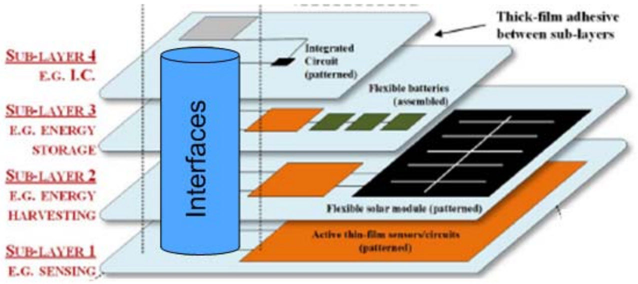
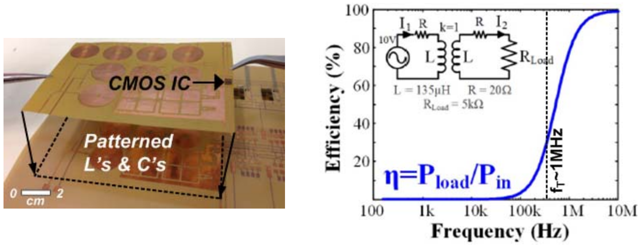


Figure 2. Modular, multi-sheet approach to hybrid systems [7].

3.2 Multi-sheet Assembly

With the multi-sheet approach suggested, a question that arises is how to physically interface the sheets (i.e., mechanically and electrically). Mechanically, lamination methods have proven successful in many-layered bonded-display assemblies, and are believed to scale to larger dimensions, more layers, and broader types of layers (e.g., flexible displays). Electrically, large-area and/or flexible systems today employ metallurgical bonds. However, generally speaking there is no reliable high-volume process for bonding many small Si-CMOS ICs on large, flexible sheets. Today, such ICs are either bonded in small numbers or via discrete flexible connectors, and their assembly typically poses dominating cost and reliability concerns.

In hybrid systems involving a relatively small number of such interfaces at a localized area, metallurgical approaches similar to those used today or those being developed for flexible systems present a path forward. However, hybrid systems where a large number of distributed interfaces are envisioned may need to consider an alternative. One alternative is the use of non-contact interfaces based on planar inductors and capacitors patterned on the sheets [2]. Such an approach is illustrated in Figure 3a. Here small Si-CMOS ICs can be bonded onto a credit-card-sized flexible carrier, for which high-volume processes do exist today (e.g., as in RFID-based smart cards), and mating inductors and capacitors can be patterned on this and the flexible LAE sheet stack. The inductor/capacitor sizes, shown to be large on the order of centimeters, are determined by the coupling requirements between driver and load. Roughly speaking, for capacitors the density achieved is 100pF/cm^2, while for inductors, where there is an important tradeoff with series resistance as described below (i.e., for thin traces enable higher inductance but also high resistance), the inductance-to-resistance ratio achieved is 400nH/Ωcm^2 (with respect to the radius squared). Hence, reducing the number of interfaces remains an important concern for density.



(a) (b)

Figure 3. Non-contact interfaces, where inductive coupling raises a dependence on frequency.

Of course, with non-contact interfaces, a challenge is that signals (for both power and information) must be AC modulated at the transmitter, and potentially demodulated at the receiver. This

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raises the need for specialized architectures, as well as the supporting circuits and devices, as described in the next section. However, within the architectures, important tradeoffs between inductive and capacitive coupling must also be considered. From the perspective of robustness, inductive coupling presents superior tolerance to proximity and alignment variations at the dimensions envisioned. From the perspective of matching driver/load requirements, inductors present the option of voltage/current step up/down. However, from the perspective of power efficiency, inductors suffer from larger loss mechanisms (series resistance) compared to capacitors (parallel resistance). This raises the dependence of power-transfer efficiency on modulation frequency, shown in Figure 3b. For reference, the maximum f_T typically achieved with a-Si TFTs is also shown. This suggests that for inductive coupling, specialized topologies capable of operating near or beyond the TFT f_T are necessary.

4. INTERCONNECTION BACKBONE

With the modular, multi-sheet approach to hybrid systems presented above, interfacing power, information, and control signals becomes a critical aspect. This section explores architectures for such interfacing, by dividing the interfaces into three categories based on signal type: (1) sensor signals; (2) processed-data signals; and (3) power signals.

4.1 Sensor Signals

Sensor signals originate within hybrid systems at LAE sensors. These have the attributes that they can be (1) large in number and distributed (exploiting the ability to create large, expansive arrays of transducers in LAE), and (2) generally sensitive to noise due to small amplitudes. Figure 4 shows key system elements we will consider for interfacing these, namely scanning circuits and active matrices, low-noise-amplifier circuits, and modulator circuits.

Scanning circuits are required because we envision a large number of LAE sensors; however, the low-performance of LAE TFTs prevents signal-processing and -analysis functions that are required over these, necessitating interfaces to Si-CMOS ICs. From discussions in Section 4, the number of such interfaces must be constrained. A noteworthy option is to employ active matrices, which enable sensor accessing through row and column signals, thereby reducing the interfaces by roughly a square-root factor. Indeed, this is done today in flat-panel displays, X-ray imagers, etc. In fact, scanning circuits may be used in conjunction with active matrices. However, generally, for the sensing applications envisioned one aspect that could limit the use of active matrices is that the optimal choice of sensor placement will be determined by the distribution of information signals, which may not be regular, as in the case of dense displays and imagers. In this case, row-/column-accessing signals will present unsuitable routing complexities. Though scanning circuits can be more amenable to irregular sensor placements, they present significant challenges also. Most notably, time multiplexing of a large number of signals for maximal scalability raises sampling rate constraints, which may be too severe for Nyquist acquisition, considering the bandwidth of information signals. As an example, typical scanning speeds are in the range of 1-10kHz, due to the limited performance of TFTs [8]. Later in this paper we will mention how algorithmic methods may overcome this.

Low-noise amplifiers are required because generally LAE sensors will be distributed but Si-CMOS ICs will be centralized. This raises the need for long interconnects on the sensing sheet, which will be susceptible to coupling of stray noise sources. The challenge with embedding low-noise TFT amplifiers near the distributed sensors is that, generally, these will have significantly lower power efficiency (transconductance efficiency) and higher noise than Si-CMOS amplifiers [5]. Specifically, the higher noise comes about due to $1/f$ noise sources originating from the increased density of carrier traps in the semiconductor and semiconductor-dielectric interface of TFTs. For illustration, Figure 5 compares cases within a voice sensing-and-localization system based on piezoelectric-film microphones [4], analyzing the total noise with and without a TFT amplifier, as stray coupling noise is increased. As seen, for low levels of coupling noise, the total noise referred to the microphone is worse due to the TFT amplifier; however, as coupling noise increases beyond a level of 150mV$_{RMS}$, the TFT amplifier becomes preferable. Recently, the possibility of employing circuit techniques, such as chopper stabilization [5], to reduce the $1/f$ noise of TFT amplifiers has been explored. While this comes at the cost of power efficiency, analysis and experimental validation show that significant reduction of $1/f$ noise is possible and viable, making distributed low-noise amplifiers a promising component in hybrid systems.

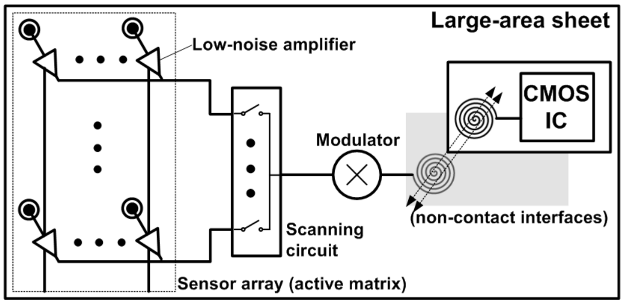

Figure 4. Interfacing sensor signals in hybrid systems.

Modulator circuits are required if non-contact interfaces are employed for transmitting sensor signals to another sheet. TFT circuits based on Gilbert-multipliers have been used successfully and are readily implemented [2]. These combine with scanning circuits for multi-sensor accessing, and typically employ capacitive interfacing due to the limited speed of TFT-based Gilbert modulators. Further, the modulation signal from a Si-CMOS IC can also be provided through capacitive interfacing. This enables readout by the IC in a synchronous manner (i.e,, using the same signal for modulation and demodulation), leading to simplified topologies [2].

4.2 Processed Data Signals

Processed data signals arise in hybrid systems in the following scenarios, summarized in Figure 6: (1) to communicate information/control signals between Si-CMOS ICs and the LAE domain for control and synchronization functions (sensor instrumentation already having been addressed in Section 4.1); (2) to communicate information/control signals between distributed Si-CMOS ICs, for instance for data aggregation; and (3) to communicate information/control signals between a multi-sheet

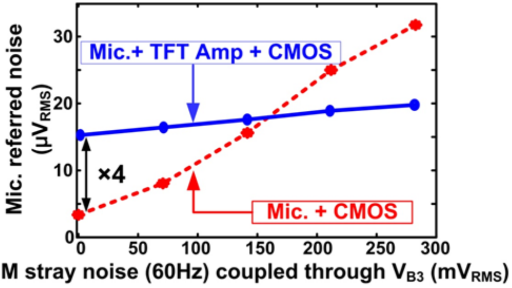

Figure 5. Analysis of noise in microphone acquisition system [4].

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hybrid system and remote systems. We explore specific cases and architectures for each scenario below.

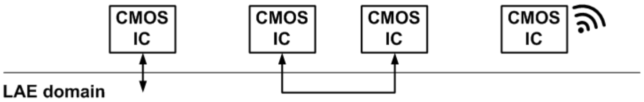


Figure 6. Interfacing processed data signals in hybrid systems.

One example of communication between the Si-CMOS domain and the LAE domain mentioned previously is the CMOS-derived modulation signal feeding a Gilbert-cell for non-contact sensor-data coupling. Another example alluded to is the control of scanning circuits. This case highlights a common challenge for voltage signals, which is that the voltage levels in the Si-CMOS domain are typically much lower than those in the LAE domain. LAE TFTs require large voltages for adequate drive current, due to the lower mobilities and lower gate-channel coupling (because of reduced gate-dielectric scalability). Hence, signals from the LAE domain to the Si-CMOS domain are easily transmitted, for instance with voltage step-down via capacitive coupling. For signals from the Si-CMOS domain to the LAE domain, where voltage step up is required, two options can be considered. First, if a high-level power supply is available in the LAE domain, explicit TFT level converters can be employed, as in [8]. However, in systems where there is no such power supply, voltage step-up can also be achieved via inductive coupling [2]. As before, this necessitates AC modulation at the transmitter, which is easily achieved in Si-CMOS ICs at frequencies where inductive losses can be tolerable. To maximize the voltage swing, operating the inductive interface at resonance is highly preferred. High resonant frequencies to also minimize inductor losses require minimizing the tank capacitance, which may for instance be formed by LAE thin-film diodes for demodulating the control signals [2]. Hence the design of such diodes, as in [9], where current density is maximized and forward voltage-drop is minimized is crucial. Even after these optimizations, the power loss in an inductive interface is quadratic with inductor resistance, since this can be represented as a parallel resistor at resonance. Further, since voltage step-up is achieved by increasing the turns ratio, for a given inductor size, the traces must be thinner, causing the resistance itself to increase roughly linearly. As a result, the overall power loss for a given inductor size is roughly cubic with the desired voltage step-up [2].

Communication between distributed Si-CMOS ICs can exploit LAE for long-range interconnects, avoiding the need for more energy-intensive wireless communication. With metallurgical connections, LAE interconnects can be driven directly with data at baseband, incurring the energy of capacitive switching (e.g., CV^2). With non-contact interfaces, AC-modulation of the communication data is required to robustly drive the interconnects (though schemes for driving data at baseband have also been explored [10]). Inductive interfaces again benefit from modulation at the resonant frequency of the interconnect network, determined by the inductance as well as the coupled and self-capacitance. Since these parameters are often difficult to know a priori, topologies that self-calibrate to the resonant frequency have been proposed [2]. As before, inductive coupling also offers the benefit of selective voltage step-up/-down. For instance, voltage step-down can be employed at the transmitter, in order to reduce the voltage amplitude and thus the power loss incurred due to the resistance of the long interconnects (which appears as a parallel resistance a resonance); while, voltage step-up can be employed at the receiver to maximize the receive SNR [2].

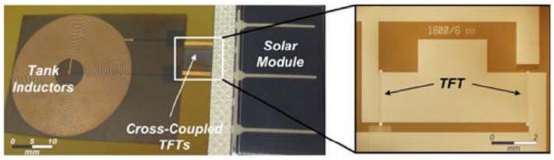
Finally, for communication between a multi-sheet hybrid system and remote systems, wireless transceivers are necessary. For these, LAE offers the benefit of large antennas, which lead to improved radiation efficiency. For the transceiver circuits themselves, where distributed functionality is typically not required, Si-CMOS implementations are preferred due to the higher performance and energy efficiency of transistors. We point out that TFT-implemented transceivers have been explored to create distributed arrays of frontends for wireless communication [11]. While experimental demonstrations show that despite low TFT performance, 10's of meters range is possible by taking advantage of the large antenna achievable in LAE, the energy-efficiency is lower than Si-CMOS-implemented transceivers.

4.3 Power Signals

Transmission of power signals across multiple sheets is an important aspect in hybrid systems, especially if energy-harvesting capabilities of LAE are to be exploited. Given that ambient power signals can be distributed in many applications, several discrete, distributed energy harvesters may be needed. While this could correspondingly raise the need for discrete interfaces to other sheets, the numbers are likely to be small. Unlike information signals from sensors, there is typically not a need to maintain separation of the power signals from discrete sources and susceptibility to noise is not as critical. Thus power from distributed sources can be combined into a small number of interfaces for transmission. This makes metallurgical bonding for power interfaces somewhat more viable.

However, for systems requiring substantial scalability, for instance by incorporating many, possibly distributed, Si-CMOS ICs, the need for a large number of power interfaces to each IC can arise [2]. Here, non-contact interfaces, avoiding metallurgical bonds, may once again be preferred. As usual, AC signal will be required for coupling. Given that many LAE harvesters output DC power (e.g., solar cells, thermo-electrics), power converters (inverters) must then also be implemented. Significant power transfer then becomes challenging due to the low current-handling capabilities of TFTs. For instance, topologies such as switching converters are used extensively in Si-CMOS and other high-performance technologies because of their high power-conversion efficiencies and large output currents; however, these are not suited for TFT-implementation due to the low currents of TFT switches and the typical lack of complimentary (NMOS/PMOS) transistors required for efficient switch control [12].

An alternate topology, which has proved to be much more suitable for LAE implementation is a free-running LC power oscillator [13], such as that depicted in Figure 7. Because this circuit requires no control circuitry, its power-transfer efficiency can be near theoretical-maximum levels, even with TFT implementation. The reason for this is that resonant operation depends strongly on the quality of inductors, which can be high in LAE, thanks to the ability to pattern physically-large planar coils (i.e., many turns for high inductance and thick traces for low resistance). Further, the use of inductors enables power transfer via inductive coupling, and the ability to resonate with the TFT capacitances allows for frequencies well beyond the TFT f_T (instead limited by f_{MAX}, which can be much larger for TFTs) [14]. Inductive coupling has the advantage that the low currents but high voltages of TFTs can be converted to high currents at the voltage levels of Si-CMOS ICs through the turns ratio, thereby enabling significant power transfer, for fully-self-powered systems [2].



V_{OP} (V)	Solar Modules (cm^2)	W/L of TFTs	f_{OSC} (MHz)	P_{OSC} (mW)	P_{LOAD} (mW)	η (%)
25	300	3600μm / 6μm	2.1	73	22.6	31

Figure 7. TFT-based LC-oscillator power inverter [13].

5. ALGORITHMS FOR INTERFACING

The primary focus of this paper has been on the platform methodologies and components required for interfacing multi-sheet hybrid systems. While several device, circuit, and architectural solutions have been presented, offering a range of tradeoffs, we generally see that interfacing poses a fundamental concern in the approach of hybrid systems. Further, the problem is most pronounced for interfacing sensor signals, because most importantly we would like to exploit the ability of LAE to create large numbers of distributed sensors and the ability of Si-CMOS to perform processing and analysis over the signals. In this section, we briefly point to algorithmic concepts that have recently emerged, possibly offering the potential to dramatically reduce the number of interfaces between LAE sensors and Si-CMOS ICs.

Specifically, the algorithmic approaches are driven by the recognition that over very large numbers of sensors, individual instances of data are likely to not be of high importance. Rather, higher-level features or information over aggregated sets of sensors are most likely to be of greatest value. This points to methods from the domains of machine-learning and statistical signal processing for creating representations of the sensor data that reduce the interfacing requirements. Two examples are described below.

5.1 TFT-based Classification

In [15], an approach for reducing the data from a large number of sensors to a small number of inference decisions is presented. The approach relies on a machine-learning algorithm knows as Error-Adaptive Classifier Boosting (EACB). EACB itself is an extension of another machine-learning algorithm knows as Adaptive Boosting (AdaBoost). In AdaBoost, a strong classifier, able to fit to arbitrary data distributions, is formed from multiple weak classifiers, unable to fit arbitrary data distributions. Training of the weak classifiers is performed iteratively, at each step biasing the training set to emphasize instances affected by fitting errors. EACB, extends this by biasing the training set not only based on fitting errors, but also based on errors due to non-ideal implementation of the weak classifiers. In this way, errors due to the large TFT variations typically encountered are overcome through data-driven training. The weak classifier decisions are then provided to the Si-CMOS domain for making strong classifier decisions. Figure 8 shows the architecture of the system. TFT-based linear classifiers are formed using a pseudo differential, two-transistor stack, appropriately biased, to provide an approximation to multiplication between a sensor input and a weight derived from training (then stored via non-volatile charge trapping in the bottom TFT). On the right, the representative performance is shown for detecting 'L' shaped images (from a set containing five different shapes) from LAE photo-sensors over multiple EACB iterations.

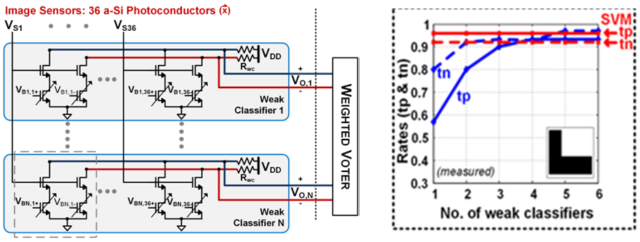


Figure 8. TFT-based weak classifiers used with EACB to achieve performance [true-positive (tp) and true-negative (tn) rates] near a MATLAB-implemented support-vector-machine (SVM) classifier[15].

5.2 TFT-based Compression

In [5], a system is presented for acquiring EEG data from an array of flexible electrodes. For providing the data to a Si-CMOS IC for further processing, it is preferable to multiplex signals from all the electrodes to a single interface, in order to address assembly complexity and robustness. However, TFT-based scanning circuits are limited to a frequency of ~10kHz [7]; with each EEG channel having a bandwidth of ~2kHz after practical filtering, the number of channels that can be support is very small, considering Nyquist-sampling requirements. Instead, the system exploits compressive sensing, using analog modulation via TFT circuits to acquire pseudo-random measurements over an epoch of data. Given that EEG exhibits sparsity in a Gabor basis, sparse reconstruction can be used to recover estimates of the original signals. However, the system in [5] also explores the extraction of spectral-energy features, which are a widely employed biomarker in EEG, directly from the compressed samples. This is done via linear estimation of the original signal followed by linear filtering. Experimental results show that the error from linear estimation is substantially tolerable when the features are subsequently employed for classification, such as detection of epileptic seizures. Specifically, seizure-detection performance is maintained out to compression rates in excess of 60×.

6. CONCLUSIONS

This paper focused on the approach of hybrid systems. Hybrid systems combine LAE, which can serve as a platform technology for sensing, with high-performance technologies such as Si-CMOS, which can severe as a platform technology for other functionalities required within a system (instrumentation, computation, power management, communication). Though hybrid systems thus provide a path to implement complete systems, they face the challenge of interfacing signals between the technology domains. This paper examined the challenges and possible solutions for interface three categories of signals: (1) sensor signals; (2) processed data signals; and (3) power signals. In all cases, circuits and subsystem architectures capable of addressing the interfacing needs at scale were explored, with respect to the various tradeoffs they face. Looking beyond the circuit and architectures, algorithmic concepts for easing the interfacing requirements (especially for sensor signals) were examined. Experimental demonstrations show that the various interfacing strategies are promising for a broad range of hybrid systems, raising the possibility for such systems to address a range of compelling new applications.

7. ACKNOWLEDGMENTS

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