High-Speed Scanning Circuit Based on Metal-Oxide Thin-Film-Transistors for Reduction of Large-Area to CMOS IC Connections

Y. Mehlman, Y. Afsar, T. Moy, S. Wagner, J. C. Sturm, and N. Verma
Department of Electrical Engineering, Princeton University, Princeton, NJ, 08544, USA
email: jmehlman@princeton.edu

Hybrid Large-Area Electronics (LAE) provides a powerful platform for complete sensing systems, in which large numbers of flexible thin-film sensors can be patterned over a large area, and most computation performed through embedded integrated circuits (ICs). Active thin-film electronics utilizing thin-film transistors (TFTs) are usually necessary for a number of interfacing functions [1], including multiplexing sensor channels to reduce the number of interfaces made with ICs. Through multiplexing, a large number of sensors can be read out through a single interface. To enable this reduction of interfaces, a novel design for a low-power TFT-based "scanner" circuit was previously demonstrated in a-Si technology, but was greatly limited in speed by TFT properties [2]. In this paper we experimentally show how the scan rate of the circuit can be improved by 30x at a fixed energy budget through implementation with ZnO TFT technology.

Given N sensors, each accessed through a switch controlled by a corresponding scan element of a "scan chain," only a single LAE/IC interface is needed for readout, as well as 3 global control signals (Fig. 1). As N increases, the power consumption of the chain remains nearly constant; with the exception of the enabled element, all others consume only sub-threshold leakage power. However, the effective sampling frequency for one sensor (scan rate/N) decreases as N increases. Accordingly, the signal bandwidth of the sensors is limited. Thus, it is desirable to increase the scan rate (# sensors accessed per second) so N can be kept large, while sharing one interface.

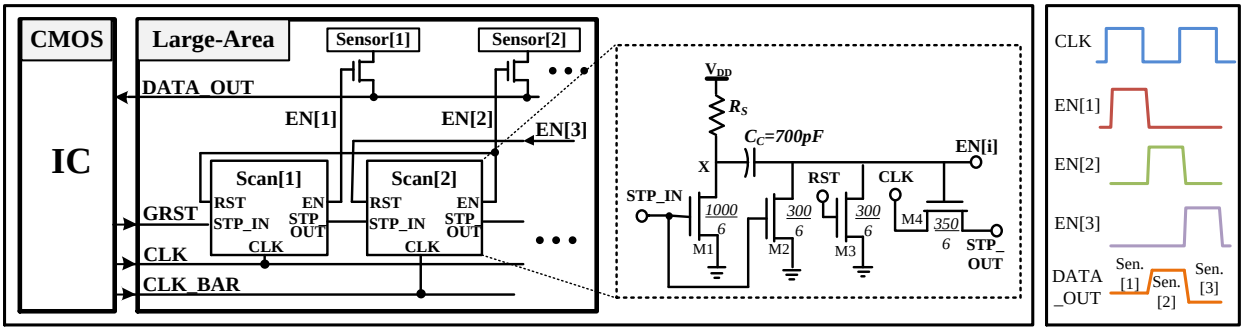
Each element of the scan chain sequentially outputs a high enable signal (EN) to activate a corresponding sensor, coordinated by a two-phase clock (CLK, CLK_BAR) fed in from an IC. When EN[i-1] is high, STP_OUT[i-1] (set by a clock signal) pulls nodes X[i] and EN[i] low through transistors M1 and M2. Subsequently, when the clock transitions, X[i] rises, bringing EN[i] high by capacitive coupling through C_C. Later, when EN[i+1] rises, EN[i] is reset (grounded) through M3 by charging C_C . All transistors are then turned off to avoid high DC power consumption, and EN[i] is robustly kept at ground through TFT leakage. To ensure sufficient swing on EN[i], two conditions must be met: (1) $R_s \gg R_{1,on}$ and (2) $C_c \gg C_{load}$, where $R_{1,\mathrm{on}}$ is the on resistance of M1 and C_{load} is the capacitance seen by EN. The scan rate is limited by the large time constant, $R_s C_c$, associated with the reset transition. The energy per element is independent of R_s and is proportional to $C_c V_{DD}^2$. Therefore, by increasing the speed of the transistors, R_s can be reduced, increasing the scan rate without sacrificing energy.

A 1 kHz a-Si scan chain was demonstrated in [2]. We present a scan chain fabricated with ZnO-channel TFTs on glass (technologies are compared in Fig. 2). The channel and oxide for a-Si TFTs are deposited by PECVD at 250°C and by PEALD at 200°C for ZnO TFTs. Due to the thin gate oxide in ZnO TFTs, V_{DD} must be kept below 12V to prevent breakdown, whereas a-Si TFTs can handle up to 30V. Measured output waveforms of a ZnO scan chain for V_{DD} = 6V are shown in Figure 3, highlighting good uniformity, sharp transitions, and 80% V_{DD} swing, despite the lack of p-channel transistors. Through improved mobility and sub-threshold slope, ZnO TFTs achieve a 30x increase in scan rate compared to a-Si technology at a given energy budget. While C_{ox}/area is larger for ZnO technology, TFT width can be proportionately downscaled without sacrificing drive given a technology-independent load (see Fig. 1). Therefore, C_c and, by extension, energy per sensor remain constant across technologies.

Figure 4 compares the scan rate for a-Si and ZnO technologies, as it varies by V_{DD}. Data for a-Si was simulated using Spectre. Both measured and simulated results for ZnO are shown, and are typically in close agreement, until low V_{DD}, where variation in turn-on-voltage begins to have a large effect. Ultimately, a ZnO scan chain can be operated at lower V_{DD}, saving energy, with a still higher scan rate for enabling aggressive reduction of LAE/IC interfaces for higher bandwidth signals.

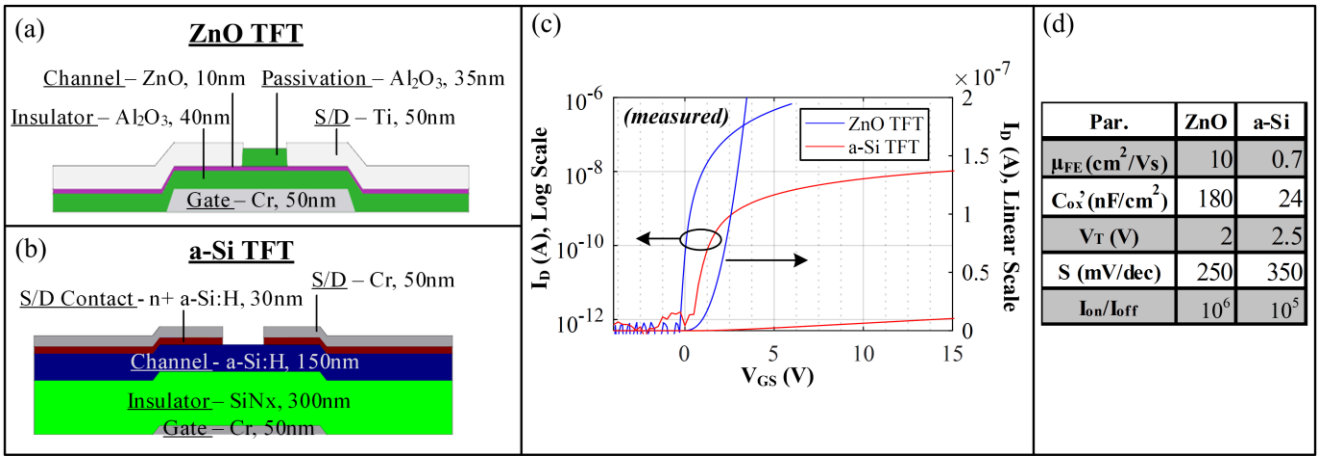
[1] N. Verma et al., "Enabling Scalable Hybrid Systems: Architectures for Exploiting Large-Area Electronics in Applications," *Proc. of IEEE*, vol. 103, no. 4, pp. 690-712, April 2015.
[2] T. Moy etal., "Thin-film Circuits for Scalable Interfacing Between Large-Area Electronics and CMOS ICs," in *Proc. of the Device Research Conference*, June 2014.

This work was supported in part by the Princeton Program in Plasma Science and Technology and FlexTech.



(a) (b)

Figure 1. (a) Block diagram and circuit diagram of the scan circuit. Three global control signals (CLK, CLK_BAR, GRST) are generated by the IC and transmitted to the scanning circuit. Each scan element has four transistors (M1-M4), one coupling capacitor (C_c) and a pull up resistor (R_s). W/L (in microns) is indicated beside each transistor for the ZnO implementation. R_s is re-optimized at each V_{DD}. (Adapted from [2].) (b) Representation of clock, enable, and sensor readout waveforms.



Par.	ZnO	a-Si
μ_{FE} (cm^2/Vs)	10	0.7
C_{ox}' (nF/cm^2)	180	24
V_T (V)	2	2.5
S (mV/dec)	250	350
I_{on}/I_{off}	10^6	10^5

Figure 2. (a), (b) Cross sections of ZnO and a-Si TFTs used in this study. (c) Transfer curves for typical ZnO and a-Si channel transistors plotted on both log (left) and linear (right) scales, measured at V_{DS}=0.1V. Drain current is normalized to W/L =1. Gate leakage is below 1 pA for W/L = 10 for both technologies. (d) Key properties for both technologies. The ZnO transistor is about 200x more conductive due to the increase in mobility and C_{ox}', and decrease in V_T.

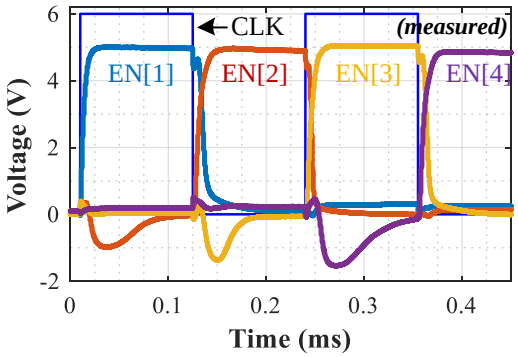


Figure 3. Measured waveforms of first four enable signals of a ZnO-based scan chain fabricated on glass. Shown for V_{DD}=6V and a 35pF external load.

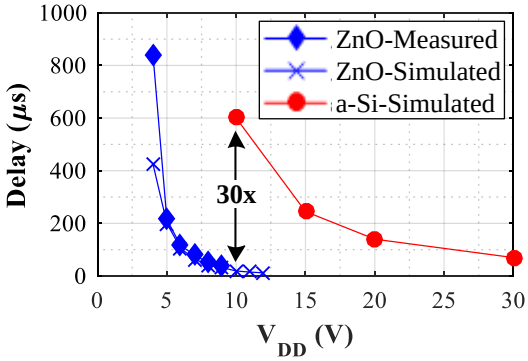


Figure 4. Delay vs. V_{DD} for ZnO and a-Si scan chains, given a 35pF external load, showing impact of μ_{FE} scaling and improved sub-threshold slope. At V_{DD}=10V, ZnO scan chain operates 30x faster than a-Si scan chain.

Research was sponsored by the Army Research Laboratory and was accomplished under Assistance Transaction Agreement Number W911NF-10-3-0001. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Laboratory or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.