Information-Processing-Driven Interfaces in Hybrid Large-Area Electronics Systems

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***Abstract*—In the development of human-centric systems, access to a large number of human information signals is required. Such signals can be acquired from both ambient and on-person (wearable) sensors. Large-area electronics (LAE) provide distinct capabilities for creating the required diverse, distributed and conformal sensors. However, the large volume of and complex correlation to target information within the captured data requires significant processing and inference. This makes an LAE-CMOS hybrid system well-suited to such applications. Interfacing between the two technologies is a challenge in hybrid system design. We demonstrate an emerging solution space based on information-processing-oriented interfaces, through two case studies: 1) an image sensing and compression system based on random projection [1]; 2) an electroencephalogram (EEG) acquisition and biomarker-extraction system using compressive-sensing circuits [2].**

Keywords— Large-area electronics (LAE), hybrid systems, thin-film sensors, thin-film transistors (TFTs).

I. Introduction

In recent years, there has been significant progress in the development of wearable technology, driven by applications ranging from medical and wellness, to augmented/virtual reality (A/VR), to advanced human-computer interfaces (HCIs). While the applications span across many different areas, their core objective remains the same: to generate a rich user experience derived from a deep understanding of human intention/function. To develop such a knowledge, these human-centric systems require access to large amounts of contextual information. Thus, the design of such systems is heavily influenced by the ability to sense the wide-range of relevant human signals.

Indicators of human intention/function can be separated into two classes: 1) ambient signals (e.g. image, pressure), captured by external sensors that are often distributed across the physically-large area over which humans act, and 2) on-person signals (e.g. EEG, EMG), measurable via wearable sensors. To capture the maximal information, a potentially larger number of these sensors must be easily integrated into our everyday lives in non-obtrusive ways. For wearable sensors, this often means a light, conformal form factor. Moreover, as applications become increasingly complex, systems will require information from multiple indicators, often across both classes. For example, [3] uses a combination of both ambient and wearable sensors to accurately monitor the activity of daily living (ADL) of elderly people to assess their ability to live independently. Thus, in order to realize these human signal-driven systems, a platform technology capable of creating diverse, spatially-distributed, and/or conformal sensors is necessary.

Based on low-temperature processing of thin films, large-area electronics (LAE) is compatible with a variety of materials, enabling the fabrication of a diverse range of sensors [4]-[6], across a variety of substrates (e.g. plastic, glass). This makes LAE suitable for creating sensors for capturing human signals. However, since the sensor data is both high-dimensional and has a complex correlation to human intention/function, significant data processing is also required. While it is possible to create active devices in LAE (i.e. thin-film transistors (TFTs)), these have low performance and high variability. This makes them impractical for computation and processing, especially at the scale of sensing possible in LAE. Instead, CMOS transistors are much better suited to perform these complex functions. Thus, a compelling platform for these applications is LAE-CMOS hybrid systems, which leverage the sensing diversity of LAE and the computational power of Si-CMOS devices [7].

A key challenge in realizing these systems lies in scalability of the interfacing between these two technologies. For instance, we require a means to transfer the large volume of LAE sensor data to the CMOS domain across a minimal number of interfaces. We have previously demonstrated hybrid systems that use circuit-based solutions (i.e. multiplexing via scan circuits) [8],[9] to significantly reduce the number of LAE-CMOS interfaces. Though useful, we are increasingly finding that solutions which also incorporate algorithmic approaches centered around the information processing of interest hold much greater promise [1], and in certain cases, can overcome the fundamental limitations of circuit-based approaches alone [2],[10]. Thus, in this paper, we focus on information-processing-oriented interfacing solutions. Unlike [11], which broadly analyzes algorithmic techniques, this implies a directed focus on signal-inference from high-dimensional data.

II. Information-Processing-Driven Interfaces

In many applications, the raw data from individual sensors is less relevant than the higher-level information that can be

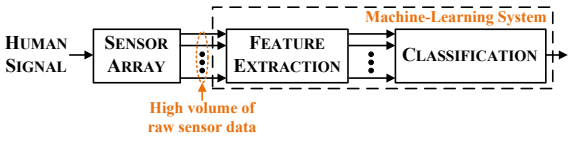

Fig. 1. Architecture of a conventional classification system.

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derived across multiple sensors. Thus, we are interested in techniques which exploit the transformation of data to information, and then interface that information, rather than raw data, from LAE to CMOS. In many cases, the data correlate with human intention/function in complex ways, and cannot be analytically modeled, let alone computed in LAE. However, the correlations can be derived from data via machine-learning methods for classification.

The objective of a classification system is to identify which class, or category, an instance of data, or observation, belongs to. As shown in Fig. 1, these systems typically consists of two stages: 1) feature extraction and 2) classification. The purpose of feature extraction is to transform the raw data to enhance pattern recognition (i.e. improve class-wise separation of data). The classification stage first involves learning a model for class-wise separation, and then applies this model to make decisions on incoming data. Thus, by using a classification system, the high volume of raw sensor data is now reduced to inferences.

Ideally, we would like to build these classification systems in the LAE domain. However, both feature extraction and classification can be computational intensive, making them challenging to implement using LAE devices. In fact, we begin to see a tradeoff emerge: an increase in the computational functions performed in the LAE domain tends to greatly limit the feasibility of the system on a functional level, but on the other hand significantly enhances interface scalability of the system on a physical-design and -assembly level. In trying to strike a balance, we have explored drawing the line at each of the stages, demonstrating hybrid systems that perform LAE-based feature extraction [1],[2] and LAE-based classification [6]. A general insight we derive is that data is increasingly reduced through the feature-extraction and classification stages. While this is beneficial for minimizing interfaces, it also restricts the leverage possible through subsequent CMOS processing for performance enhancement, following intentionally-relaxed LAE processing. The case studies specifically illustrate the value of maintaining this leverage.

As previously mentioned, feature extraction aims to enhance class-wise separation. This is usually accomplished through dimensionality reduction and/or computation of specific features that are indicators of the inference of interest (e.g. biomarkers in medical applications). Drawing on concepts from statistical signal processing, we find that it is feasible to perform dimensionality reduction in the LAE domain. We have demonstrated two systems which perform feature extraction via different methods. The first is an image sensing and detection system, employing random-projection based compression that preserves the information required for subsequent classification [1]. The second is an electroencephalogram (EEG) acquisition and seizure detection system, which performs compression via TFT-based circuits, deferring biomarker computation, on already-compressed EEG data, to the CMOS domain [2]. In the following sections, we present these two systems as case studies.

III. Image Sensing and Detection System Using Random Projection-Based Compression

A commonly used circuit-based interfacing solution is active-matrix addressing, in which sensors are accessed row/column-by-row/column. This results in an approximately square-root reduction in the number of interfaces. While significant, the number of interfaces still scales prominently with the number of sensors. In [1], we present a system which reduces this number far beyond the level achieved with just an active matrix, by incorporating a TFT-based compression matrix based on random projection.

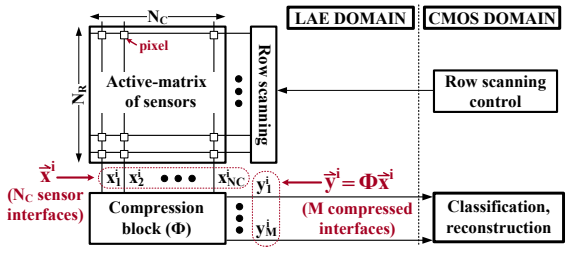

Fig. 2. Architecture for random projection-based compression system [1].

A. System Overview

Fig. 2 shows the system architecture. As mentioned above, an active matrix can access an array of $N_R \times N_C$ sensors with just $\sim N_C$ (plus a few control signals for row scanning) interfaces. This N_C-interface signal $\vec{x}^i$ is then fed into (i.e. is multiplied with) a TFT-based compression block Φ with dimensions $M \times N_C$ (where $M < N_C$), resulting in a compressed M-interface signal, $\vec{y}^i$ (i.e. $\vec{y}^i = \Phi\vec{x}^i$), and a compression rate N_C/M. While performing compression in this way means that it is difficult to reconstruct $\vec{y}^i$, with the correct selection of Φ, the inner product between two compressed output vectors $\vec{y}^j, \vec{y}^k$ statistically preserves the inner product between the two corresponding uncompressed vectors $\vec{x}^j, \vec{x}^k$. This is important because inner products are used as the similarity metric in many classification algorithms, including support-vector machines (SVMs). Thus, with an appropriate Φ, classification can be performed directly on the transmitted compressed signal in the CMOS domain [12] (and, in some cases $\vec{y}^i$ can also be reconstructed [1]). In a typical active-matrix array, the frame rate, determined by the time to scan all rows, is an important parameter of performance and is limited by the time required to drive the row-gate and column-data lines through an access TFT. The compression block should add minimal additional delay, as discussed below.

B. Random Projection and Inner-Product Preservation

As mentioned above, Φ must be chosen carefully to ensure statistical inner-product preservation. This includes matrices which are drawn from a zero-mean random variable. One such easily-implemented Φ, contains elements drawn from a zero-mean Bernoulli random variable (i.e. ±1 with probability = ½) [12]. This is beneficial for an LAE-based implementation, since with a Φ that contains only ±1, compression is now reduced to simple add/subtract operations over $\vec{x}^i$.

$$\vec{y}^{jT}\vec{y}^{k} = (\Phi\vec{x}^{j})^{T}\Phi\vec{x}^{k} = \vec{x}^{jT}\underline{\Phi^{T}\Phi}\,\vec{x}^{k} \approx \mathbf{M}(\vec{x}^{jT}\vec{x}^{k})$$

$$\Phi^{T}\Phi = \begin{bmatrix}\varphi_1\\ \varphi_2\\ \vdots\\ \varphi_{NC}\end{bmatrix}_{M} \times \begin{bmatrix}\varphi_1 & \varphi_2 \cdots & \varphi_{NC}\end{bmatrix}_{N_C} = \begin{bmatrix}\varphi_1\varphi_1 & \varphi_1\varphi_2 \cdots\\ \varphi_2\varphi_1 & \varphi_2\varphi_2 \\ \vdots & \ddots\end{bmatrix}_{N_C \times N_C}, \quad \varphi_p\varphi_q = \begin{cases}\sim 0 & (p \neq q)\\ \mathbf{M} & (p = q)\end{cases}$$

$$\approx \mathbf{M}(\mathbf{I}_{NC})$$

Fig. 3. Inner-product preservation after compression with Φ [1].

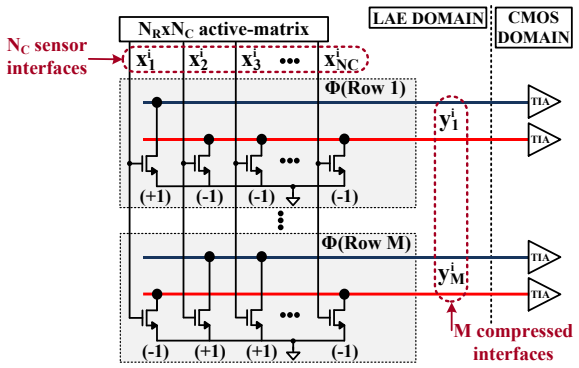

Fig. 4. TFT-based implementation of Φ [1].

Fig. 3 illustrates how preservation of inner products occurs even after compression with Φ. For sufficiently large values of M (Φ has dimensions M×N_C), $\Phi^T\Phi$ approaches a scaled version of the identity matrix (i.e. MI_{NC}), whose off-diagonal entries are ~0 with variance scaling with 1/M.

C. LAE-Based Implementation of Φ

Fig. 4 shows the TFT-based implementation of Φ, where each TFT corresponds to an element of Φ. Thus, for each of the M rows of Φ, the N_C sensor outputs ($x^i_1 \ldots x^i_{NC}$) feed the gates of N_C TFTs, converting the sensor voltage output into a current as determined by the TFT transconductance. As mentioned above, compression only involves add/subtract operations, determined by the ±1 elements of Φ. To implement this, the TFT currents are combined into differential outputs formed by two summing nodes per row: one for +1 elements and one for -1 elements, resulting in the outputs $y^i_1 \ldots y^i_M$. To maintain a fixed drain-source voltage across the TFTs, the summing nodes connect to the virtual ground of transimpedance amplifiers (TIAs) (implemented in CMOS). This virtual-ground condition also greatly mitigates the circuit's delay, which is caused by TFTs driving their self-capacitance (and wiring capacitance) on the output nodes. With this implementation, at the achieved levels of compression, the number of additional TFTs in the compression block (M×N_C) is small with respect to the number used for the active matrix (minimally N_R×N_C).

D. System Demonstration

A system prototype is formed by integrating an a-Si TFT compression matrix with an array of a-Si photoconductors [6] representing an 80×80 active matrix. To demonstrate the system, image classification (and reconstruction) is performed on 1500 images from the MNIST database of handwritten-digits [13]. One-versus-all classification is performed for each digit using an SVM with a radial-basis-function kernel. High levels of classification performance are achieved, even at large compression factors (i.e. at 20× compression, true-positive/true-negative/error rates are 90%/93%/7%).

IV. EEG Acquisition and Seizure Detection System using Compressive-Sensing Circuits

In the system described above, handwritten digit recognition can be performed directly on the compressed data. However, for seizure detection, feature extraction requires both dimensionality reduction on and computation of biomarkers (i.e. spectral energies) from the EEGs. We now discuss a system with interfaces incorporating compressive-sensing algorithms with scanning circuits to perform LAE-based compression, after which biomarker extraction can be performed directly on the compressed data in the CMOS domain [2].

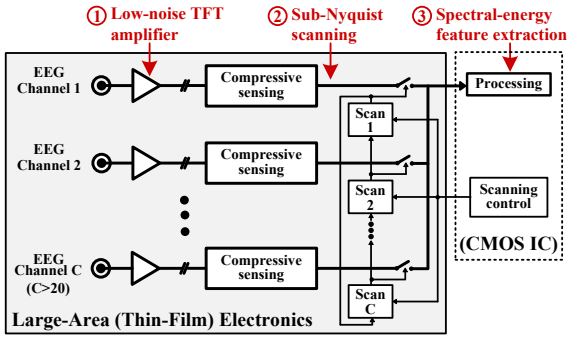

Fig. 5. Architecture of EEG acquisition and seizure detection system [2].

A. System Overview

By means of a flexible-form factor, this system aims to overcome many of the limitations of conventional EEG acquisition methods (i.e. electrode setup, motion artifacts, patient discomfort). Such an approach raises its own challenges, specifically in the case of transferring EEG data to the CMOS domain with minimal degradation by stray noise and minimal number of interfaces. Shown in Fig. 5, the system is designed to address these challenges through three main stages: 1) low-noise thin-film amplifiers, 2) compressive multiplexing circuitry and 3) CMOS-domain spectral-energy extraction. The amplifier of stage 1 mitigates the effects of stray noise degrading the low-amplitude EEG signal. A chopper-stabilized topology is used to overcome the 1/f-noise limitations typically faced by EEG amplifiers. Stages 2 and 3 are implemented to achieve minimal interfacing of LAE and CMOS. First, a conventional scan circuit [14] is used to multiplex all EEG signals onto a single interface. However, maximum scanning speeds are ~10kHz and EEG signals have a bandwidth ~2kHz (after filtering). Using Nyquist sampling, this limits the system ~5 channels. This is significant, as typical EEG systems consist of >20 electrode channels. The system overcomes this by incorporating an algorithmic approach based on compressive sensing. The compressed signals are then passed to the CMOS domain via a single interface, where biomarkers are extracted (in the second step of feature extraction) without the need for full reconstruction.

B. Compressed Spectral-Energy Extraction

Compressive sensing allows us to perform sub-Nyquist sampling by exploiting the fact that EEG can be sparsely represented in the Gabor basis. More specifically, it is possible to sample at a rate related to the number of non-zero coefficients (i.e. very few) in this sparsity basis, Ψ. Moreover, there is no need to transform the signal into its sparse representation. Instead, a compressed output, $\hat{x}$, of just a few measurements, M, can be derived from linear combinations of the N-length EEG signal samples, $\vec{x}$. This corresponds to multiplication of $\vec{x}$ by an M×N measurement matrix Φ. The only condition is that ΦΨ satisfies the Restricted Isometry Property (RIP) [15]. An analog

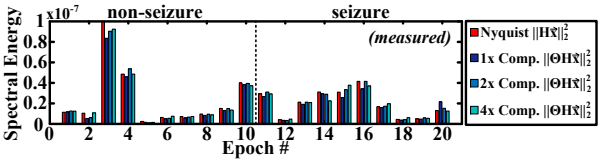

Fig. 6. Comparison of 20 derived estimates at different compressions [2].

TFT implementation based on [16] is used in the system, which takes pseudo-random compressed measurements.

The compressed outputs $\hat{x}$ are transferred to the CMOS domain for biomarker (i.e. spectral-energy) extraction. This typically involves feeding an epoch of EEG data into a band-pass filter $\boldsymbol{H}$, after which the output is used to derive the energy. Since $\boldsymbol{H}$ is only known for application to time-domain signals, reconstruction of the original signal is needed. While compressive sensing states that it is possible to reconstruct the original signal via sparse reconstruction based on l1-norm minimization [15] (and this is demonstrated in [2]), such reconstruction can be computationally intensive. Instead, focusing on estimating energy-based features, which correspond to taking an inner product of the time-domain vector with itself, we avoid sparse reconstruction, and instead pursue a much simpler l2-norm-minimizing linear estimate of the signal corresponding to: $\vec{x} \approx \Phi^{T}(\Phi\Phi^{T})^{-1}\,\hat{x}$. We note that this corresponds to the transform $\Phi^{T}(\Phi\Phi^{T})^{-1}\Phi$ applied to the original signal $\vec{x}$ ($\hat{x} = \Phi\vec{x}$). Since Φ is a random matrix, such a transform will also exhibit properties of a random matrix. This is significant because as described in Section IIIB, the inner products of vectors are preserved following random projection, enabling computation of energy-based features directly from the compressed signals. While we expect this linear estimation to incur error, especially after filtering the estimated signal with $\boldsymbol{H}$ (and further compression via Θ as described in [2]), we find this to be sufficiently minimal for subsequent classification.

C. System Demonstration

A system prototype is formed using a-Si TFT-based circuits. Seizure detection on 4950/100 non-/seizure 2-sec epochs from the CHB-MIT dataset [17], [18] is performed, using the algorithm described in [19]. Fig. 6, which compares energies of 20 epochs after filtering (centered at 0Hz), shows that the error incurred due to linear estimation is minimal. The performance of the system is maintained out to high compression rates (i.e. error rate<8% at 64× compression).

V. Conclusions

Hybrid LAE-CMOS systems provide a platform for the development of human-centric systems, incorporating both on-person and ambient sensors. A major challenge in building these systems lies in the interfacing between the two technologies. Recognizing the importance of transferring higher-level information rather than raw data, we have explored information-processing-based solutions, in addition to circuit-based approaches. The two case studies illustrate that by shifting the LAE-CMOS boundary to implement selective LAE-based transforms for feature extraction, a significant reduction in the number of interfaces can be achieved, while still enabling subsequent processing to be leveraged in CMOS towards high levels of performance.

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