

A 10-b Statistical ADC Employing Pipelining and Sub-ranging in 32nm CMOS

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Abstract—This paper presents a 10-b statistical ADC (S-ADC), achieving higher resolution (INL) than any previously reported S-ADC. This resolution requires a large number of statistical observations via comparators (12k) with offset variation, making code estimation a key challenge. The efficiency of estimation is enhanced by a coarse frontend estimator, employing pipelining and sub-ranging to arrive at a reduced range, which is then provided to a fine backend estimator. The total computations are reduced by 19 \times , compared to single-stage estimation over the entire analog range. Implemented in a 32nm process, the S-ADC achieves $INL < 1.73$ LSB and total code estimation error (non-linearity and noise) < 2.3 LSB_{RMS}. Designed to run at 20MHz, excess supply impedance limits comparator speed to 2MHz. The energy per 10-b conversion for the comparator array (at 2MHz) is 744 pJ and the energy per 10-b conversion of the digital estimator (at 20MHz) is 627 pJ.

Keywords—Analog-digital conversion; analog-digital integrated circuits; estimation; statistical distributions

I. INTRODUCTION

Statistical ADCs (S-ADCs) represent a class of ADCs that utilize stochastic behaviors (e.g., variations) at the circuit and device levels as mechanisms for data conversion. The appeal of S-ADCs is that they potentially avoid the need to employ resource-intensive strategies for mitigating such behaviors, as are required in traditional ADCs. Instead, statistical estimation is employed with the stochastic behaviors to arrive at the output code. However, thus far, S-ADCs have primarily employed only flash-type architectures [1-3]. This has limited their achievable resolution and energy efficiency. The aim of this paper is to introduce architectural enhancements, namely pipelining and sub-ranging, which have substantially benefitted traditional ADCs. More theoretical concepts behind this were discussed in [4]. Here, we present the architecture and associated circuits, implementing a 10-b S-ADC in a 32nm SOI technology.

II. STATISTICAL-ADC (S-ADC) ARCHITECTURE

Fig. 1 shows a block diagram of the proposed S-ADC. The analog input is fed to an array of comparators, whose variations lead to a set of 1-b statistical observations. An estimate of the corresponding 10-b digital code is then derived using a frontend estimator (FE), backend estimator (BE), and decoder. As is typical in S-ADCs, the accuracy of code estimation is limited by the number and distribution of the statistical

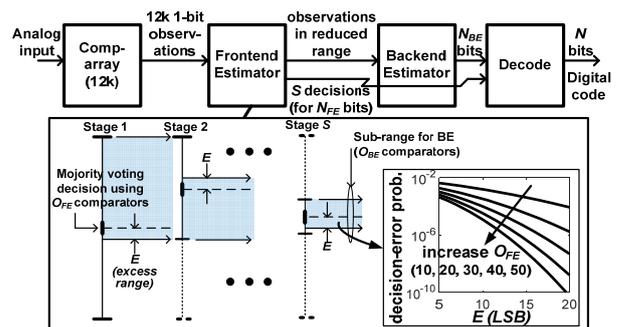


Fig. 1. Block diagram of S-ADC with pipelining and sub-ranging scheme in FE.

observations [1]. The problem is that statistical estimation over a large number of observations increases computational energy, making it dominate the S-ADC. Our aim is to minimize this. The FE performs coarse estimation to derive N_{FE} MSBs by employing pipelining and sub-ranging. The BE then performs fine estimation over a smaller range to derive N_{BE} LSBs through a simplification to maximum likelihood estimation (MLE) made feasible thanks to the reduced estimation range [4]. Thus, $N_{FE} + N_{BE} = 10$.

As shown in Fig. 1, the FE consists of S stages, each making a binary decision to successively sub-divide the estimation range. Each decision is based on majority voting over O_{FE} comparator observations, whose averaged nominal threshold is at the midpoint of the range. If each stage were to divide the estimation range by half, decisions to full (10-b) accuracy would be required, necessitating large O_{FE} and thus high computational energy in each stage. Rather, a sub-range larger than half is retained following each decision, requiring $S > N_{FE}$. This allows decision errors to be tolerated, as seen from the plot of decision-error probability vs. the excess range E . As a result, O_{FE} can be reduced, leading to lower energy.

The BE then performs fine MLE within the final sub-range by employing O_{BE} comparator observations, whose averaged nominal threshold is at the mid-point of the sub-range. Within this reduced sub-range, the comparators can be assumed to have thresholds drawn from the same probability density function (PDF), thereby substantially simplifying MLE computation [4].

Energy savings primarily result thanks to sub-ranging in the FE. Namely, rather than devoting a large number of observations for fine estimation over the *entire* analog range,

fine estimation can be confined to a *substantially smaller* range, thus requiring fewer comparator observations. The tradeoff is that energy must now be expended to make sub-ranging decisions in the FE stages. While the excess sub-range E at each stage is critical for reducing this energy, E ultimately limits the amount to which the final sub-range can be reduced. Thus, there is a tradeoff between the computational complexity in the BE (set by the final size of the sub-range for fine estimation) and the FE (set by the number of stages and the energy per stage, to arrive at the final sub-range).

Fig. 2 shows this tradeoff, based on simulations [targeting decision-error probability of 10^{-5} in the FE stages and root-mean-square error (RMSE) of 1.3 LSB in the BE, at a 10-b level] [4]. The underlying computations in both the FE and BE are additions over comparator observations. The total number of additions is minimized at a particular size of the final sub-range, represented as N_{BE} : below this, a smaller range necessitates additional sub-ranging decisions, and thus higher FE energy; above this, a larger range necessitates higher BE energy. The effect of increasing E is also shown, having the benefit of reducing the energy of FE decisions [notice that larger E also limits how small the final range (i.e., the minimum possible N_{BE}) for fine estimation can be made]. From Fig. 2, we can see the benefit of sub-ranging in the FE; the optimal point amounts to $19\times$ fewer additions compared to fine estimation over the entire range (i.e., $N_{BE}=10$), as used in previous architectures [1-3]. From the simulations, the optimal N_{FE} and N_{BE} are thus determined to be 5 and 5, respectively, corresponding to optimal O_{FE} , O_{BE} , E , and S of 18, 492, 14 LSB, and 8, respectively. To simplify the implementation, as presented below, O_{FE} is designed to be 36 and O_{BE} is designed to be 492. Though this moves us slightly off the optimal point shown, the analysis in Fig. 2 assumes that the BE performs all of its own required computations; in fact, some of additions performed in the FE, i.e., which fall in the final sub-range, can actually be reused in the BE. Thus, even at our design point, the total number of additions performed is reduced by $19\times$, compared to fine estimation over the entire range.

III. IMPLEMENTATION

A. Comparator Array

Fig. 3 shows the comparator array. The analog input range is 0-0.9V, set by the technology. Over this range, a resistor string is employed to create a uniform distribution of nominal comparator thresholds. On top of this, the comparators (employing nearly minimum-sized devices) exhibit the offset distribution shown, having $\sigma_{OS}\approx 17\text{mV}\approx 20\text{LSB}$ (from Monte Carlo simulations). To ease the implementation, the number of resistor-string taps can be reduced so long as the voltage differences are substantially smaller than σ_{OS} . From MATLAB simulation of the architecture, we verified that 256 taps (i.e., voltage difference of 4LSB) is sufficient. Further, at the given σ_{OS} , simulations determine that the total number of comparator observations required for <1.3 LSB RMSE at the 10-b level is 12k [4]. These are distributed uniformly among the taps, resulting 48 comparators at each nominal threshold.

To minimize the effects of kickback noise from such a large number of comparators, the value of resistors in the string

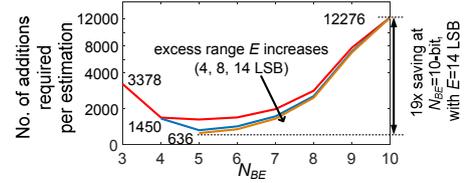


Fig. 2. Total number of additions in FE and BE, showing minimum achieved in the proposed architecture.

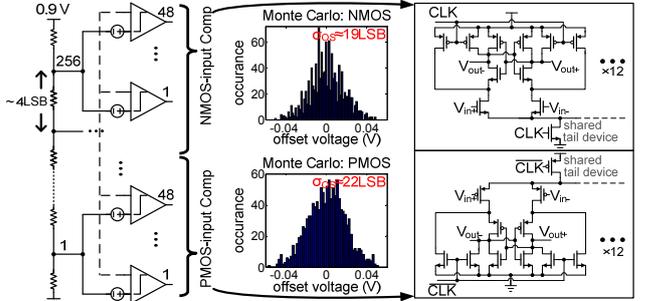


Fig. 3. Comparator-array implementation and simulated comparator offset.

is set to 20 k Ω , based on simulation. For strong regeneration of comparators across the array, the top-half employs NMOS-input comparators, and the bottom half employs PMOS-input comparators, as shown. Finally, for compact layout, the tail enable device is shared among 12 comparators.

B. Frontend Estimator (FE)

The FE is composed of blocks referred to as observation pipelines (OBPIPEs). Each OBPIPE takes, as input, statistical observations from a group of comparators who share a resistor-string tap. Within each OBPIPE, the input observations are progressed forward in a pipeline corresponding to the $S=8$ stages of the FE. To ease the layout, the 48 comparators sharing a tap are actually split to feed four parallel, identical OBPIPEs; each OBPIPE thus takes 12 inputs, and there are total of $\sim 1\text{k}$ (1025) OBPIPEs.

In the design, there are 8 different versions of OBPIPEs (OBPIPE1, ... OBPIPE8). The different versions are required because certain comparator observations are involved in sub-ranging decisions at each stage. For this reason, the corresponding OBPIPEs must perform addition over those observations, to enable the majority voting. Subsequently, the addition results can be progressed forward in the pipeline, rather than the original observations, as these may be used for fine estimations in the BE, depending on the final sub-range selected after the S stages. For comparator observations not involved in sub-ranging decisions, additions should not be performed until it is determined that these are required either for subsequent sub-ranging decisions or for eventual fine estimation. This enables the computational energy savings within the architecture. Further, for comparator observations determined to be outside of the selected sub-range at each stage, the observations or addition results should not be progressed forward in the pipeline in order to save active energy in the OBPIPEs.

The circuit structure of the OBPIPEs is explained through one of the OBPIPE versions shown in Fig. 4. (a). Progression

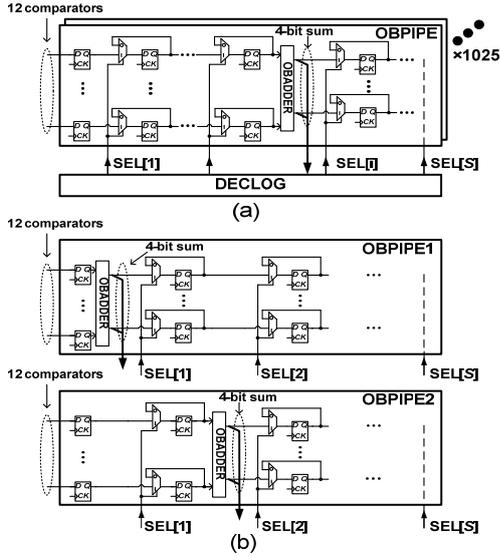


Fig. 4. Structure of OBPIPEs (a) generally, and (b) for two versions.

through the pipeline is gated by $S=8$ select signals $SEL[1-S]$, which are asserted by a Decision-Logic block (DECLOG) if the pipeline stage belongs to a selected sub-range. The gating is performed via a multiplexor that feeds back the pipeline register's output, thereby eliminating a logic transition (full clock-network gating would be preferred, but is avoided in this implementation to ease clock-network layout and timing closure). At a point in the pipeline where the comparator observations may be required for a sub-ranging decision, an Observation Adder (OBADDER) block is inserted, to convert the 12 comparator observations into a 4-bit sum. For $O_{FE}=36$, the sums from 3 OBPIPEs are then provided to DECLOG to make the sub-ranging decision and generate a tree of SEL signals to feed all OBPIPEs. For illustration, Fig. 4. (b) shows two particular OBPIPE versions (OBPIPE1, OBPIPE2), corresponding to comparator observations used for first-stage and second-stage sub-ranging decisions, respectively. Notice, following addition by the OBADDER, the 4-bit sum, rather than the original comparator observations is conditionally progressed in the pipeline, as only these would be required for fine estimation in the BE.

C. Backend Estimator (BE)

Given the reduced range for fine estimation, the BE employs summation over O_{BE} observations to perform an approximation to MLE. MLE involves solving the following objective function to derive the estimate \hat{x} [where x is the analog voltage, c_i is a comparator output, and $p_{c_i|x}(c_i|x)$ is the probability of the observed comparator output conditioned on the analog input]:

$$\hat{x} = \arg \max_x \prod_{i=1}^{O_{BE}} p_{c_i|x}(c_i|x). \quad (1)$$

Typically, solving this in the log domain enables simplification, by transforming multiplication over the probabilities into summation. The challenge that remains when using a large number of observations (needed to improve estimation) is that the number of probability terms is

proportionately large, making the solution intractable. Analysis in [4] shows that thanks to the reduced range of estimation, all $O_{BE}=492$ observations employed can be assumed to have the *same* probability function $p_{c_{BE}|x}(c_{BE}|x)$. This simplifies the log-domain objective function to a single probability term, based on an effective probability density function (PDF_{eff}) and associated cumulative distribution function (CDF_{eff}). The nominal PDF_{eff} is based on both the equally spaced resistor-tap voltages and the statistical comparator offsets. Setting the derivative of the log-likelihood function to zero, the approximate MLE is thus reduced to the following (where A is the number of comparators with observation equal to '1'):

$$CDF_{eff}(\hat{x}) = \frac{\sum_{i=1}^{O_{BE}} c_{BE,i}}{\sum_{i=1}^{O_{BE}} 1} = \frac{A}{O_{BE}}. \quad (2)$$

To solve this efficiently to N_{BE} bits of precision, the BE employs the approach shown in Fig. 5. The corresponding $2^{N_{BE}} - 1$ values of the CDF_{eff} are stored in N_{BE} pipelined look-up tables, and the A/O_{BE} ratio is compared to the stored values, using binary search to resolve the N_{BE} bits (COMP[i]). This is possible because CDF_{eff} is a monotonically increasing function.

To enhance the accuracy of estimation, rather than simply using nominal values of the CDF_{eff} in the look-up tables, two calibration approaches are explored. First, foreground calibration is explored. With $S=8$ in the FE, the CDF_{eff}'s for each of the 256 possible sub-ranges that the BE could be presented with are calibrated for the given S-ADC and stored in the look-up tables. Second, statistical calibration is explored. Here, the CDF_{eff}'s for each of the 256 possible sub-ranges are once again stored, but, this time, these are calibrated by averaging over a set of previous S-ADCs. Thus, calibration for a particular S-ADC is not required. The methods for calibrating the CDF_{eff}'s are presented in Section IV.

IV. PROTOTYPE TESTING

The prototype S-ADC is fabricated in a 32nm CMOS SOI process from GlobalFoundries. A die photo and measurement summary are in Fig. 6. Details are in the sections below. As shown, the $\sim 1k$ FE OBPIPEs are laid out as two 64×8 arrays (plus a 1025th OBPIPE in an extra row), with the DECLOG block placed in between.

A. Comparator Offset and Noise Measurement

During testing, larger-than-expected supply noise was observed due to power-grid layout error. To overcome this, the

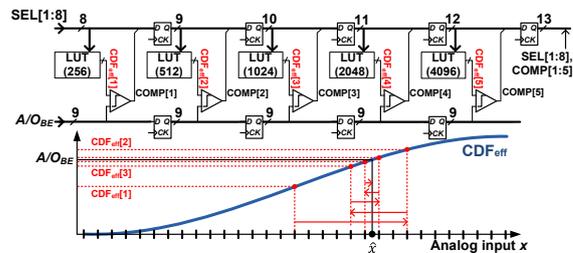


Fig. 5. Approximate MLE based on pipelined binary search of look-up tables.

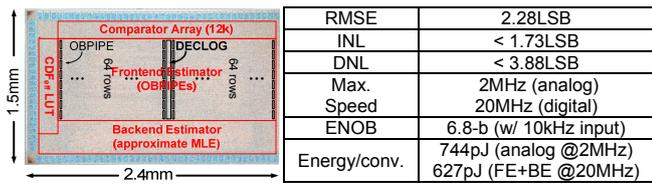


Fig. 6. S-ADC die photo and measurement summary.

analog supply was lowered to 0.6V, reducing the current (and IR noise), but also limiting the speed of the comparator array to 2MHz.

Then, both the noise and static offset of the 12k comparators were characterized. The first stage of every OBPIPE consists of a bank of flip-flops, which can be configured into a scan-chain to acquire the raw comparator outputs for any analog input. To characterize the noise and offset, the S-ADC is driven, multiple times, by a step-by-step analog ramp, generated using a 14-b linear DAC (appropriately scaled to the input range). Fig. 7(a) shows the reconstructed output of a particular comparator during one ramp; due to various noise sources, we see that the output value does not have a clear trip point, with respect to the analog input. Thus, the reconstructed output is averaged over multiple ramps (10 runs), allowing us to identify both an average trip voltage and a standard deviation. The average is taken to be the offset-dependent effective trip voltage, and the standard deviation is taken to be the noise. Fig. 7(b) then shows the effective trip voltage of each indexed comparator, and Fig. 7(c) shows the standard deviation (noise). Finally, having found the effective trip voltages, Fig. 7(d) shows the standard deviation σ_{OS} of the comparator offset in each group of 48 comparators, sharing a nominal trip voltage (resistor-string tap); as seen, σ_{OS} is similar to that expected from Monte Carlo simulations.

B. CDF_{eff} Calibration

The effective trip voltages are used to calibrate the CDF_{eff} 's employed in the BE for fine estimation. With $S=8$ stages in the FE, 256 different sub-ranges can be selected for use by the BE. Because of the excess range E associated with each sub-range decision, the sub-ranges will overlap. Further, due to non-linearity in the FE, the selected sub-ranges are not contiguous with respect to the input voltage. Thus, for best overall linearity of the S-ADC, the CDF_{eff} values should be calibrated considering the FE decisions. Accordingly, calibration is performed by choosing CDF_{eff} values that maximize the linearity of the final decoded S-ADC output (i.e., based on the FE decisions and BE estimate). This is done by selecting the linearization range of each CDF_{eff} based on where sub-range transitions actually occur due to FE decisions.

For foreground calibration, this approach is applied for each die of the S-ADC. For statistical calibration, a pool of seven S-ADC die are taken to perform 7-fold cross-calibration (i.e., each of the seven die are calibrated using the average over the other six).

C. INL/DNL and ENOB

Following calibration, the measured INL/DNL are shown in Fig. 8 [(a) is for foreground calibration, and (b) is for

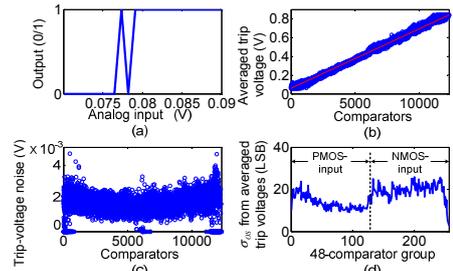


Fig. 7. Statistics of comparator trip voltages: (a) output of a particular comparator; (b) averaged effective trip voltage; (c) trip-voltage noise of each comparator; (d) σ_{OS} from averaged trip voltages over 48-comparator group.

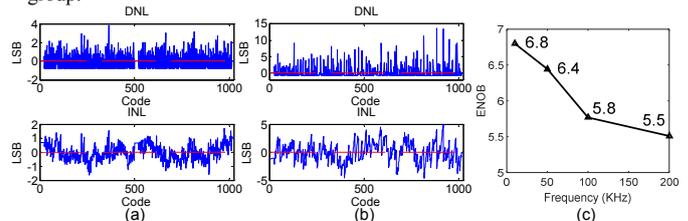


Fig. 8. (a) INL/DNL in foreground calibration; (b) INL/DNL in statistical calibration; (c) ENOB in foreground calibration.

TABLE I. COMPARISONS BETWEEN [1-3] AND THIS WORK

Technology	0.18um [1]	0.18um [2]	0.25um [3]	32 nm [This work]
Area (mm ²)	5.76	2	1.2 (core)	3.6
Resolution (bit)	6	6	6	10
max(INL/DNL) (LSB)	-1.06/+1.07	-0.91/1.23	N/A	-1.62/3.88
No. of comparators	1152	127	332	12k

statistical calibration]. Foreground calibration gives $INL < 1.73$ LSB and $DNL < 3.88$ LSB. The RMSE is 2.28 LSB, higher than the simulated 1.26 LSB due to noise; this corresponds to an ENOB of 6.8-b with 10 kHz input. Statistical calibration gives $INL < 5$ LSB and $DNL < 14$ LSB, with RMSE of 6.42 LSB; the lower performance is due to die-to-die variation. Both cases have missing codes. Table I compares [1-3] and this work.

V. CONCLUSION

As device-level variabilities increase, S-ADCs represent an intriguing direction, whereby circuit resources need not be expended to overcome certain variabilities. This paper presented a 10-b S-ADC in 32nm CMOS that integrates 12k comparators. The prototype achieves an INL of 1.73 LSB, and reduces the computations by 19 \times . The final digital energy is 627pJ, now falling below the analog comparator energy of 744pJ. Though not at the state of the art for ADCs generally, this represents a step forward for S-ADCs.

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