17.3 Hybrid System for Efficient LAE-CMOS Interfacing in Large-Scale Tactile-Sensing Skins via TFT-Based Compressed Sensing

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Tactile sensing has wide-ranging applications, from intelligent surfaces to advanced robotics. Large-Area Electronics (LAE), based on low-temp. fabrication (<200°C) of thin films, presents distinct capabilities, due to compatibility with a broad range of materials (enabling diverse transducers), as well as large and flexible substrates and materials-deposition methods (enabling expansive and formfitting sensing arrays). However, low performance/energy-efficiency of LAE thin-film transistors (TFTs) necessitates hybrid systems, integrating Si-CMOS ICs for system functions (sensor readout/control, processing, etc.). Initial work shows that a primary challenge in hybrid systems is the large number of interfaces required between LAE and CMOS, particularly as the number of sensors scales [1,2]. This paper presents a force-sensing system that exploits signal sparsity exhibited in many large-area tactile-sensing applications (e.g., detecting point damage/stress in structures [3]), to reduce interfacing complexity to the level of sparsity, rather than a level related to the number of sensors (e.g., [1]). This is achieved via compressed sensing (CS), enabling sensor-acquisition by simple switches, readily implemented using TFTs. While CS has previously been leveraged in a hybrid-system architecture targeting signal sampling-rate requirements [2], this system applies it for high spatial resolution in tactile sensing.

Figure 17.3.1 summarizes CS and the system-level motivations. As shown, CS involves sampling different superpositions $\vec{y}$ of input data $\vec{x}$ (having dimensionalities M and N, respectively), via a measurement matrix ϕ. CS theory says that: (1) if $\vec{x}$ has at most K non-zero elements (K sparse), only $M>K\times\log_2(N/K)$ different superpositions are needed to reconstruct $\vec{x}$; and (2) a random and simple matrix ϕ, with elements 0/1, can be found for acquiring such superpositions. This makes TFT implementation possible, and Fig. 17.3.1 compares how system complexity (vs. number of sensors N) would scale compared to traditional TFT architectures for hybrid-system interfacing (sequential scanning, active matrix), based on the following key metrics: (1) number of acquisition cycles (operational complexity); (2) number of interfaces (system-assembly complexity); (3) dynamic range (DR) of each interface (CMOS/readout complexity); (4) number of TFTs (LAE complexity). If M,K<<N (i.e., high sparsity), CS substantially benefits cycles and interfaces, which together with DR represent total data bandwidth of transfer, and can be traded-off. But, modest increase in DR (~K) is preferred, as it pushes complexity to the high-efficiency CMOS domain and because sensor proximity to embedded signals in tactile sensing typically yields large responses [3]. A drawback with CS is the number of TFTs; but, as described below, the statistical nature of acquisition with CS enables high tolerance to typical TFT faults.

Figure 17.3.2 shows the CS hybrid-system architecture, demonstrated for an array of resistive force sensors (applicable to other resistive sensors, e.g., temp./strain/pressure/light). While the transfer function of $R_{SNS,i}$, shown for 10 sensors, exhibits variation, the aim of tactile sensing is often coarse readout from each sensor, but with high spatial resolution. Each sensor feeds an access TFT, controlled to implement the 0/1 elements of ϕ for one column. A TFT Matrix-Logic Control block controls the access TFT, via a Matrix-Row-Selection code R/Rb[4:0] from CMOS. The control-block details are shown, consisting of matrix TFTs arranged in 32 branches with 5 TFTs/branch. The Matrix-Control signal C/Cb[4:0] enables one branch at a time, driving the access-TFT gate high/low (V_{ON}/V_{OFF}). To simplify design, the Matrix-Logic Control block is the same for each sensor, but the connections between R/Rb[4:0] and C/Cb[4:0] are different, so that the access TFTs are enabled differently as R/Rb[4:0] is cycled through 32 codes (e.g., truth-table shown for 20th sensor). By superimposing the currents from accessed sensors via the CMOS TIA, which ensures constant sensor biasing of 0.4V, a 32-row ϕ matrix is realized. The architecture thus employs a single interface and M=32 cycles, one for each conceptual row of ϕ (same effective data bandwidth as Fig. 17.3.1); but, an additional 5 differential interfaces are required for R/Rb[4:0]. M=32 supports up to N=120 sensors at target sparsity of K=3, but 20 sensors are implemented for demonstration (requiring 20×(5×32)=3200 matrix TFTs). The W/L's for matrix/access TFTs are shown, designed for access-TFT on-resistance $R_{ACC}\approx1.5k\Omega$, well below the target range for force sensors.

Figure 17.3.3 analyzes TFT fault tolerance. While all interfacing architectures in Fig. 17.3.1 require an access TFT, the 160 matrix TFTs per sensor pose notable overhead (though, this increases slowly with number of sensors N, due to $\log_2$-dependence of M on N). Figure 17.3.3 shows substantial system tolerance to matrix TFT faults. Typical faults include: (1) S-D open; (2) S-D leakage/short; (3) G-S/D leakage/short. Probability of G-S/D shorts must be controlled, as it impacts the global control signal R/Rb[4:0]; this can be done via gate-dielectric processing (oxide quality/thickness, minimizing gate-electrode hillocks). Other faults can be analyzed by considering their effective impact on ϕ. As shown, S-D opens cause element values to be set by charge dynamically held at the access-TFT gate from the previous state, corresponding to previous row. On the other hand, S-D leakage/shorts and G-S/D leakage cause contention at the access-TFT gate, making elements take intermediate values. Monte Carlo simulations, applying such fault models, show high reconstruction SNR (RSNR) is maintained to high fault rates (much higher than typically allowed for access TFTs), and RSNR improves with even higher N. This is due to use of statistical-optimization methods and many superpositions in the CS reconstruction process.

Figure 17.3.4 shows a block diagram of the CMOS IC, having 8 channels of a TIA, offset-correction, and 10b ADC readout chain, as well as digital control and R/Rb[4:0] generation. Offset correction consists of a 32-word register file and 7b current DAC (I-DAC). This enables an offset-correction current to be applied to the TIA for each matrix-row readout, via a code in the register file determined at start-up (with no force applied). The I-DAC consists of 6 binary-weighted N/PMOS current sources. The TIA employs a 2-stage op-amp, designed for stability with 500pF of input capacitance, supporting >200 access-TFT load. The ADC is a 10b SAR with 5b main/sub cap-DACs. The 8 channels enable further scaling in sensor number, via parallel arrays.

The force-sensing system is implemented with in-house-fabricated ZnO TFTs, commercial force sensors, and custom 130nm CMOS IC (Fig. 17.3.7). To ease testing, 3 PCBs are used, consisting of: (1) 20 force sensors; (2) 20 wire-bonded matrix-control/access-TFT die; (3) CMOS IC. The TFTs are fabricated on glass for dicing and wire bonding, but are fully flex compatible (process temp. <200°C). Figure 17.3.5 (left) shows overlaid waveforms from 32 TFT die from one sample, showing proper matrix-TFT operation, and proper pull up/down by access TFT (with test 10kΩ load resistor connected to 1V). Also shown are the I_D-V_{DS}'s of the access TFTs, showing $1k\Omega<R_{ACC,i}<1.9k\Omega$ (in V_{DS} range of interest for sensor resistance). Figure 17.3.5 (right) shows CMOS IC measurements, including ADC and full-system (TIA+ADC) DNL/INL, as well as the ADC code vs. I-DAC code (no input current). A summary table is at the bottom.

Figure 17.3.6 shows the demonstration setup, as well as full-system sensor acquisition/reconstruction. A sample heat map is shown for force-sensor resistance, both directly measured and reconstructed by the system, with <2.9% error (after correcting for nominal $R_{ACC,i}$=1.5kΩ). The scatter plot is derived from many such measurements, showing error of $0.7k\Omega_{RMS}$. R/Rb[4:0] codes switch at 1kHz, giving frame rate of 1kHz/32=31fps, and total energy of 1.2μJ/frame.

Acknowledgements:
This work was supported by the Semiconductor Research Corporation (SRC), Princeton Program in Plasma Science and Technology, DARPA and Princeton University. IC fab provided by MOSIS.

References:
[1] Y. Afsar, et al., "Large-Scale Acquisition of Large-Area Sensors Using an Array of Frequency-Hopping ZnO Thin-Film-Transistor Oscillators," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb. 2017.
[2] T. Moy, et al., "A Flexible EEG Acquisition and Biomarker Extraction System Based on Thin-Film Electronics," *ISSCC Dig. Tech. Papers*, pp. 294-295, Feb. 2016.
[3] B. Glisic, et al., "Strain Sensing Sheets for Structural Health Monitoring Based on Large-area Electronics and Integrated Circuits," *Proc. of IEEE*, vol. 104, no. 8, pp. 1513-1528, June 2016.

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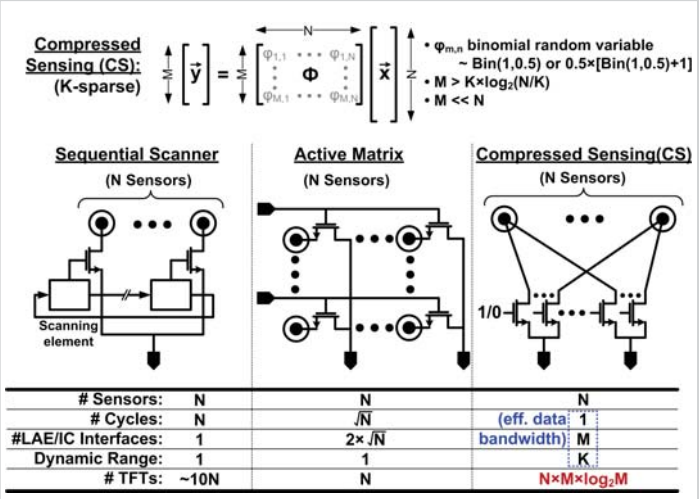


Figure 17.3.1: Summary of CS (M measurements for N sensors), and comparative analysis of systems with traditional hybrid-system-interfacing architectures, as N scales.

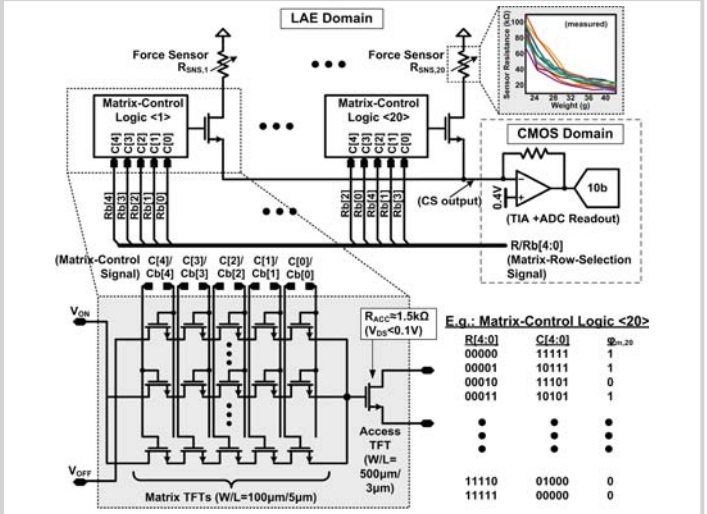


Figure 17.3.2: System for performing readout of sensor-current superpositions, controlled by access and matrix TFTs, using Matrix-Row-Selection signal R/Rb[4:0].

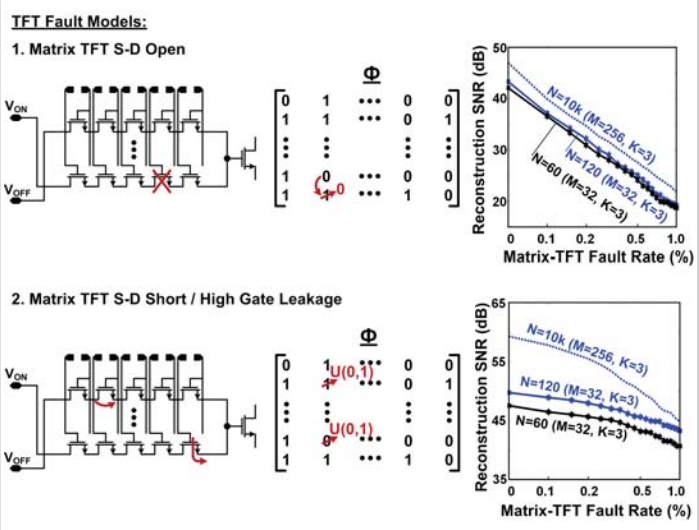


Figure 17.3.3: Analysis of reconstruction-performance tolerance to typical faults in matrix TFTs.

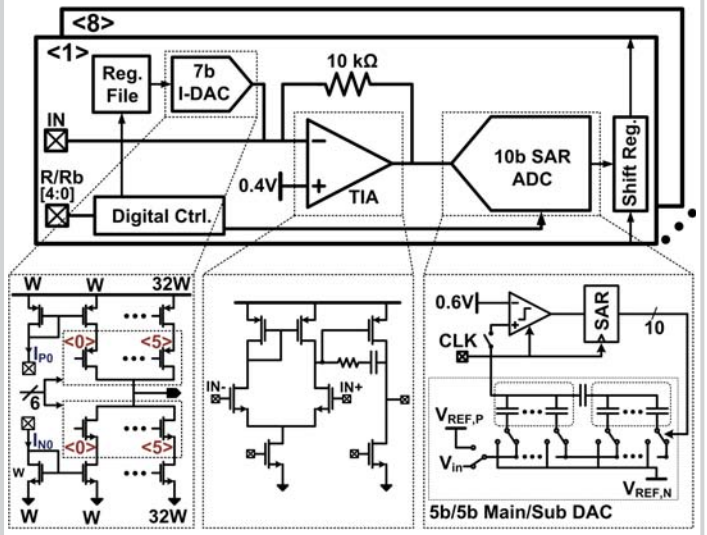
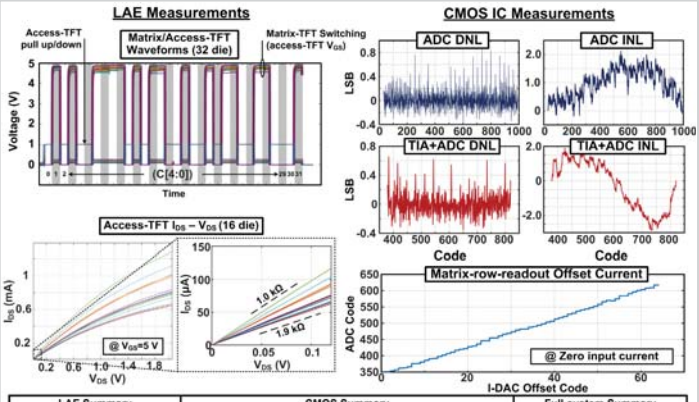


Figure 17.3.4: Block diagram of CMOS IC for matrix-row readout, showing 8 readout channels comprised of offset-canceling I-DAC, TIA, and 10b ADC.



LAE Summary		CMOS Summary				Full-system Summary	
No. sensors	20	Technology	130nm	ADC resolution	10 b	Sensor F range	24 g-40 g
TFT technology	ZnO	V_{DD}	1.2V	ADC energy	212 pJ/conv.	Sensor R range	100 kΩ-15 kΩ
Process temp.	<200°C	Area	4mm²	ADC DNL/INL	0.85/2.0	Sparsity	3
TFTs/sensor	161	No. channels	8	ADC rate	100 kS/s	Recon. error	0.7 $kΩ_{RMS}$
Matrix-TFT speed	1 kHz	TIA power/ch.	37μW	ADC ENOB	8.7 b @50kHz	Frame rate	31 fps
Access-TFT res.	1.5 kΩ	I-DAC res.	6b	TIA+ADC DNL/INL	0.65/2.0	E/frame	1.2 μJ

Figure 17.3.5: Matrix-Control block and access TFTs (left), CMOS ADC DNL/INL, full-system (ADC+TIA) DNL/INL, and I-DAC transfer function (right), with summary table.

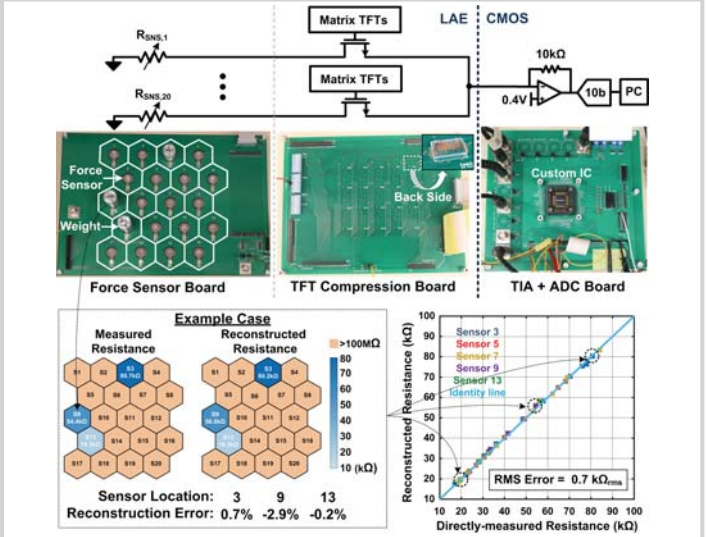


Figure 17.3.6: Measurement and demonstration setup as well as characterization of reconstruction accuracy.

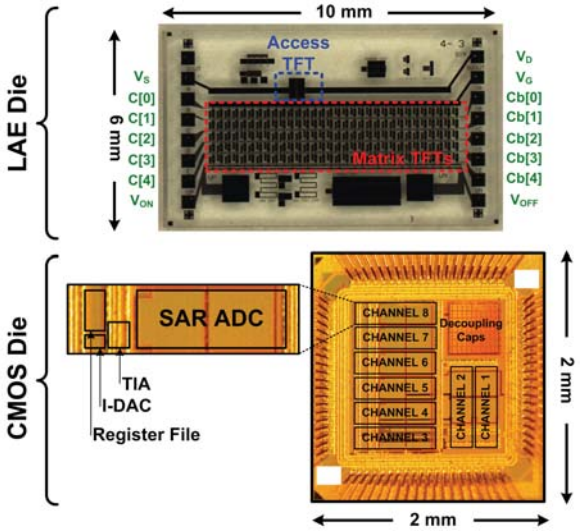


Figure 17.3.7: TFT die micrograph (showing matrix/access TFTs) and CMOS IC die micrograph.

978-1-5386-8531-0/19/$31.00