nature electronics

ARTICLES

https://doi.org/10.1038/s41928-021-00648-z

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A phased array based on large-area electronics that operates at gigahertz frequency

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Large-aperture electromagnetic phased arrays can provide directionally controlled radiation signals for use in applications such as communications, imaging and power delivery. However, their deployment is challenging due to the lack of an electronic technology capable of spanning large physical dimensions. Furthermore, applications in areas such as aviation, the Internet of Things and healthcare require conformal devices that can operate on shaped surfaces. Large-area electronics technology could be used to create low-cost, large-scale, flexible electromagnetic phased arrays, but it employs low-temperature processing that limits device- and system-level performance at high frequencies. Here we show that inductor–capacitor oscillators operating at gigahertz frequencies can be created from large-area electronics based on high-speed, self-aligned zinc-oxide thin-film transistors. The oscillator circuits incorporate frequency locking and phase tuning, which are required for electromagnetic phased arrays. We integrate our phase-tunable oscillators in a 0.3-m-wide aperture, creating a phased array system that operates at ~1 GHz and is capable of beamforming.

The electromagnetic (EM) field of a radiative aperture depends on its dimensions and frequency, and remains the same when these two parameters are inversely scaled. For a phased array, controllability of its radiation pattern is determined by the ratio of aperture size (D) to radiation wavelength (λ). In the far field, where the aperture is small compared with the radiation distance (r) (that is, the Fraunhofer region, where $r \gg \sim \frac{D^2}{\lambda}$), a phased array looks like a point-source radiator, resulting in a steerable beam, with angular resolution determined by D/λ (ref. [1]). In the near field, where the aperture is increased to the order of the radiation distance, (that is, the Fresnel region, where $r < \sim \frac{D^2}{\lambda}$), the radiator effectively gains additional geometric degrees of control, enabling focusing on a single point. Examples of beam-steering and beam-focusing radiation patterns are given in Supplementary Fig. 1. Beyond steering and focusing, the enhanced control from increasing D/λ also enables richer and more diverse radiation patterns to be achieved[2]. These factors have implications for various emerging applications. They could, for example, enable high specificity in three-dimensional spatial addressing over densely distributed nodes in the Internet of Things (IoT)[3,4] and precise delivery of therapies such as localized wireless heating in healthcare[5,6].

While D/λ is a critical parameter in phased array systems, the feasible dimension (largest D) and highest operation frequency (smallest λ) that can be achieved depend on the underlying technology. Conventional technologies, such as silicon complementary metal–oxide–semiconductor (Si-CMOS), are capable of operating at high frequencies up to hundreds of gigahertz[7], but chip sizes are limited (typically from a few millimetres to a few centimetres), restricting D and hence the frequencies at which high D/λ can be achieved. For decades, research has explored enhancing D/λ through assembly methods by placing together numerous discrete active and passive components based on different technologies[5,8–19]. In practice, these non-monolithic integration approaches have problems with scalability, reliability and cost, which impede the wide-scale deployment of emerging phased array applications. While monolithic implementations have recently become possible by going to shorter wavelengths (that is, frequencies higher than 60 GHz)[20,21], the substantial attenuation in air[22] limits applications such as long-distance communications and wireless power transfer.

Large-area electronics (LAE) is an alternative technology based on low-temperature (<200 °C) deposition and processing of thin-film metals, semiconductors and dielectrics on glass or plastic substrates. The approach provides the monolithic integration of a range of active/passive electronic devices and transducers over large dimensions[23–31]. LAE-based flat-panel displays, X-ray imagers and solar panels are already in mass production. The display industry has driven the development of process technology for LAE-based integrated circuits on substrates up to 10 m^2 in size with reducing cost per area (roughly \$30.0 m^{-2} today[32] versus \$0.1 mm^{-2} for Si-CMOS[33]). Further process technology development focuses on even larger sizes using additive printing and roll-to-roll production[34], as well as on flexible form factors using plastic substrates. Recent research in LAE systems has also focused on new applications that can take advantage of these unique physical attributes, especially by exploiting the compatibility with diverse materials enabled by low-temperature processing towards a range of sensing applications[28,29,35–40].

Low-temperature processing, however, degrades semiconductor electrical properties, leading to low performance of active semiconductor devices such as thin-film transistors (TFTs). For instance, electron mobility is limited to around 1 $cm^2 (V\,s)^{-1}$ in amorphous silicon (a-Si) technologies. Recent research on thin-film metal–oxide semiconductors and low-temperature polysilicon has pushed this to 10–100 $cm^2 (V\,s)^{-1}$ (refs. [23,41–43]). A handful of demonstrations have also reached the near-gigahertz range for device metrics (f_T and f_{MAX})[44–47] and small two-transistor oscillator test circuits[48]. But no system has yet demonstrated operation in the microwave frequency range (300 MHz to 300 GHz), which is required for D/λ in practical EM phased array applications.

In this Article, we show how the scaling and electronic properties of LAE-based thin-film technologies make them suitable for use in the manufacture of large D/λ phased array systems. We use

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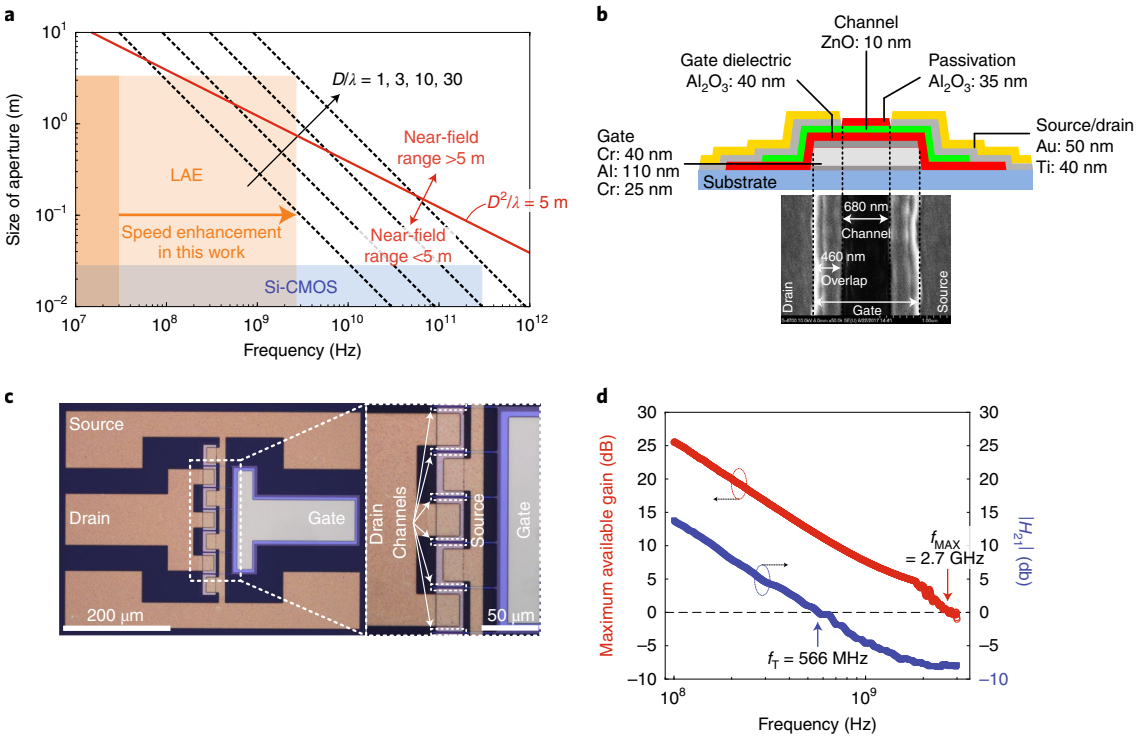

Fig. 1 | Values of D/λ of LAE and device optimization. a, Comparison of aperture sizes and frequencies achievable by LAE and Si-CMOS technologies. The dashed straight black lines illustrate $D/\lambda = 1$, 3, 10 and 30. The solid red line shows the smallest aperture size that attains near-field operation at a distance of up to 5 m (that is, $D = \sqrt{\lambda r}$, where $r = 5$ m). For LAE, the darker-shaded region denotes the regime previously achievable; this work extends to the lighter-shaded region. **b**, Schematic of the cross-section of a bottom-gate LAE ZnO TFT, and corresponding top-view SEM image highlighting the channel region self-aligned to the underlying gate. The low-resistance gate metal consists of a stack of Cr/Al/Cr (25/110/40 nm), with the bottom Cr layer providing adhesion to glass or plastic substrates and the top Cr layer providing the desired work function. The gate dielectric (Al_2O_3), channel semiconductor (ZnO) and passivation (Al_2O_3) layers were deposited by plasma-enhanced atomic layer deposition. Ti/Au (40/50 nm) formed the source/drain contacts. **c**, Microscopy images of a ZnO TFT fabricated on glass. The TFT (width, $W_{TFT} = 150.0$ μm; length, $L_{TFT} = 0.7$ μm) has six identical fingers, each of which is 25.0 μm wide and 0.7 μm long. The ground–signal–ground contact pads were laid out for compatibility with RF probes. Inset: zoomed-in image of the channel region. **d**, MAG and $|H_{21}|$ values of self-aligned ZnO TFT versus frequency. Frequencies at 0 dB crossings show the f_{MAX} and f_T values.

zinc oxide TFTs that are fabricated with a self-aligned process that reduces parasitic capacitance and thus increases the maximum frequency of operation. With this LAE-based thin-film technology, we fabricate a phased array system operating at $f_0 = 982$ MHz .

Values of D/λ of LAE and device optimization

While the frequency of conventional LAE TFTs has been limited to tens of megahertz, in this work, TFT speed (f_{MAX}) of 2.7 GHz was achieved via a composite gate stack and by source/drain-to-gate self-alignment. A careful co-design of circuits and systems to take advantage of this high f_{MAX} enabled LAE operation to reach gigahertz frequencies. Given the standard industrial fabrication capability for LAE at the 10 m^2 scale, such LAE systems will reach a regime of high D/λ that is inaccessible to existing technologies, for example, Si-CMOS.

Figure 1a illustrates aperture sizes (D) and operating frequencies (c/λ) achievable by LAE and Si-CMOS technologies (c is the speed of light). The dashed black lines show the regimes of increasing D/λ attainable with the achieved TFT speed enhancement. Notably, in the UHF band from 430.0 MHz to 2.7 GHz, D/λ of 5–30 can be achieved by LAE, corresponding to a phased array with 10–60 elements at $\lambda/2$ spacing. In contrast to frequency bands above 10 GHz, where EM signals suffer from substantial attenuation in air[22], the UHF band is specifically of interest for broad applications in long-distance communication (cellular phones and satellites) and indoor metre-distance communication (wireless local area network and bluetooth communication). Further, the solid red line demarcates the boundary between the far-field regime (Fraunhofer region) and near-field regime (Fresnel region), at a radiation distance of 5 m (that is, $D^2/\lambda = 5$ m). Accessing the near-field regime affords additional geometric degrees of control, enabling rich radiation patterns; one example is the focusing on a point, as illustrated in Supplementary Fig. 1. Radiation distance of metres (for example, 5 m as illustrated above) is of particular interest because wireless communication/power delivery for healthcare and indoor IoT devices demands high spatial resolution on this scale[3–6,12]. Overall, enhancing the LAE speed, together with the existing trend of increasing physical dimensions, thus enables a unique design space for phased array systems.

High-frequency operation of LAE required for the phased array is achieved through device and circuit co-design. The frequency is fundamentally limited by the TFT speed metrics, that is, f_{MAX} and f_T. Most importantly, f_{MAX} determines the achievable oscillation frequency for EM excitation, and can be expressed by the following simplified expression:

$$f_{MAX} = \frac{1}{4\pi}\sqrt{\frac{g_m}{R_G(C_{GS}+C_{GD})C_{GD}}} = \frac{1}{4\pi}\sqrt{\frac{\mu_n(V_{GS}-V_T)}{R_G C_O W L L_{OV}(L+2L_{OV})}}$$

(ref. [49]), where μ_n is the electron mobility; R_G is the gate resistance; C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitance, respectively; C_O is the gate capacitance per unit area; V_{GS} is the gate-to-source bias voltage; V_T is the threshold voltage; and W, L and

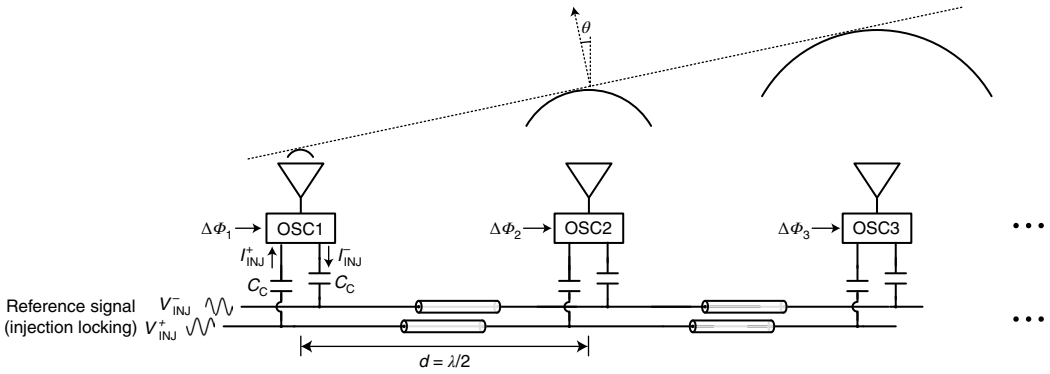

Fig. 2 | Architecture of the designed phased array system. The system consists of a linear array of antennas at $\lambda/2$ spacing. Each antenna is driven by a localized oscillator (OSC*i*) that generates a sinusoidal voltage signal as excitation. A differential reference signal ($V^{\pm}_{INJ}$) is coupled to each oscillator through a 50 Ω transmission line for injection locking. The phase of each oscillator is independently tuned, relative to the reference signal $\Delta\Phi_i$ ($i = 1, 2, 3,...$). As an example of operation, a far-field beam is steered to the direction of angle θ when $\Delta\Phi_i - \Delta\Phi_{i-1} = \pi\sin\theta$ ($i = 2, 3,...$).

L_{OV} are the channel width, channel length and gate–source/drain overlap, respectively. This suggests several factors that become the focus of our device design described next, namely, mobility, gate–source/drain overlap, gate resistance and channel width/length.

Low-temperature processing, necessary for large-area fabrication, produces semiconductors with high density of defect states in the bandgap, which trap and scatter charge carriers, leading to substantial degradation of mobility. The widely adopted transition of LAE technology from a-Si to oxide semiconductors, such as indium gallium zinc oxide[23,50], zinc oxide (ZnO)[45,51] and indium tin oxide[52,53] enhances mobility from approximately 1 to 10 $cm^2 (V s)^{-1}$, with various oxide technologies providing roughly similar mobility. As a representative technology, in this work, we employ ZnO and demonstrate device enhancements that are applicable to other technologies. Figure 1b shows the structure of the bottom-gate ZnO TFT employed, where the semiconductor (ZnO), gate oxide (Al_2O_3) and passivation (Al_2O_3) layers were deposited by plasma-enhanced atomic layer deposition[51] at 200 °C, and then lithographically patterned.

Even with the use of oxide semiconductors, TFT f_{MAX} and f_T have been limited to tens of megahertz[50,54,55], roughly four orders of magnitude lower than that of Si-CMOS transistors. To overcome this, we focus on reducing the large gate–source/drain overlap capacitance that results from conventional TFT processing. Typically, source/drain patterning employs a separate lithographic mask from gate patterning, which necessitates a large overlap margin (typically 5–20 μm) to avoid misalignment. As mentioned, while a handful of previous TFT demonstrations have achieved f_{MAX} above gigahertz values[44,46,47,52,53], these relied on processing not compatible with large-area electronics, such as electron-beam lithography, to pattern short channels and/or overlaps. To reduce the parasitic overlap capacitance while maintaining large-area compatibility, in this work, a self-aligned process was employed (Supplementary Fig. 2 provides a detailed illustration of the fabrication process)[45,54,56]. To pattern the source/drain region, ultraviolet (UV) exposure was applied from the bottom of the substrate, taking advantage of the high transparency of Al_2O_3 and ZnO thin films due to their wide bandgaps. In this manner, the transistor channel is defined by the gate metal itself, eliminating the misalignment associated with conventional non-self-aligned processing. The length of the channel is only slightly less than that of the gate electrode due to the diffraction of UV light, leading to minimal overlap between the gate and source/drain. With proper duration of UV exposure time, the overlap can be controllably reduced to 0.5 μm, as shown in the SEM image (Fig. 1b), without noticeably increasing the parasitic source/drain contact resistance. Sub-micrometre channel lengths (Fig. 1b) further reduce the gate capacitance and enhance the transconductance of the TFT.

To employ such self-alignment, a thick gate stack, namely, Cr/Al/Cr (25 nm/110 nm/40 nm), ensured effective blocking of the UV source (Fig. 1b). Importantly, this composite gate electrode, employing a low-resistance Al layer, also directly benefits f_{MAX} by reducing the gate resistance. To further reduce the gate resistance and enhance f_{MAX}, a multi-finger device layout was used (Fig. 1c), which shortens the effective gate electrode width and hence reduces the gate resistance. The resulting f_{MAX} and f_T were characterized by measuring the maximum available gain (MAG) and current gain (H_{21}) of the TFT via a vector network analyser (VNA), interfaced through high-frequency RF probes and compatible ground–signal–ground contact pad layout (Fig. 1c). The f_{MAX} (frequency corresponding to unity MAG) is 2.7 GHz (Fig. 1d), implying a speed boost of two orders of magnitude over conventional non-self-aligned LAE metal oxide TFTs with similar field-effect mobility of ~10 $cm^2 (V s)^{-1}$ (extracted from the transfer curve in Supplementary Fig. 3). The f_T (frequency corresponding to unity $|H_{21}|$) value is observed to be 566 MHz, similar to other recent demonstrations of self-aligned TFTs[56]. The f_T value is notably lower than f_{MAX}, exposing an important consideration in circuit/system design with LAE technology. While f_T is primarily dependent on the field-effect mobility and device geometry, f_{MAX} additionally depends on the resistance of the metal gate electrode, which—unlike the semiconductor—is not affected by the low process temperature. This will explicitly motivate LAE circuit architectures that are limited by f_{MAX} rather than by f_T.

System design of LAE-based phased array

Having boosted the fundamental performance metrics of LAE ZnO TFTs, thus enabling the potential for large D/λ, the design of a phased array system is pursued. A phased array is an array of antennas at $\lambda/2$ spacing, each of which is excited by a coherent sinusoidal signal with controllable phase. Although the fundamental performance enhancements enable LAE to achieve the required dimensions and frequencies, the design of microwave circuits and their integration in an architecture distributed over such dimensions poses critical challenges. First, key components, such as switches, amplifiers, phase shifters, etc., conventionally employ circuit topologies that are limited by f_T, or similar metrics and constituent parameters (further explained in Supplementary Fig. 7). As a result, they typically require an f_T that is orders of magnitude higher than the circuit operating frequency f_0. This would limit operation

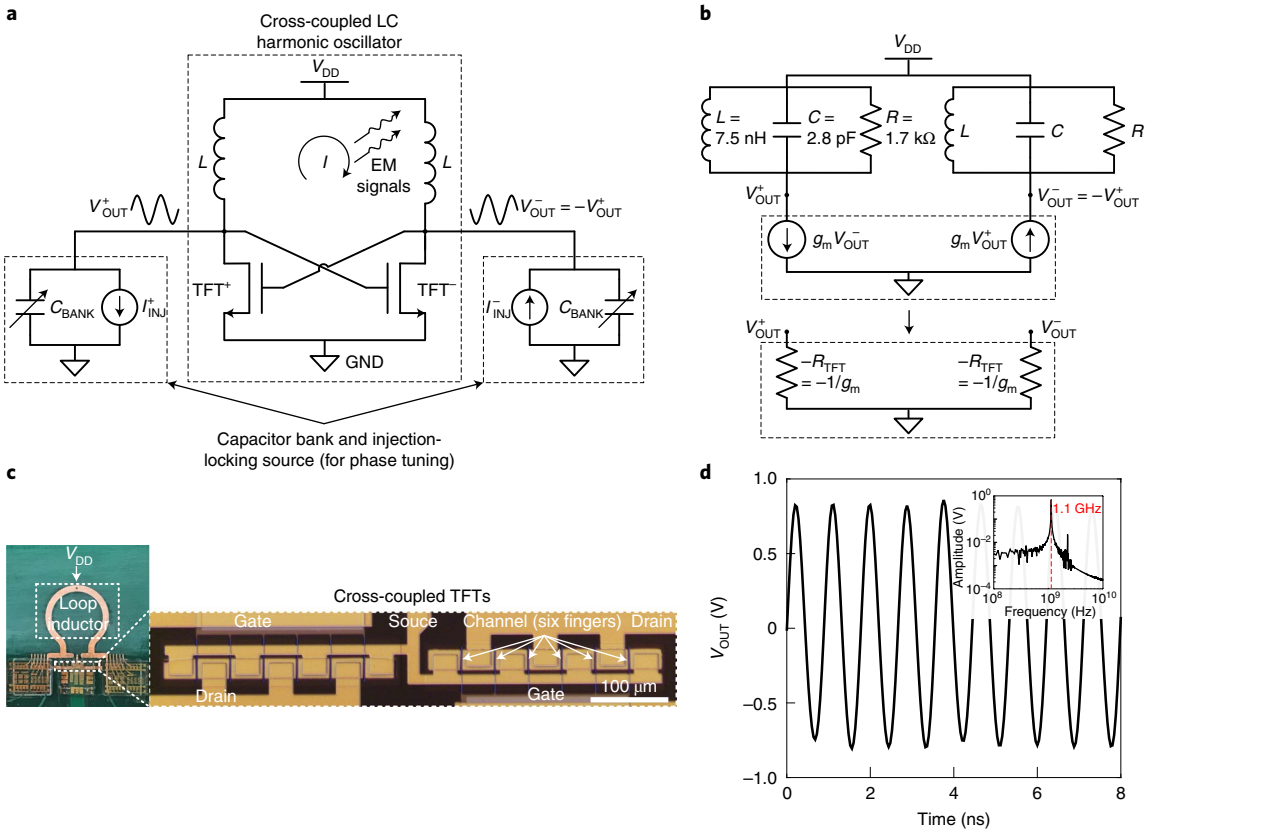

Fig. 3 | Gigahertz LAE-based oscillator with phase tunability. a, Circuit diagram of the cross-coupled LC harmonic oscillator with phase-tuning functionality. With the d.c. power supply provided (V_{DD}), the oscillator generates a differential sinusoidal voltage ($V^{\pm}_{OUT}$). The alternating current (I) in the inductors generates the EM radiation. Phase tuning is achieved by injection locking with a tunable capacitor bank (C_{BANK}; details shown in Fig. 4a,b). The design parameters are $L = 7.5$ nH, $W_{TFT} = 150.0$ μm and $L_{TFT} = 0.7$ μm. **b**, Equivalent circuit of the harmonic oscillator (without the tunable capacitor bank and injection-locking source for phase tuning). The capacitor (C) and resistor (R) in each network represent parasitic capacitances and losses, respectively (resulting from TFTs, inductors, metal routing and so on). To sustain oscillations, the cross-coupled TFTs provide a negative resistance ($-R_{TFT}$), which must compensate the losses represented by R. Details of extracting and analysing the network parameters are provided in Methods. **c**, Photograph of the oscillator. The inductor was implemented as a planar loop of a 35-μm-thick copper trace on a PCB, with 4.0 mm radius and 0.9 mm width, resulting in an inductance of 7.5 nH. The cross-coupled TFTs were fabricated on glass and wire-bonded to the PCB. Inset: microscopy image of the cross-coupled TFTs with $W_{TFT} = 150.0$ μm and $L_{TFT} = 0.7$ μm. **d**, Measured time-domain waveform at the output of the cross-coupled LC oscillator and its Fourier transform. The signal was captured by an oscilloscope (sampling rate, 25 GHz) at the oscillator output on the PCB via a voltage buffer. The Fourier transform of the time-domain signal shows an oscillation frequency of 1.1 GHz.

with LAE to tens of megahertz, well below that required in practical phased-array applications. Second, in conventional architectures, a single RF power source is often employed to maintain the coherence of distributed transmitted signals[1,11]. To do so, the required distribution network for RF power delivery raises concerns because of high losses and degraded signal integrity directly related to the transmitted power, which limits the feasible dimensions[57]. These issues are addressed at the circuit and architecture levels, as discussed below.

Figure 2 illustrates our system architecture. For each antenna, a localized oscillator was used for excitation. This addresses the substantial losses that would be incurred in distributing power from a centralized RF source to the radiating antennas across a large-scale phased array. However, individual oscillators require frequency synchronization for maintaining coherence and phase tuning to synthesize radiation patterns. These requirements are met by injection locking[58] via a differential reference signal ($V^{\pm}_{INJ}$) shared by all the oscillators. Injection locking serves two purposes: (1) it locks all the oscillators to a reference frequency, rather than allowing oscillations at their own natural free-running frequencies, which vary due to intrinsic device variations from fabrication; (2) it establishes a well-defined and tunable phase relationship between each oscillator and the reference signal ($\Delta\Phi_i$, $i = 1, 2, 3,...$) and hence a well-defined phase relationship among all the oscillators, thereby enabling the synthesis of radiation patterns. Importantly, as described below, the proposed injection-locking scheme employs a design approach that overcomes the challenges identified with a large-scale LAE-based phased array. First, it eliminates the need for f_T-limited devices. Instead, frequency locking and phase tuning were accomplished only using passive capacitors, whose fundamental performance metrics can be more readily addressed in LAE, compared with those of active devices or passive switches. Second, while injection locking requires distributing a high-frequency signal, the signal is for the synchronization of elements rather than directly distributing RF power for radiation, thus incurring much lower losses in the distribution network (further explanation in Methods).

Gigahertz LAE-based oscillator with phase tunability

The central components of the architecture are the phase-tunable oscillators, which serve as the distributed excitation sources. Figure 3a shows the circuit topology, consisting of a cross-coupled inductor (L) and capacitor (C) harmonic oscillator and a bank of tunable capacitors, with an injection-locking source for phase tuning.

The RF current in the inductor generates the EM signal with controllable phase for synthesizing the radiation patterns. The equivalent circuit of the inductor–capacitor (LC) harmonic oscillator without the phase-tuning functionality is shown in Fig. 3b, explicitly with a capacitor (C) and a resistor (R), representing the parasitic capacitances and losses in the system, respectively. To sustain oscillations, a feedback with a loop phase shift of 0° and gain larger than unity must be formed, which is achieved as follows: (1) a phase shift of 0° provided by resistor–inductor–capacitor (RLC) networks at their resonant frequency ($1/\sqrt{LC}$, the oscillator's natural frequency); (2) an effective negative resistance ($-R_{TFT}$) provided by the cross-coupled TFTs, which compensate the losses in the circuit (that is, when $|-R_{TFT}| < R$). These conditions establish a positive feedback loop that sustains oscillations at the natural frequency. The ability to sustain oscillations is thus measured by the ratio of the two resistances (R/R_{TFT}), which themselves depend on a number of operating and design parameters of the circuit devices, namely, frequency, inductance, capacitance, layout and phase-tuning circuitry. Especially for operation close to the f_{MAX} limit, there exists a critical tradeoff between the oscillation frequency and ability to sustain oscillations. Thus, a careful co-design of the circuit and devices was pursued. This exploited the ability to create high-quality-factor inductors in LAE, enabled by large geometries as well as low-loss planar traces and substrates[48,59]. Details of the design methodology as well as analysis of the parasitics are provided in Methods, and the resulting device parameters are provided in Fig. 3a,b.

LAE-based LC oscillators were thus demonstrated. Cross-coupled TFTs with $W_{TFT} = 150.0\,\mu m$ and $L_{TFT} = 0.7\,\mu m$ were fabricated on glass using the self-aligned process described above. Then, to enhance testability, a custom printed circuit board (PCB) with circuitry for power supply and signal monitoring was developed. On the PCB (Fig. 3c), the inductor was implemented as a planar loop of a copper trace with 4.0 mm radius and 0.9 mm width, resulting in an inductance of 7.5 nH (modelled by EM simulation; details provided in Supplementary Fig. 5). The TFTs on glass were diced and then directly wire-bonded to the PCB. In a mature industrial-scale fabrication process, the TFTs along with the inductor, as well as the whole phased array system, would be monolithically integrated onto a single substrate. With a direct current (d.c.) power-supply voltage of 6 V, the oscillator achieved a frequency of $f_{NAT} = 1.1$ GHz (Fig. 3d). To the best of our knowledge, this—also recently reported in ref. [48]—corresponds to one of the highest operating frequencies achieved by LAE-based TFT circuits.

As mentioned, in addition to generating gigahertz signals via the cross-coupled LC oscillators, a phased array also requires them to be a frequency-synchronized and phase-tunable system. Given the TFT frequency limitations, we devised an approach employing injection locking, a nonlinear effect that occurs in numerous physical systems[58]. When an oscillator is coupled to an external periodic signal (injection signal), the frequency of the oscillator shifts from its natural frequency to the frequency of the injection signal, provided the two frequencies are close enough to meet specific conditions. Injection-locking dynamics are well captured by Adler's equation[60], whose steady-state solution indicates a stable phase difference between the oscillator output and injection signal. The phase difference monotonically depends on the difference between the oscillator's natural frequency and injection-signal frequency. A phasor diagram illustrating this phase relationship is shown in Fig. 4a. Taking advantage of these dynamics, phase tuning of the oscillator was accomplished by controlling its natural frequency, which can be readily achieved via a bank of precisely tunable capacitors in parallel with the oscillator's RLC resonator (shown as tunable capacitor C_{BANK} in Fig. 3a). The advantage of this approach is that it avoids the use of TFTs as either f_T-limited active stages or passive switches, which would be problematic due to the TFT frequency limitations. As a result, using an injection current with a fixed amplitude and frequency, serving as a reference signal, injection locking results in the oscillator having the same frequency as the reference, but with controllable phase.

Therefore, as shown in Fig. 2, injection locking was realized by connecting the differential oscillator output to the shared differential reference signal ($V_{INJ}^{\pm}$) through two coupling capacitors (C_C). In the oscillator (Fig. 3a), to simplify the phase-tuning analysis, the injection (reference) signals are modelled as two current sources (I_{INJ}^{+} and I_{INJ}^{-}) by Norton equivalence ($I_{INJ}^{\pm} = j\omega C_C V_{INJ}^{\pm}$). As mentioned, a bank of tunable capacitors is needed in conjunction with injection locking for phase tuning. Figure 4b shows the implemented 4-bit digitally controlled and binary-weighted capacitor bank. The ith bit contains 2^i duplicates of a basic capacitance-tuning unit, which consists of a fixed-value capacitor (C_0), in series with a switchable TFT-based MOS capacitor (M_0), namely, a TFT as a two-terminal device with its source and drain shorted. The capacitor C_0 is used to decouple the d.c. bias from the LC oscillator. The MOS capacitor M_0 itself consists of a fixed extrinsic capacitance (due to fringing and overlap) between the gate and source/drain nodes. By raising the d.c. bias voltage at the gate, a conductive channel is induced in the n-type ZnO semiconductor. This results in an additional intrinsic capacitance. While traditional digitally controlled capacitor banks employ transistors as explicit switches in series with capacitors, such an MOS capacitor structure avoids the TFT f_T limitation that would be faced, enabling phase tuning at much higher frequencies. In addition to switching fidelity, losses introduced by the MOS capacitor also impact the ability to sustain oscillations. Compared with a traditional TFT switch, where current goes through its whole lossy channel, the MOS capacitor leads to reduced loss, as current tends to concentrate closer to the source and drain contacts, causing effectively shorter channel length and hence less resistive loss.

The bank was fabricated using the same process as for cross-coupled TFTs (Fig. 4c). The capacitor C_0 was implemented as a parallel-plate capacitor with a 40-nm-thick Al_2O_3 layer as the dielectric, sandwiched between two metal pads whose overlap was $3\,\mu m \times 3\,\mu m$. The MOS capacitor M_0 employed the same structure as a standard TFT with $W_{BANK} = 30\,\mu m$ and $L_{BANK} = 1\,\mu m$ having its source and drain shorted. Its high-frequency performance was characterized by a VNA. As shown in Fig. 4d, for the most significant bit, raising the d.c. bias voltage at the gate from −2 to 8 V causes a capacitance increase of 544 fF. This leads to an overall capacitance change of 115 fF from the capacitor bank, which is sufficient for phase tuning over 180° (as described Methods). At these two voltages (−2 V and 8 V), a high quality factor greater than 9.9 is maintained, from which the losses due to the capacitor bank can be derived. The losses must be considered for oscillator analysis and design; the analysis described in Methods shows that the capacitor bank leads to a tolerable 15% degradation in the condition required to sustain oscillations. Figure 4e shows the measured tunability achieved by an oscillator with the 4-bit binary-weighted bank, both in terms of capacitance change and phase (that is, ΔC and γ in Fig. 4a), under injection locking at $f_0 = 982$ MHz. The oscillator achieved an average phase-tuning resolution of ~13°, which can be further improved by adding more bits to the capacitor bank, if desired.

System demonstration

With phase-tunable oscillators, a three-element phased array operating at $f_0 = 982$ MHz was demonstrated. The prototype system and experimental setup are shown in Fig. 5a. The element components, including the oscillator TFTs, tunable capacitor banks, inductors and testing circuits, were integrated on PCBs and then mounted with 15 cm (~$\lambda/2$) spacing on a rotating rigid base. While all the necessary LAE components could be monolithically integrated, a heterogeneous approach to integration was adopted because of the following: (1) the substrate size with our cleanroom fabrication equipment is limited to 7.5 cm, making dicing of the circuits

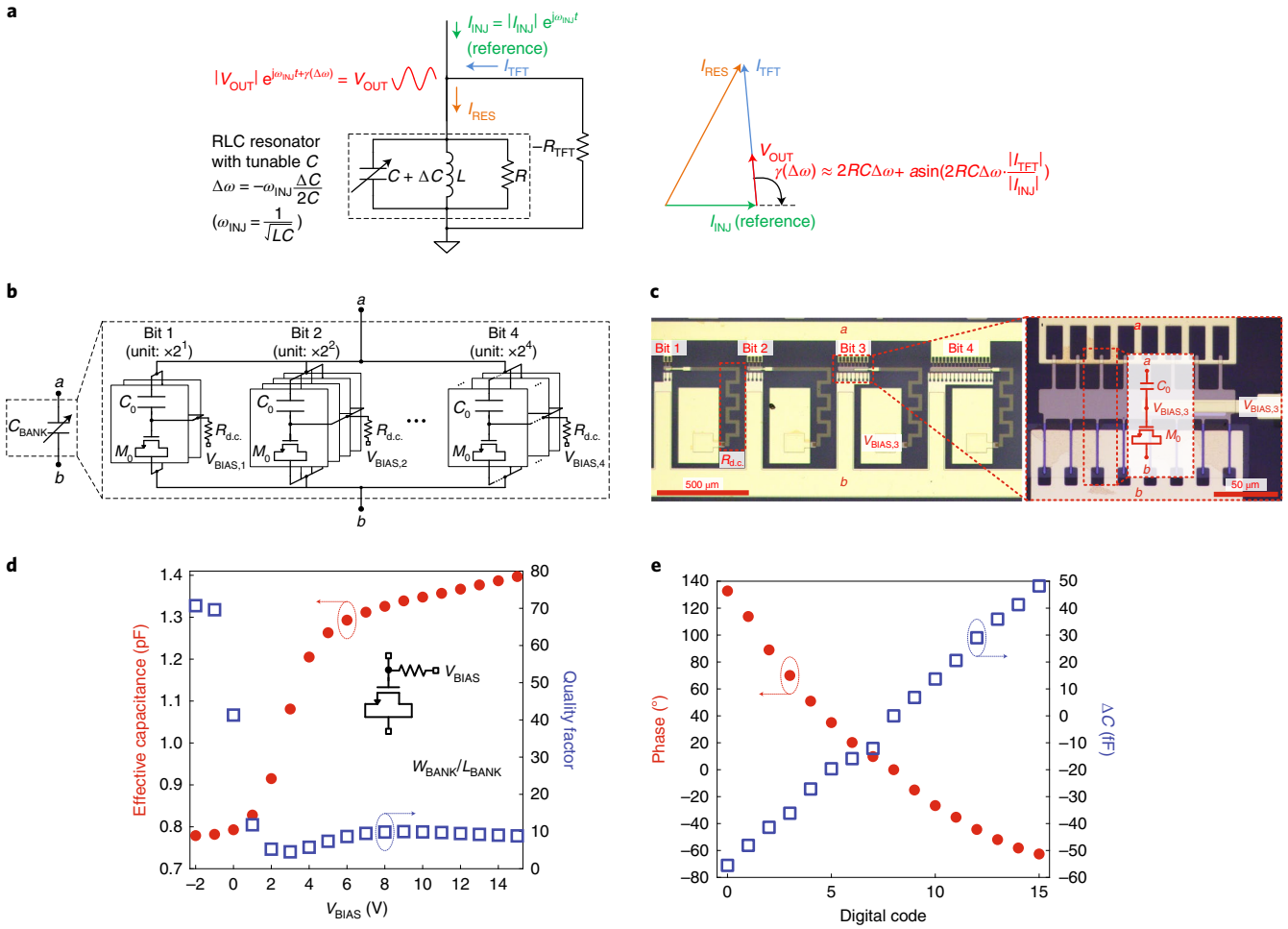

Fig. 4 | Phase tuning based on injection locking. a, Principle of the oscillator's phase tuning. Left: network showing the oscillator under injection locking, with the current and voltage at the output node labelled, where I_{INJ} is the injection current, I_{RES} is the current flow into the RLC resonator and I_{TFT} is the current flow out of the TFT. Right: phasor diagram showing the vector superposition of the three currents, yielding the resultant oscillator phase (γ), set by the difference ($\Delta\omega$) between the natural frequency of the resonator ($1/\sqrt{LC}$) and the frequency of the injection-locking signal, ω_{INJ}. As a result, the phase of the output voltage V_{OUT} is controlled by tuning the natural frequency via slightly varying the capacitance: $\gamma(\Delta\omega) = V_{OUT}(\Delta\omega) = 2RC\Delta\omega + a\sin(2RC\Delta\omega|I_{TFT}|/|I_{INJ}|)$, where $\Delta\omega(\Delta C) = -\omega_{INJ}\Delta C/2C$. **b**, The 4-bit, binary-weighted capacitor bank. The basic capacitance-tuning unit consists of a fixed capacitor (C_0), in series with a TFT-based MOS capacitor (M_0) having its source and drain shorted. Capacitance tuning is controlled by the gate bias voltage of the MOS capacitor, fed through a large resistor $R_{d.c.}$ (causing a cutoff frequency well below the oscillator operating frequency). The ith bit contains 2^i duplicates of such a unit. **c**, Microscopy image of the 4-bit, binary-weighted capacitor bank. Inset: zoomed-in image at the third bit, which consists of eight fixed capacitors (C_0) and eight MOS capacitors (M_0). The resistor $R_{d.c.}$ was implemented by a 10-nm-thick chrome trace. **d**, Measured capacitance of the MOS capacitor for the most significant bit (the fourth bit) and corresponding quality factor, versus the gate bias voltage (V_{BIAS}). The -2 V and 8 V bias points were chosen as the digitalized control-signal levels ($W_{BANK} = 2^4 \times 30\,\mu m$; $L_{BANK} = 1\,\mu m$). **e**, Measured change in capacitance (ΔC) and phase tuning of the oscillator (γ), controlled by the 4-bit digital code.

necessary for proper phased array element spacing; (2) for testing purpose, voltage regulators and high-speed buffers are included for probing intermediate signals.

To measure radiation patterns, a receiver antenna, followed by a low-noise amplifier, was fixed at a distance of 3.4 m (>10λ). Beamforming, a basic function of a phased array, was tested. For this, first, the phase of each oscillator i (i=1, 2, 3) was set by tuning its digital code, such that it satisfied $\Delta\Phi_i - \Delta\Phi_{i-1} = \pi\sin\theta$ within the precision provided by the 4-bit bank ($\Delta\Phi_i$ is the relative phase of the ith oscillator output, monitored through a high-speed buffer via the VNA and oscilloscope, using V_{INJ} as a reference). This yielded constructive interference in the direction of angle θ. Then, the magnitude of the radiated signal was measured at the receiver antenna as the array is rotated in steps of 1.8°. Details of the testing methodology are shown in Supplementary Fig. 4. The measured radiation patterns at θ=0°, 15°, –30° and 30° are shown in Fig. 5b–e, respectively, together with the simulation results assuming omnidirectional element antennas. Phased array operation is clearly achieved. Deviations in measurements from theory are found to be due to interferences from the cables used in the testing setup. Despite the use of electromagnetic interference (EMI)-shielding materials, the cables reflect/absorb the radiated EM signals, thus causing non-omnidirectional element radiation. We note that amplitude variations in the elements fluctuate somewhat across different steering angles; however, no apparent correlation is observed with an increasing angle. From the measured data, the half-power beamwidth for three θ values are extracted to be 30.6°, 32.4° and 37.8°. The theoretical half-power beamwidth for an array of omnidirectional antennas is $0.89/Nd\cos\theta$, which would result in corresponding values of 33.8°, 35.0° and 39.1°. The match between

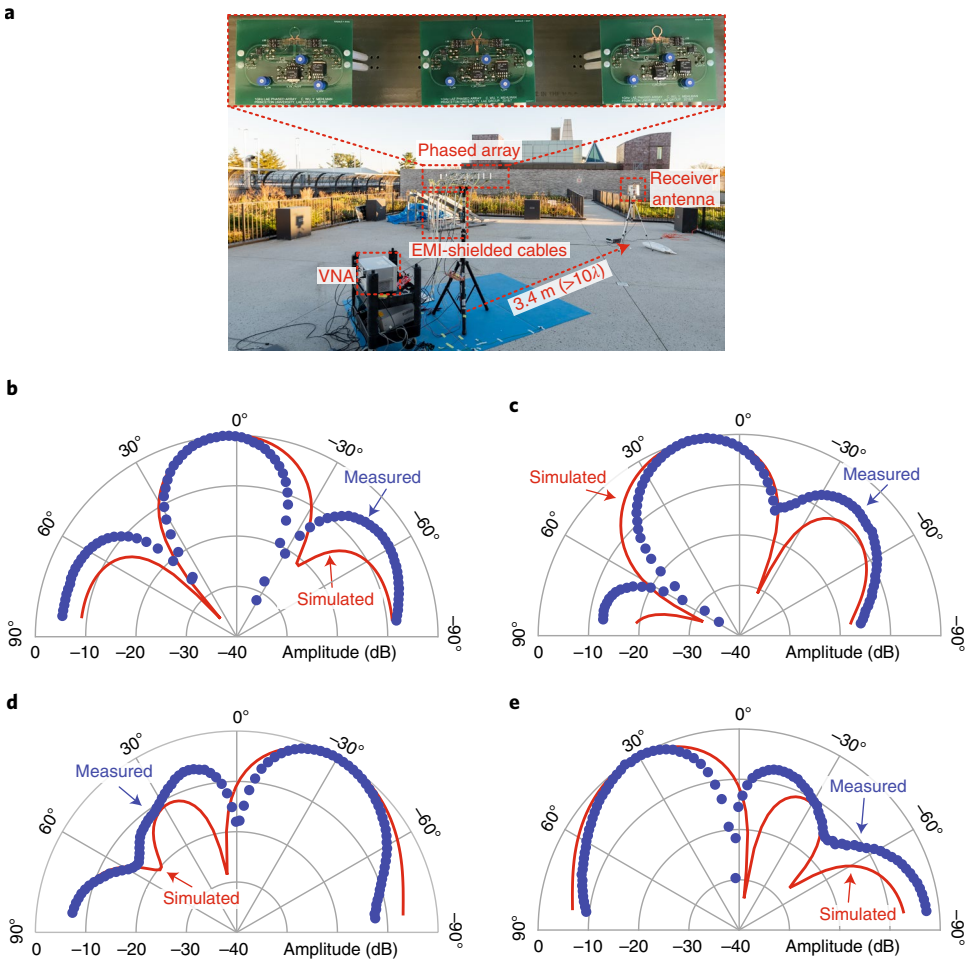

Fig. 5 | System demonstration. a, Photograph of the test setup; the inset shows the three-element phased array. The phased array was mounted on a rotating rigid base. The reference (injection-locking) signal was provided by the VNA. All the cables were coated with EMI-shielding materials to avoid near-field interference. The receiver antenna was placed 3.4 m away in the far field. The antenna output was followed by a low-noise amplifier with its output fed back to the VNA, and hence, the magnitude of the radiated signal from the phased array was measured. **b**, Measured and simulated far-field radiation pattern at $f_0 = 982$ MHz when the beam was steered to $\theta = 0°$. The element phases are measured to be $\Delta\Phi_2 - \Delta\Phi_1 = 9°$ and $\Delta\Phi_3 - \Delta\Phi_2 = -4°$ (ideally, $\Delta\Phi_2 - \Delta\Phi_1 = \Delta\Phi_3 - \Delta\Phi_2 = 0°$) due to the finite phase-tuning resolution, and the magnitude variation in each element is measured to be −0.38, −0.25 and 0.60 dB. **c**, Measured and simulated far-field radiation pattern at $f_0 = 982$ MHz when the beam was steered to $\theta = 15°$. The element phases are measured to be $\Delta\Phi_2 - \Delta\Phi_1 = 53°$ and $\Delta\Phi_3 - \Delta\Phi_2 = 42°$ (ideally, $\Delta\Phi_2 - \Delta\Phi_1 = \Delta\Phi_3 - \Delta\Phi_2 = 46.6°$) due to the finite phase-tuning resolution, and the magnitude variation in each element is measured to be 0.19, −0.09 and −0.10 dB. **d**, Measured and simulated far-field radiation pattern at $f_0 = 982$ MHz when the beam was steered to $\theta = -30°$. The element phases are measured to be $\Delta\Phi_2 - \Delta\Phi_1 = -88°$ and $\Delta\Phi_3 - \Delta\Phi_2 = -105°$ (ideally, $\Delta\Phi_2 - \Delta\Phi_1 = \Delta\Phi_3 - \Delta\Phi_2 = -90°$) due to finite phase-tuning resolution, and the magnitude variation in each element is measured to be −1.07, 0.83 and 0.14 dB. **e**, Measured and simulated far-field radiation pattern at $f_0 = 982$ MHz when the beam was steered to $\theta = 30°$. The element phases are measured to be $\Delta\Phi_2 - \Delta\Phi_1 = 95°$ and $\Delta\Phi_3 - \Delta\Phi_2 = 101°$ (ideally, $\Delta\Phi_2 - \Delta\Phi_1 = \Delta\Phi_3 - \Delta\Phi_2 = 90°$) due to finite phase-tuning resolution, and the magnitude variation in each element is measured to be −0.22, 0.57 and −0.38 dB. In the simulated pattern, the phase and magnitude variations are accounted for and ideal omnidirectional antennas are assumed.

measurement and theory (given the interference from cables) shows that beamforming was successfully achieved. As indicated in Fig. 1a, this demonstrated phased array function—along with the LAE's capability in spanning large physical dimensions—opens up a new regime of phased array operation with near-field focus at radiation distance on the scale of metres. The table in Supplementary Fig. 9 shows a comparison of the demonstrated system against other first-time/leading demonstrations in different technologies. Like Si-CMOS, LAE enables the monolithic integration conducive to broad applications and wide-scale deployment. Distinct from Si-CMOS, LAE does so by enabling applications in a previously unachievable frequency range (that is, gigahertz range, yielding lower loss in air for longer-range communication). LAE also enables the large near-field range required for rich radiation patterns at practical wireless distances.

This demonstration of basic phased-array operation in LAE paves the way for larger-scale systems. The feasibility of such scale up is further explored in Supplementary Fig. 8, by introducing the measured characteristics (including variations and losses) from elements into simulations.

Conclusions

We have reported an LAE-based phased array system that operates at microwave frequencies. This was achieved through the co-design of devices, circuits and system architectures. At the device level, we used self-aligned fabrication and a gate-electrode resistance reduction

technique to attain a high TFT f_{MAX}. At the circuit level, taking advantage of high-quality-factor planar inductors available in LAE, we developed an oscillator that can operate near the f_{MAX} limit at a frequency of f_{NAT} = 1.1 GHz. At the architecture level, we used injection locking to synchronize the frequency and tune the phase of the distributed oscillators, in a manner that overcomes the need for active stages or passive switches that are conventionally limited by f_T. Instead, injection locking allows phase tuning via the control of each oscillator's natural frequency, implemented by a switched capacitor bank comprising TFT-based MOS capacitors, which enable low losses at the required frequencies. With this co-design approach, we created a three-element phased array operating at 982 MHz.

Our approach could lead to conformal, wallpaper-like and monolithically integrated phased arrays with very large aperture sizes. Such systems could provide rich radiation-pattern control for emerging applications in aircraft surfaces, IoT and healthcare devices. They could also find near- and short-term applications within 5G/6G networks: first, in the 2.4 GHz low-frequency bands for high-specificity spatial addressing across many densely distributed sensor nodes, and then, in higher-frequency bands, for example, >5 GHz, enabled by ongoing technology progress on TFT feature-size and mobility scaling, for delivering high-bandwidth content across distributed devices.

Key areas for further development include the search for materials and devices that can provide higher TFT f_{MAX}, such as through mobility enhancement[42,43] and feature-size scaling[52,53], which could further increase the operating frequency and enhance the power efficiency of LAE-based phased arrays. A critical issue in improving TFT f_{MAX} is thermally induced power breakdown, limiting voltage and current biasing[61]. Further research on thermal dissipation mechanisms, especially with thermally insulating (glass or plastic) substrates, could lead to biasing for higher f_{MAX}. Research on mechanisms of electrostatic discharge damage in TFTs and mitigation approaches will also be essential, especially to enable robustness against transmission interconnect networks necessary for phased arrays of increasing dimensions.

In terms of circuits, the development of architectures to address device variability and beam-steering resolution is important. Within oscillators, topologies that employ regulated current biasing, for example, using tail TFTs, could enhance biasing, oscillation condition and phase stability. Within capacitor banks, adding additional capacitors for coarse and fine tuning could enable a reduction in element phase error to enhance beam-steering resolution. Finally, integrated calibration mechanisms, which monitor the element phase errors (arising due to drift, noise and device degradation) and provide automatic correction (a possible architecture is considered in Supplementary Fig. 7), will ultimately be necessary for robust deployment and use.

Methods

Analysis and design of LAE-based oscillator with phase tunability. The oscillator can be modelled as an RLC resonator in parallel with a negative resistor ($-R_{TFT}$) provided by the cross-coupled TFTs (a conceptual diagram is shown in Supplementary Fig. 6b).

The oscillation frequency is determined by the natural frequency of the resonator:

$$\omega = \frac{1}{\sqrt{LC}}.$$

When the losses of the oscillator, represented by R, are compensated by the negative resistor, a positive feedback with gain larger than unity is established, and oscillations continue indefinitely at the natural frequency. Hence, a term called the oscillation condition is defined to characterize whether oscillations are sustained:

$$\text{Oscillation condition} = R/R_{TFT}.$$

The design goal is to maximize the oscillation condition at a target frequency. To properly design the oscillator, the negative resistance and losses need to be analysed.

Negative resistance $-R_{TFT}$. As shown in Supplementary Fig. 6a, in a cross-coupled TFT pair, the negative resistance $-R_{TFT}$ is determined by

$$-R_{TFT} = -1/g_m.$$

where g_m is the transconductance of the TFT. Here g_m is extracted from the I_{DS}–V_{GS} transfer curve of the TFT, where I_{DS} is the drain-to-source current and V_{GS} is the gate-to-source voltage. Typically, a ZnO TFT with a channel length of 0.7 μm gives a g_m/W value of 12 μS μm^{-1} at $V_{GS} = V_{DS} = 6$ V, where W is the channel width and V_{DS} is the drain-to-source voltage (extracted from Supplementary Fig. 3).

Losses in the oscillator. There are three sources of loss: inductor (R_L), TFT resistance (R_{TFT}) and tunable bank resistance (R_{BANK}).

The inductor was implemented by a loop of copper trace on the PCB (Fig. 3c), with a radius of 4.0 mm, width of 0.9 mm and height of 35.0 μm. The loss is due to the finite conductance of the metal trace, which substantially suffers from the skin effect at microwave frequencies. The loop inductor was analysed using the High-Frequency Structure Simulator (HFSS) package—a finite element method solver for electromagnetic structures. The simulation (Supplementary Fig. 5a) results in an inductance of 7.5 nH and a self-capacitance of C_{IND} = 212 fF. To measure the loss caused by the inductor, the series resistance (due to both resistive and radiative losses) of 0.21 Ω is translated into a parallel resistance of $R_{L,P} = \frac{R_L^2 + (\omega L_{IND})^2}{R_L} = 10.6\,\text{k}\Omega$ at 1 GHz, where L_{IND} and R_L are the series inductance and resistance of the inductor, respectively. A circuit model of the loop inductor is illustrated in Supplementary Fig. 5b.

The loss in the TFTs is caused by the finite resistance of the gate electrode, R_G, and the drain-to-source output resistance in the saturation regime, r_0. R_G was minimized by using a thick composite gate stack (Cr/Al/Cr; Fig. 1b) and a multi-finger layout (Fig. 1c). The cross-coupled TFTs were designed with six identical fingers for overall values of W_{TFT} = 150.0 μm and L_{TFT} = 0.7 μm. For each 25-μm-wide TFT finger, a gate resistance of 0.5 Ω was measured, and the output resistance r_0 was extracted to be 1.7 kΩ from the TFT output characteristics (Supplementary Fig. 3). Hence, following the equivalent circuit for the cross-coupled TFTs (Supplementary Fig. 6a), at 1 GHz, the TFT contributes a resistive loss of $R_{TFT} = R_{G,P} || r_0 = \frac{1}{\omega^2 (2C_{GD} + C_{GS})^2 R_G} \| r_0 = 82.50\,\text{k}\Omega \| 1.70\,\text{k}\Omega = 1.67\,\text{k}\Omega$. Note that the TFT also contributes a capacitance of $C_{TFT} = 5C_{OV} + C_{OX} + C_{METAL} = 1.38$ pF (Supplementary Fig. 6a). Here $C_{GD} = C_{OV} = C_0 W_{TFT} L_{OV}$ is the capacitance due to the overlap between gate and source/drain, $C_{OX} = C_0 W_{TFT} L_{TFT}$ is the capacitance of the channel, C_{METAL} is the capacitance due to the overlaps between different metal layers in the layout. Also, $C_0 = \frac{\varepsilon_r \varepsilon_0}{t_{dielectric}} = \frac{8 \times 8.85 \times 10^{-12}\ \text{F m}^{-1}}{40\ \text{nm}} = 1.77 \times 10^{-3}\ \text{F m}^{-2}$ is the capacitance per area, where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of Al_2O_3 and $t_{dielectric}$ is the thickness of Al_2O_3, L_{OV} = 0.7 μm is the overlap length between the gate and source/drain (the horizontal length of the gate-to-source/drain overlap as shown in Fig. 1b, in addition to the vertical sidewall of the gate electrode), W_{TFT} = 150.0 μm is the channel width and L_{TFT} = 0.7 μm is the channel length.

The basic capacitance-tuning unit consists of a fixed parallel-plate capacitor in series with a tunable MOS capacitor (Fig. 4b,c). The impedance of the MOS capacitor was measured (Fig. 4d) and bias voltages of −2 V and 8 V were chosen as the digitalized operating points because they (1) offer adequate capacitive change for phase tuning and (2) exhibit a fairly high quality factor, indicating the low loss required to ensure that the oscillation condition is met. The worst case of oscillation condition happens when all the MOS capacitors are biased at 8 V. Using the model parameters summarized in Supplementary Fig. 6c, the binary-weighted bank contributes a resistive loss of $R_{BANK} = 2^{-1} \times 255.5\,\text{k}\Omega \| 2^{-2} \times 255.5\,\text{k}\Omega \| 2^{-3} \times 255.5\,\text{k}\Omega \| 2^{-4} \times 255.5\,\text{k}\Omega = 8.5\,\text{k}\Omega$ and a capacitance of $C_{BANK} = 2^1 \times 19.0\,\text{fF} \| 2^2 \times 19.0\,\text{fF} \| 2^3 \times 19.0\,\text{fF} \| 2^4 \times 19.0\,\text{fF} = 629.2\,\text{fF}$ to the oscillator.

Oscillation condition. Hence, combining all the sources of losses above, the total resistance R is 10.60 kΩ ‖ 1.67 kΩ ‖ 8.50 kΩ = 1.23 kΩ. Thus, for our design, the oscillation condition is $g_m R = 12\,\mu\text{S}\,\mu\text{m}^{-1} \times 150\,\mu\text{m} \times 1.23\,\text{k}\Omega = 2.2$, which is larger than unity. Therefore, the oscillation condition is met. For a reference, without the bank, the oscillation condition would be $g_m(R_L \| R_{TFT}) = 2.6$. Thus, the bank degrades the oscillation condition by 15%.

In addition, all the components contribute to an overall capacitance of $C_{TOTAL} = C_{IND} + C_{TFT} + C_{PAR} + C_{BANK} = 0.2120\,\text{pF} + 1.3800\,\text{pF} + 1.2500\,\text{pF} + 0.6292\,\text{pF} \approx 3.500\,\text{pF}$, where C_{PAR} is the parasitic capacitance from the coupling between the metal traces in the layout. Therefore, the operating frequency is

$$f_0 = \frac{1}{2\pi\sqrt{LC_{TOTAL}}} = 982\,\text{MHz}.$$

(Without the capacitor bank, the natural frequency of the oscillator would be $f_{NAT} = \frac{1}{2\pi\sqrt{L(C_{IND} + C_{TFT} + C_{PAR})}} = 1.1\,\text{GHz}$.)

Note that, in principle, the oscillator can oscillate at frequencies higher than 1 GHz. However, a tradeoff exists between frequency and the oscillation condition.

Here 1 GHz was chosen as the operating point because it offers a reasonable margin for the oscillation condition, as shown above.

Impact of device variations. Variations in the TFT parameters (that is, threshold voltage, mobility and capacitance) impact the oscillator characteristics.

Variations in threshold voltage and mobility affect g_m and hence the oscillation condition (g_mR). This will require a fully integrated phased array to set the d.c. power supply (that is, V_{DD}; Fig. 3a) with adequate margin against the worst-case condition of g_m in the oscillator TFTs.

An additional impact is on the phase of the oscillators. As described in Fig. 4a, phase tuning depends on the current magnitude and configured bank capacitance: $\gamma(\Delta\omega) = V_{OUT}(\Delta\omega) = 2RC\Delta\omega + a\sin(2RC\Delta\omega|I_{TFT}|/|I_{INJ}|)$, where $\Delta\omega(\Delta C) = -\omega_{INJ}\Delta C/2C$. Variations in the TFT threshold voltage and mobility affect $|I_{TFT}|$, and variation in TFT capacitance effectively offsets ΔC, which impacts the phase of the oscillators. In practice, two approaches can be applied to address this issue: (1) a bank capacitor with redundant bits can be employed to fine-tune the TFT capacitance and compensate the offset ΔC back to zero; (2) an integrated calibration mechanism can be embedded in the synchronization network to actively cancel out the phase-tuning error (possible calibration architecture is presented in Supplementary Fig. 7).

Design of transmission line for the injection-locking signal. The demonstrated phased array architecture involves localized RF power generation via distributed oscillators, rather than the distribution of RF power from a centralized RF generator. This enhances phased array scalability over large dimensions by reducing power loss in the distribution network. As mentioned, the distribution of an injection-locking signal is required for the synchronization of the oscillators. Because this signal does not directly provide the radiated power (while localized oscillators do), its power loss can be made small through proper design. Specifically, the power loss is determined by the injection-signal voltage V_{INJ} required for phase control of the oscillator voltage, which is distributed via a 50-Ω-terminated transmission line (Fig. 2). By Thevenin-to-Norton source transformation, $V_{INJ} \approx I_{INJ}/j\omega C_C$, with a transmission-line impedance (50 Ω) much smaller than the coupling-capacitor impedance of $1/j\omega C_C$. I_{INJ} is determined by the term $\gamma(\Delta\omega) = 2RC\Delta\omega + a\sin(2RC\Delta\omega|I_{TFT}|/|I_{INJ}|)$, where γ is the phase of the oscillator voltage, as shown in the phasor analysis (Fig. 4a). Thus, to achieve the desired γ, $|I_{INJ}|$—and correspondingly $|V_{INJ}|$—can be reduced by reducing $\Delta\omega$ (difference between the oscillator's natural frequency and injection-signal frequency). This can be readily achieved by reducing the unit capacitance of the capacitor bank. For example, feasible values of $I_{INJ} = 10\,\mu A$ and $C_C = 100\,fF$ lead to V_{INJ} of just 15.9 mV. This corresponds to a capacitance change of 59 aF from the basic bank unit, which can be directly implemented or by fabricating series combinations of larger unit capacitances.

The reference signal is thus distributed using a single 50 Ω transmission line, with taps feeding each oscillator through a coupling capacitor ($C_C = 100\,fF$). The coupling-capacitor impedance converts the voltage of the reference signal into an injection current. Sharing the transmission line in this way can result in coupling/pulling between the oscillators, causing the phase of one to affect that of the other. This was avoided by making the impedance seen by the transmission line looking into the coupling capacitor (C_C) much larger than the 50 Ω impedance of the transmission line itself: $\left|\frac{1}{j\omega_{INJ}C_C}\right| = 1.59\,k\Omega \gg 50.00\,\Omega$. Thus, the current drawn by the oscillators is a small portion of the current running through the transmission line. This ensures a minimal effect of the injection currents on the overall current in the transmission line. While providing the injection current through a buffer would also eliminate coupling, such a buffer circuit would be limited by f_T, restricting the operating frequency with TFTs. Encouraging results on increased electron mobility in oxide TFTs[42,43], combined with speed-enhancement techniques discussed in this work, are expected to enable LAE-based voltage buffers operating in the gigahertz regime.

Data acquisition and power-supply circuits. The voltage waveforms of the oscillators were acquired via a buffer circuit integrated on the element PCBs (TI LMH6559 chip). An oscillator voltage was coupled to the buffer through a small (50 fF) capacitor to minimize loading effects on the oscillator. The buffer output was then coupled to an oscilloscope or VNA via a capacitor with a 50 Ω termination resistor for transmission-line impedance matching. For d.c. power supplies to the oscillators (that is, V_{DD}; Fig. 3a), low-dropout voltage regulators (LT1764A, Linear Technology) were used, with a potentiometer to tune the d.c. output voltage relative to the 1.21 V reference voltage generated by the low-dropout voltage regulators. Both buffer and voltage regulator circuits were designed according to the manufacturer datasheet, with minor modifications to satisfy our system requirements.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Received: 31 March 2020; Accepted: 25 August 2021;
Published online: 7 October 2021

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Acknowledgements

This work was supported in part by Center for Brain-Inspired Computer (C-BRIC), one of the six centres in JUMP sponsored by DARPA, under grant number 40001859-075 (N.V., C.W., Y. Ma and P.K.), and by Princeton Program in Plasma Science and Technology (PPST) (J.C.S. and Y. Mehlman). This work also utilized the Princeton Institute for the Science and Technology of Materials (PRISM) cleanroom facilities. We thank S. Venkatesh from Princeton University for the helpful discussions.

Author contributions

N.V., J.C.S. and C.W. conceived the idea of the LAE-based phased array and experiments. N.V., J.C.S. and S.W. supervised the project. C.W. and Y. Mehlman designed, fabricated and performed the measurements of the LC oscillators. Y. Mehlman fabricated and characterized the devices. Y. Ma characterized the material. C.W. designed and prototyped the phased array circuits/systems, and performed the measurements together with Y. Mehlman, P.K., T.M. and H.J. C.W. wrote the manuscript with the help of N.V., S.W. and J.C.S. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-021-00648-z.

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Peer review information *Nature Electronics* thanks George Kyriacou and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

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