Laboratory Capabilities; 2

The Department of Energy's weapons labs (Sandia National Laboratories, Lawrence Livermore National Laboratory, and Los Alamos National Laboratory) and the Department of Commerce's National Institute of Standards and Technology (NIST) offer potential for improving the competitiveness of U.S. semiconductor manufacturers and their suppliers. All four labs have developed strong competencies in areas the Semiconductor Industry Association (SIA) has identified as critical to the future success of the U.S. semiconductor industry, such as lithography, modeling and simulation, environmental safety and health, and equipment design. In 1993, the four labs devoted resources valued at approximately $115 million to cooperative research and development agreements (CRADAs) with the commercial semiconductor industry.

At present, the labs' work with industry is fragmented, consisting of numerous small projects that build upon the capabilities of individual researchers or research groups. However, each of the labs appears to have strong capabilities in particular subjects that could become focal points of their efforts to support the commercial semiconductor industry. NIST is clearly the leader in most areas of metrology; Sandia has particular capabilities in equipment modeling and design, as well as in contamination-free manufacturing; Los Alamos is strong in both the modeling of semiconductor devices, manufacturing processes, and complete factories, and in environmental safety and health; Lawrence Livermore has particular expertise in soft x-ray lithography and materials processing. Already, the labs are beginning to pursue leadership roles in some areas and coordinate their research with the other labs, industry, and universities.

Integrating the labs more closely with industry will not be easy, though. DOE labs are new to commercial missions and do

not operate with the same cost considerations or time horizons as commercial companies. Such cultural differences are likely to cause frustration in joint R&D programs between industry and the labs. Industry has already found negotiating CRADAs with DOE labs slow and laborious. In addition, the labs have only limited experience with the most advanced commercial practices for manufacturing integrated circuits (ICs). While Sandia has manufactured ICs for defense applications and NIST has provided support in metrology (the science of measurement) to the commercial IC industry for several decades, the labs as a whole have not been operating on the leading edge of commercial IC production. Los Alamos and Lawrence Livermore boast strong capabilities in simulation and modeling, but do not have extensive experience applying these strengths to commercial semiconductor processes and factories. It may therefore take some time before their contributions to commercial industry become evident in the marketplace.

LABORATORY/INDUSTRY COLLABORATION

Both the DOE weapons labs and NIST offer significant, and complementary, capabilities to aid the U.S. commercial semiconductor industry, While these are not the only federal laboratories with capabilities of interest to the semiconductor industry, they are, for several reasons, the labs most likely to contribute to commercial missions in the near term. First, with the decline in nuclear weapons work, the DOE labs may be given new missions to assist commercial industry through technology transfer and cooperative research and development,[1] They are already being encouraged to work more closely with industry through CRADAs. Second, NIST has a long history of working with industry to develop and disseminate new standards and measurement methods. In the last decade, NIST has been given new responsibilities to support manufacturing extension programs and commercial technology development.

DOE Labs

The Department of Energy Defense Program Laboratories (or weapons labs) were created to develop nuclear weapons technology. In fulfilling this mission, the weapons labs developed diverse science and engineering capabilities for producing, testing, and ensuring the safety of the nation's nuclear deterrent. These capabilities, which include specific competencies in physics, chemistry, materials science, engineering, and computer science (box 2-A), now form the basis of the DOE labs' ability to help improve U.S. industrial competitiveness in the semiconductor industry.

The weapons labs have experience in nearly all stages of technology development, with the notable exception of full-scale commercial production. The labs invented a complete design and manufacturing process, beginning with detailed nuclear and atomic physics and extending through systems integration, for both the nuclear and non-nuclear components of the weapons systems. Each of the labs played a specific role in the process. Los Alamos and Lawrence Livermore were chartered to understand the physics of nuclear devices and to develop materials technology in support of the weapons program. Sandia National Labs was directed to develop the science and engineering skills required for the non-nuclear portion of nuclear weapons systems, including custom and radiation-hardened ICs and other electronics.

The weapons labs may be best-suited to address research problems that are in the middle of the development cycle-between basic research and product development—and that com-

[1]Two bills currently under consideration in Congress, H.R. 1432 and S.473, direct the DOE labs to work more closely with industry. The House bill restricts DOE to missions in nuclear weapons, defense, energy, and environmental remediation, but encourages greater technology transfer and cooperative R&D. Tbe Senate bill includes a broader mission statement that explicitly charters the labs to conduct programs of industrial R&D.

Box 2-A—Core Competencies of DOE Weapons Laboratories

Lawrence Livermore

Applied physics, chemistry, and materials science
- Plasma, solid-state, and atomic physics and chemistry
- Synthesis and processing of metal and alloys, ceramics, and organics
- Surface science and processing, adhesion and bonding, microstructural science
- Chemical kinetics and synthesis
- Superconductivity, materials and mechanisms
- Nuclear chemistry
- Materials characterization via synchrotrons radiation, accelerator mass spectrometry, electron and scanning microscopy, positron spectroscopy, etc.

Measurements and diagnostics
- Plasma and high-temperature diagnostics
- Surface diagnostics
- Sensors and detectors
- Data capture, analysis, fusion, and control
- Process monitoring and control
- X-ray micro- and macro-tomography

Computational science and engineering
- Modeling of solids, fluids, atomic structure at micro and macro scales, under normal and extreme conditions
- Constitutive models for complex materials processing
- Quantum chemistry, lubrication and bio-molecules on surfaces
- EM circuit and electro-optic device design
- Electricity and magnetism in 3-dimensional Maxwell's equations solvers with complex boundary conditions
- Scientific visualization
- Imaging and signal processing

Microelectronics and photonlcs
- High-density, high-performance chip packaging (multichip modules)
- High-speed electrical and optical data transmission
- Materials and systems reliability
- Band-gap engineering and verification
- Gas immersion laser doping (GILD)
- Display technologies
- High-speed electromagnetic and optical circuit modeling, test, and diagnostics

Lasers, optics, electro-optics
- Soft x-ray lithography systems: x-ray sources, optics, and materials
- High-power/high-radiance solid-state lasers
- High-power semiconductor laser arrays
- Optoelectronics design and development
- High-power optical fiber transport
- Laser processing of materials

Manufacturing
- Precision engineering
- Metrology
- Advanced design and process engineering
- Computed tomography and ultrasound
- Non-destructive evacuation

Engineered materials and processes
- Modellng, production, and metrology of multi-layer and epitaxial materials
- Advanced low- and high-dielectric materials
- Atomic, ionic, particle, and photon beam materials processing and modeling
- Plasma processing-modeling and validation of processing methods
- Aerogels, zerogels, and solgels
- Microstructure: microchannel coolers, actuators, sensors, and micro instruments
- Molecular dynamic modeling of machined and deposited microstructure

Atmospheric and geosciences
- Seismology and imaging
- Geochemistry
- Global climate and transport modeling
- Transport measurements, atmospheric chemistry

Defense sciences
- Nuclear system design
- Scientific computing of massive problems with disparate time and distance scales
- Energetic materials and conventional munitions
- Nuclear measurements and design validation under extreme conditions

Blosclence/Biotechnology
- Genomics
- Physical biology
- Analytical cytology
- Synthetic and natural biomaterials sciences
- Micro-instruments and sensors

Environmental science and technology
- U.S. and California compliance and remediation expertise
- Measurements and sensors
- Remediation technologies
- Process developments
- Bio, chemical, and radiation dosimetry

(continued on next page)

Box 2-A–Core Competencies of DOE Weapons Laboratories-Continued

Sandia

Microelectronics and photonlcs
- IC design, fabrication, and test
- Advanced lithography
- Reliability physics and engineering
- Advanced packaging
- Compound semiconductor and strained-layer semiconductor technology
- Optoelectronics and photonics
- Lasers, laser arrays, and associated technology
- Compound Semiconductor Research Laboratory

Engineered materials and processes
- Synthesis and processing of metals, ceramics, and organics
- Characterization and analytical technique development
- Theory, simulation and modeling of materials and processes
- Melting, casting, and joining
- Chemical vapor deposition and plasma deposition
- ion beam processing and analysis

Pulsed power
- intense particle beam physics
- High-speed switching
- Intense x-ray physics
- Radiation effects simulation
- Plasma and electromagnetic theory and application

Physical simulation and engineering sciences
- Combustion sciences
- Geological sciences
- Experimental mechanics
- Solid and structural mechanics
- Radiation transport and above-ground radiation testing
- Diagnostics and instrumentation
- Fluid and thermal sciences
- Nondestructive evaluation
- Environmental testing and engineering
- Research reactor engineering and experimentation

Computational simulation and high-performance computing
- Massively parallel computing
- High-performance scientific computing
- Quantum chemistry and electronic structure
- Computational hydrodynamics, mechanics, and dynamics
- Digital communications and networking
- information surety
- Development and application of intelligent machines
- Signal processing

plement the R&D capabilities of industry and universities. The labs have the capabilities and the facilities necessary to conduct applied research programs and to develop prototypes of new systems for demonstration/validation purposes. This is a mission that industry has slowly retreated nom, universities have not yet ventured into, and government rarely supports,

Each of the labs has managed and executed large-scale programs requiring large facilities, high levels of funding, and multidisciplinary scientific expertise. Together, the labs managed an operational budget of $3.4 billion and employed almost 25,000 people in 1993. Their technical staffs employ more than 11,500 workers, over one-third of whom hold Ph.D. in fields such as physics, chemistry, engineering, mathematics, and computer science (figure 2-l).

Furthermore, the weapons labs are gaining experience in working with industry. Since 1989, all DOE labs have begun programs of cooperative R&D with industry. Though implementation of CRADAs has been slow and frustrating, the three weapons labs had signed 179 CRADAs as of May 1993, totaling over $235 million of in-kind laboratory contributions.[2] Many of these agree-

[2] U.S. Congress, Office of Technology Assessment, *Defense Conversion: Redirecting R&D,* OTA-ITE-552 (Washington, DC: U.S. Government Printing Office, May 1993), pp. 104-105.

Box 2-A—Core Competencies of DOE Weapons Laboratories-Continued

Los Alamos

Nuclear technologies
- Nuclear weapons design
- Reactor design and safety analysis
- Nuclear medicine
- Nuclear measurements

High-performance computing and modeling
- Global environment (climate change, etc.)
- Computational test bed for industry
- Massively parallel processing
- High data rate communication
- Traffic modeling
- Visualization

Dynamic experimentation and diagnostics
- Arms control/verification
- Global environment
- Neutron scattering
- Measurement of explosive phenomena
- Light detection and ranging for atmospheric measurements

Theory and complex systems
- Human genome
- Traffic simulation
- Neural networks
- Non-linear phenomena

Advanced materials and processing
- Plutonium processing
- Manufacturing process analysis
- Materials modeling (material by design)
- Polymers
- Ceramics
- Metallics
- Composites

Beam technologies
- Accelerator transmission of waste
- Laser diagnostics
- Materials characterization
- Photonics
- Photolithography (x-ray sources)
- Neutron beam chemistry and physics

Systems engineering and rapid prototyping
- Transportation systems
- Environmental and energy systems analysis
- Lasers manufacturing
- Accelerator systems

SOURCE: Lawrence Livermore National Laboratory, Livermore, CA; Los Alamos National Laboratory, Los Alamos, NM; Sandia National Laboratories, Albuquerque, NM.

ments cover R&D in fields related to semiconductor technology.

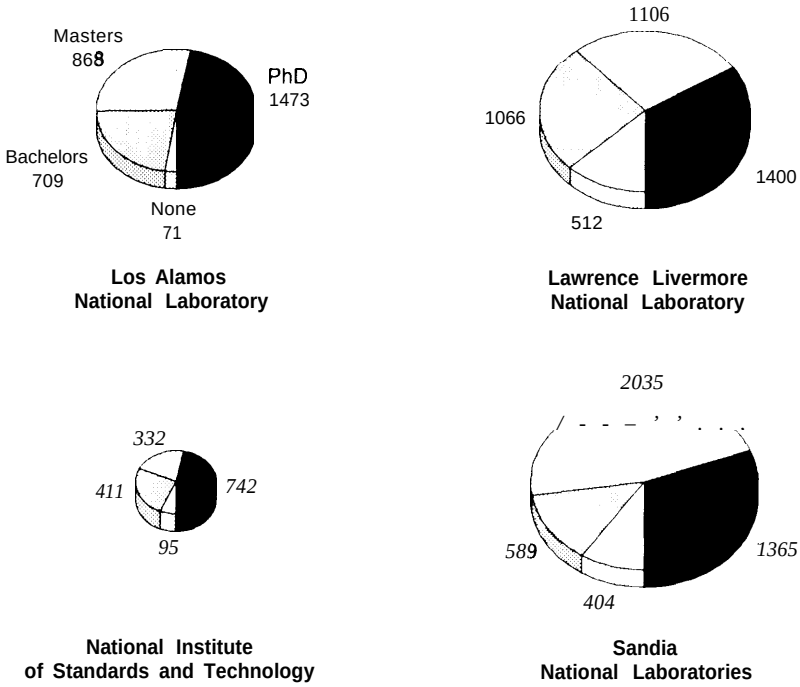
With declining defense budgets, the labs may be able to dedicate more of their resources to nondefense problems. Already, the portion of their budgets directed to defense has fallen. In 1993, defense activities at Los Alamos comprised 71 percent of its total operating budget, compared with 78 percent in 1987; at Lawrence Livermore, defense activities dropped to 67 percent, down from 76 percent in 1988; and at Sandia, defense activities have declined from 87 percent to 78 percent since 1989. Despite these changes, the labs' combined operating budgets remained constant (in real dollars) during this period,[3]

NIST

Originally founded in 1901 as the National Bureau of Standards, NIST is the national custodian of the fundamental units of measurement. Measurements developed at NIST rest on the most secure metrological foundation possible in the United States and, in many cases, anywhere in the world. NIST is legally designated to function as the lead national laboratory for providing the measurements, calibration, and quality assurance

[3] Ibid, p. 83.

Figure 2-l—Professional Staff of DOE Weapons Labs and NIST by Degree



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 27.

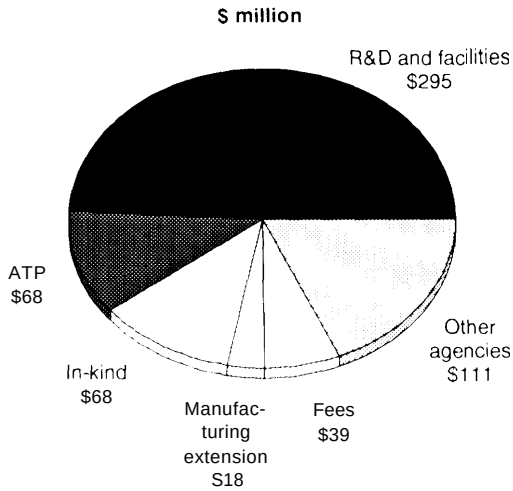
techniques that underpin U.S. commerce. Among other activities, NIST represents the United States in international affairs having to do with weights and measures, provides technical advice and consultation to other parts of the government, and cooperates with the private sector in the development of voluntary standards. NIST has developed or improved a large fraction of the measurement methods used daily by the semiconductor industV .

NIST's mission was expanded in the Omnibus Trade and Competitiveness Act of 1988 to give it a greater role in stimulating U.S. industrial competitiveness. NIST now operates a growing number of manufacturing extension centers (nine as of 1993) that bring best-practice manufacturing methods to small and medium-sized business. MST also manages the Advanced Technology Program, which provides cost-shared R&D grants to companies and other institutions developing critical commercial technologies. These extramural programs have grown from $6 million in 1988 to $86 million in 1993.

NIST is smaller than the DOE weapons labs, with a total staff of about 3,200, approximately 1,600 of whom are on the technical staff and 800 of whom hold Ph.D. degrees. NIST had a total budget of $599 million in 1993 (figure 2-2). Congress appropriated two-thirds of this total: $295 million to support MST's intramural research program and construction of new facilities, and $86 million to support ATP and the manufacturing extension centers. The remainder of NIST's budget came from outside sources: other federal agencies that support research at MST; in-kind contributions of staff and equipment from companies conducting joint research with NIST; and fees from companies using agency facilities or purchasing standard reference materials.

NIST's operating budget is likely to grow significantly in the next four years. The Clinton administration plans to shift federal R&D priori-

Figure 2-2—NIST Funding By Source, 1993



SOURCE: National Institute of Standards and Technology, "General Information About NIST," briefing to OTA, March 15, 1993.

ties away from defense and toward commercial problems. NIST has been targeted as a key player in a larger civilian effort; its budget may grow by a factor of four, to $1.7 billion, by 1997, ATP would receive the largest proportional increase, growing from $68 million in 1993 to $730 million by 1997.

Unlike the DOE weapons labs, which have only recently been chartered to collaborate with and support commercial industry, NIST has long had an industrial mission. In its work with the semiconductor industry, NIST not only supports performance specifications and operation of advanced manufacturing tools, but also provides the standards and metrology required to assure the purity and composition of materials used in manufacturing.

NIST's intramural research occupies a unique niche in the nation's infrastructure. Most companies do only enough measurement work to solve specific problems. Academic attention to measurement problems is limited. Many measurement problems cannot be broken down into small enough pieces for a student to solve in the course of a graduate program. Furthermore, in the United States, there is little perceived professional glamour in most metrological issues, so professors usually pursue other topics.

NIST has earned a worldwide reputation for impartiality and technical excellence. Its competencies in metrology span a number of disciplines (table 2-l). The efficiency of solving a measurement problem once at NIST and then disseminating the results throughout the whole industry, rather than each company performing the job independently for itself, provides outstanding leverage for NIST's metrological development. Examples studied in the semiconductor field have been estimated to have benefit-to-cost ratios ranging from 5:1 to over 100: 1.[4]

NIST produces measurement systems and prototype instruments as a byproduct of its work and initiates few projects to develop measurement hardware. Metrological programs are not like system development projects in which the end products are often the only useful results. Most NIST projects are conducted in cooperation with outside companies or laboratories, and the continuing interaction between the staffs of NIST and its collaborators transfers useful technology steadily as the work progresses. Information--not hardware-is the usual product. Project objective, organization, and size, staff operating techniques, and the types of deliverables are qualitatively different from those at DOE labs.

SEMICONDUCTOR PROGRAMS AT THE FOUR LABS

The DOE weapons labs and NIST currently support several programs that address the needs

[4]U.S. Department of Commerce, National Bureau of Standards, National Engineering Laboratory, ' 'Benefits and Costs of Improved Measurements: The Case of Integrated-Circuit Photomask Linewidths, " NBSIR 82-2458, March 1982; U.S. Department of Commerce, National Bureau of Standards, Planning Office, "Productivity Impacts of NBS R&D: A Case Study of the NBS Semiconductor Technology Program, " June 1981; Judson C. French, National Bureau of Standards, Electron Devices Section, ''Improvement in the Precision of Measurement of Electrical Resistivity of Single Crystal Silicon: A Benefit-Cost Analysis, " report no. 807, Sept. 20, 1967,

Table 2-1—NISTsS Core Competencies

Measurement services	**Physics**
Calibrations	Atomic and molecular physics
Reference data and materials	Chemical physics
	Molecular dynamics and theory
Electronics and electrical engineering	Photon, far UV, and electron physics
Electronic instrumentation	Radiation metrology and dosimetry
Superconducting materials	Radiometric physics
Electric power systems	Time and frequency standards
Magnetics	X-ray spectroscopy
Microwave components and systems	
Optical communication	**Computer science**
Semiconductor devices	Computer security
Semiconductor materials	Image recognition
Semiconductor packaging	Networking architecture and protocols
Semiconductor processes	Software standards and validation
Superconducting electronics	Speech recognition
Manufacturing engineering	**Computing and applied mathematics**
Factory automation	Mathematical software
Mechanical sensors	Numerical optimization
Microelectronics dimensions	Statistical engineering
Precision engineering	
Robotics	**Building and fire research**
	Building fire physics
Chemical science and technology	Building systems
Analytical methods	Earthquake engineering
Biotechnology	Fire safety engineering
Chemical kinetics and transport	Fire hazard analysis
Fluid flow	Structural evaluation
Nuclear chemistry	Thermal machinery
Process sensing	
Thermodynamics	

SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993, p. 45.

of the U.S. semiconductor industry.[5] All three DOE labs have strengths in high-performance computing-originally developed to design and predict the effects of nuclear weapons—that can also be applied to device modeling, process chamber modeling, and factory modeling in the semiconductor industry. Lawrence Livermore's work in lasers and x-ray optics can help develop next-generation lithography equipment. Sandia, responsible for technologies such as microelectronics-driven guidance and control systems, operates a state-of-the-art research line that can produce submicron linewidths on 6-inch wafers. These labs can undertake large projects to develop semiconductor technologies and manufacturing equipment, and have expressed a desire to do so.

NIST offers strong capabilities in metrology, including measurements needed to produce more advanced semiconductors. NIST has maintained a program of work in semiconductor manufacturing since the late 1950s. The lab has several efforts underway to support the semiconductor

[5] This section of the report discusses major semiconductor programs at the labs. For a more complete discussion of lab projects applicable to semiconductor technology, see Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993.

industry-for example, new techniques for measuring surface characteristics of silicon wafers and the thickness of thin films deposited on them, and development of standard reference materials for industry to use in calibrating its systems. While NIST has been named as the lead lab in metrology issues applicable to the Semiconductor Industry Association (SIA) technology roadmaps, it does not have—nor is it likely to be appropriated-the resources to address all requirements. NIST will therefore need to coordinate with industry and other government agencies capable of conducting complementary research, as it has recently done with Sandia.

If properly coordinated, research efforts at NIST and the DOE labs could complement both industry and university R&D efforts. In recent years, industry has displayed an increasing reluctance to invest in new enabling technologies because the R&D is too expensive, too risky, has lengthy payback periods, and requires strengths in many separate disciplines. This is the area in which the labs offer the strongest capabilities. These labs may be most effective as part of long-term, industry-led efforts that require large, multidisciplinary resources and facilities.

Sandia National Laboratories

Sandia National Laboratories operates the largest semiconductor program of the three DOE weapons labs. In 1993, Sandia's expenditures for microelectronics-related programs totaled $106 million, much of which supported collaborative work with commercial industry. Sandia's mission has required the lab to design and manufacture microelectronics and photonics components that withstand harsh operating environments, such as high temperatures and high levels of radiation, and to incorporate them into operational systems. Sandia has also conducted extensive test and evaluation exercises to qualify these components for use in nuclear weapons and to ensure their reliability in an adverse environment over the life of the systems.

As a result, Sandia has considerable experience in the fabrication of semiconductors and ICs. Sandia was one of the early leaders in CMOS (complementary metal oxide semiconductor) technology, the current standard for commercial devices, and helped develop the laminar-flow clean room, which is now used in most commercial manufacturing facilities. In the process, Sandia developed partnerships with defense semiconductor manufacturers, who often produced ICs designed by Sandia and returned them to the lab for final testing and acceptance.

Most of Sandia's work, however, has been directed toward the design and manufacture of ICs for defense purposes--ICs not commercially available. Most of Sandia's products are therefore either radiation-hardened circuits, high-temperature circuits, or custom ICs that industry could not efficiently produce in small volumes. These ICs are often about two generations behind commercial chips in critical parameters such as minimum linewidth, level of integration, and maximum operating speed; Sandia's most sophisticated ICs are typically those it takes from industry and radiation hardens. In addition, because it supplies primarily defense needs, Sandia's manufacturing processes have not been required to achieve the high levels of production routine among competitive commercial semiconductor manufacturers.

Nevertheless, Sandia is unique among the DOE weapons labs in that it supports several facilities for R&D and production of semiconductor devices. The largest of these is the Microelectronics Development Laboratory (MDL). The 74,000-square-foot lab includes 37,500 square feet of clean-room space with 12,500 square feet of state-of-the-art, Class 1 clean space in 22 separate clean rooms that can support individual projects. This design provides maximum flexibility for new processing equipment and device technologies. The capabilities of the MDL were expanded in 1993 by a major donation of equipment and technology from IBM. MDL now houses a state-of-the-art submicron silicon R&D line. MDL's complete

Box 2-B--Sandia's Facilities for Microelectronics

In performing its defense mission, Sandia has established several facilities for microelectronics R&D and production that may be of interest to commercial industry. These facilities address a broad spectrum of issues, from near-term to long-term, and provide, at a single facilit y, the capacit y to design, build, and test ICs and other components. This capability is unique within U.S. government facilities. These facilities are described briefly below.

Microelectronics Design Laboratory

To produce custom designs for its customers, Sandia has developed an integrated approach to the design of microelectronic components and systems. As part of these activities, Sandia writes custom support software, which has become the basis for multiple commercial design packages. Sandia's capabilities reside in a network of over 60 design stations and servers that can support either classified or unclassified projects. The software environment supports the complete design cycle, from photomask layout to systems simulation. Sandia's software environment combines circuit-level simulators, logic-level simulations, as well as both analog and digital system-level simulators, with complete verification from chip to multi-chip module to printed circuit board. The software package also combines layout of photomask with schematic vs. layout checking as well as design-rule checking.

Microelectronics Quality and Reliability Center

Sandia has the facilities and equipment to evaluate and verify the electrical and mechanical properties of microelectronic materials. This capability is applied at the parts level through Sandia's Microelectronics Quality and Reliability Center (MQRC). Sandia's reliability physics and engineering efforts draw upon materials science programs that develop a basic understanding of such failure mechanisms as electromigration or stress voiding, defects in insulators and metalizations, and defects in semiconductors.

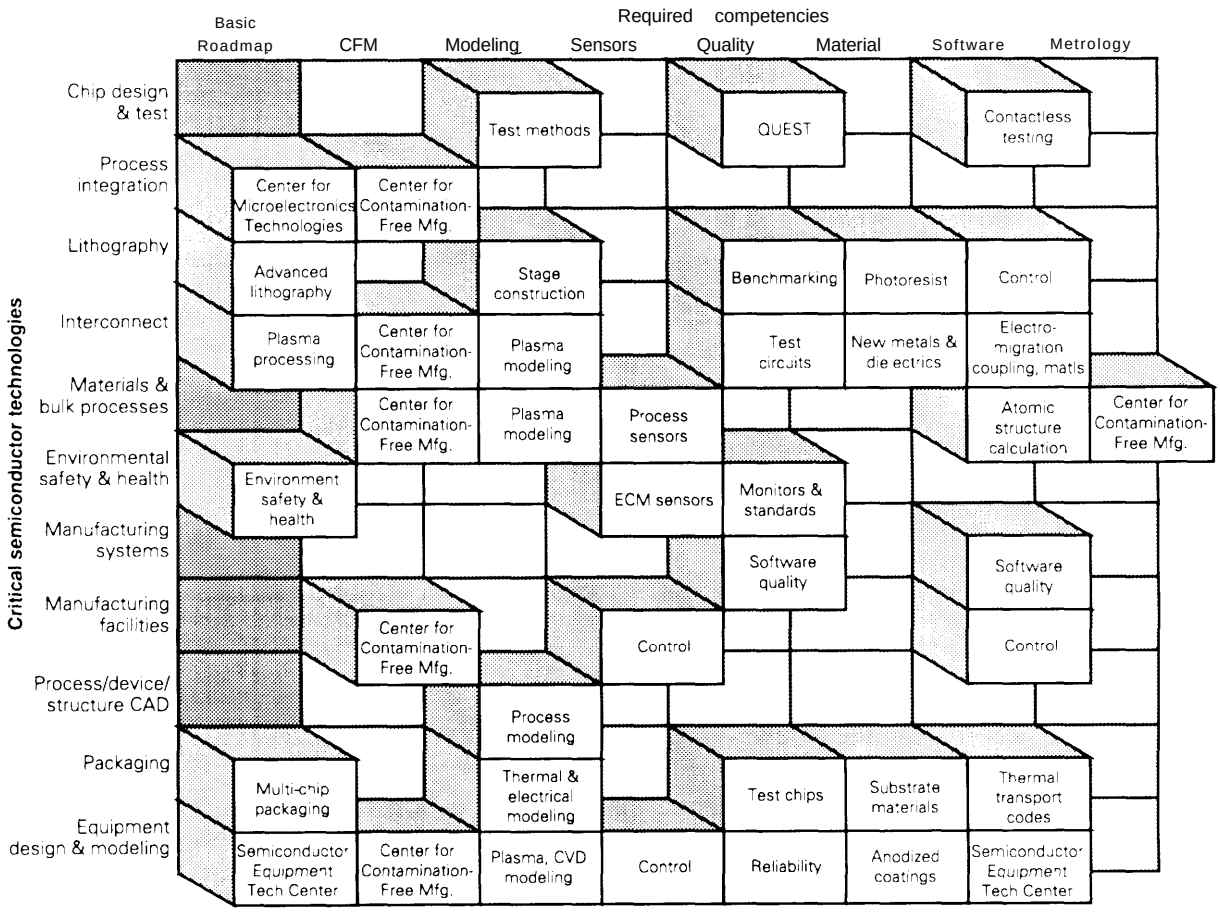
Compound Semiconductor Research Laboratory (CSRL)

The CSRL encompasses the full range of activities--theoretlcal and experimental solid-state physics, materials science, crystal growth, device and circuit design and fabrication-to develop the next generation of compound semiconductor electronic and optoelectronic devices. Facilities include MolecularBeam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) crystal growth capabilities, ion implantation, and electron-beam lithography in a 6,000-square-foot, class-100 clean room with state-of-the-art processing equipment.

Process Design Laboratory (PDL)

This facility for advanced prototype manufacturing is housed in a 100,000-sq.ft. facility and handles hybrid microcircuits, thin film, printed circuits, ceramics, plastics, and rapid prototyping facilities. The PDL coordinates its activities with an integrated manufacturing technology laboratory at Sandia's Livermore, California facility. The charter of the manufacturing center is to examine reliability and quality of manufacturing processes. Particular emphasis is given to automation and robotic hardware. This facility also acts as a proving ground and design center for custom sensors. Additional emphasis is placed on novel approaches to joining and sealing dissimilar materials that have particular relevance to advanced packaging. Collaborations with the Iaccoca Institute at Lehigh University on American competitiveness allow the PDL to support empirical investigations of manufacturing issues such as control and optimization of material flow and workspace organization.

Figure 2-3—Sandia's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 30.

equipment set supports the total semiconductor development cycle. Other Sandia facilities support work in materials quality and reliability, compound semiconductor materials and devices, and process design (see box 2-B),

Commercial Semiconductor Programs

Many of Sandia's ongoing programs are relevant to the commercial semiconductor industry (figure 2-3). Over the past few years, Sandia has initiated a number of new programs specifically targeted at commercial manufacturing. CRADAs are an important part of this process. As of August 1993, Sandia had signed 19 CRADAs related to semiconductor manufacturing (table 2-2), a figure that represents about one-third of all CRADAs underway at Sandia. DOE's total contribution to these projects over their lifetime is estimated at $220 million; the annual contribution is approximately $63 million.

The largest of Sandia's CRADAs is a five-year agreement with SEMATECH. Sandia has been working with SEMATECH for about four years in equipment design and modeling and in technology development. Initially, Sandia's cooperation with SEMATECH operated under a work-for-others contract in which all the work was conducted by Sandia personnel at the lab and was

Table 2-2—Major Sandia CRADAs in Microelectronics

Project title	DOE funding ($K)
Soft X-ray Lithography Tools	**9,286**
Microelectronics Packaging Benchmark	**250**
Advanced Diffusion Barrier Technology	**1,950**
Reduced Lead Loss in Electronics Manufacturing	**570**
Materials Processing at High Temperature/Voltage	**2,308**
Microelectronics Quality/Reliability	**3,130**
Copper-chemical Vapor Deposition for ICs	**1,110**
Printed Wiring Board Interconnects	**5,230**
Application of IRIS to Semiconductor Plasma Processing	**420**
Synthetic Diamond for Multichip Modules	**1,250**
Fabrication of Microreactors in Silicon	**295**
Gold-sulfite Electroplating	**447**
SEMATECH Program (integrated)	**22,500**
Stable Housing **for X-ray Lithography**	**1,150**
Advanced Materials for High-performance Digital	**5,100**
Advanced Intermetal Dielectric Technology	**2,100**
Ferroelectric Read/Write Optical Disk	**1,600**
High-throughput Rotating Disk Reactors	**1,950**
Advanced Manufacturing Techniques for Monolithic Multichip Modules	**2,300**
Total	**$62,946**

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

paid for by SEMATECH. Sandia then signed a one-year CRADA with SEMATECH, which was followed in mid-1993 by the larger, multi-year CRADA. This five-year, $113-million CRADA contains some 19 individual projects. Sandia's annual contribution to the CRADA will average $22.5 million.

The bulk of Sandia's microelectronics work with industry can be divided into three primary areas: semiconductor equipment design/improvement, contamination-free manufacturing, and pilot line services, most of which are coordinated through the Center for Microelectronics Technology (CMT). Many of these programs are geared toward design and development of semiconductor manufacturing equipment, a task that is suited to the lab's technical workforce, over 60 percent of whom are engineers. Sandia has long had the responsibility for integrating new manufacturing technologies into DOE's weapons production facilities and may be able to apply such skills to commercial manufacturing processes as well.

Pilot Line Services-The focus of Sandia's industry-related work is the CMT, which DOE established to serve as a facility for industry-relevant research and development, including maturation of research concepts into manufacturable technologies. This facility is also designed to develop and test next-generation equipment and associated processes. CMT is supported by a large range of semiconductor and microelectronics capabilities and projects, and is associated with Sandia's MDL. Through CMT, university and industry researchers can gain access to the pilot line housed in MDL. This pilot line duplicates the equipment and processing capabilities found on an actual IC manufacturing line. Engineers can use the line to test and optimize new processes before launching into full-scale production on their own lines

Sandia hopes that the CMT pilot line will reduce the time and money semiconductor manufacturers must invest in R&D for new generations of process technology. These burdens have forced

even large semiconductor manufacturers to form strategic alliances with competitors in order to share R&D costs.[6] The pilot line donated by IBM includes equipment worth over $20 million and an estimated $60 million of process technology. The line offers state-of-the art processing capabilities, such as a GCA I-line stepper capable of 0.35-micron minimum feature sizes. Sandia plans to integrate its electron-beam and soft x-ray lithography modules into the line and upgrade all of the equipment to 8-inch wafers, giving them a research line capable of O. l-micron linewidths on select features. This equipment coupled with Sandia's current 6-inch wafer, 0.5-micron fabrication facility (or fab) will provide a research line service not found anywhere else within the government research community.

Equipment Design and Modeling—in August 1989 Sandia established the Semiconductor Equipment Technology Center (SETEC) to help design and improve semiconductor manufacturing equipment. SEMATECH was originally the sole sponsor of the program, providing $12 million over 30 months for ''direct support to U.S. companies engaged in the design and manufacture of IC manufacturing equipment and materials. Since 1991, SEMATECH and DOE have jointly sponsored SETEC through a CRADA, each contributing an average of $6 million per year.

SETEC projects are directed toward development of equipment models to enhance the performance of future-generation equipment, developing design-for-reliability methodologies, and equipment benchmarking. Semiconductor equipment costs are increasing at an extremely fast rate. Today's new semiconductor factory will cost over a billion dollars-three-quarters of which is due to the cost of machinery and equipment.[8] According to current projections, future factories will not yield an adequate financial return unless significant advances are made in equipment reliability and design[9].

One SETEC project, the Reliability Analysis and Modeling Program (RAMP), which is jointly conducted with seven equipment manufacturers, developed software for modeling the reliability of their equipment, including mean time before failure, life cycle cost, and reliability improvement. Such analysis allows manufacturers to redesign equipment so as to improve its performance. Since the project was completed in early 1992, over 150 copies of the RAMP software have been distributed to a wide range of equipment suppliers. Sandia trained 200 people to use the software.

In another SETEC project, Sandia is modeling plasma etch and deposition equipment[10]. Although plasma processing is the method of choice for most etching and deposition steps, the physical characteristics of plasmas are not well known, making them difficult to predict and control. Understanding the mechanism for transferring ions to the silicon wafer requires knowledge of

6 For example, in the last few years, IEM, Toshiba, and Siemens have agreed to jointly develop technologies to produce 256M DRAMs, and Intel has teamed up with Sharp to develop flash memories using 0.6- and 0.4-micron processes.

7 ''Sandia National Laboratories Complete Intitial SETEC Program/Sign New Work Agreement With SEMATECH,'' *SEMATECH Communique,* May/June 1992, p. 6

8 Semiconductor Industry Association *Annual DateBook: Global and US. Semiconductor Competitive Trends, 1978-1991 (San* Jose, CA: Semiconductor Industry Association 1992), p. 38

9 Semiconductor Industry Association, *Semiconductor Technology—Workshop Working Group Reports (San* Jose, CA: Semiconductor Industry Association, 1993), p. 14.

10 A plasma is an ionized gaseous discharge in which there is no resultant charge, the number Of Positive and negative ions being equal. Plasma processing occurs in a reactor, sometimes called a cell, where a high level of control is exerted over the gas temperature and electrical inputs. Plasmas can be used to etch, or remove material from, the patterned surface of a wafer, opening up windows that allow the electrical properties of the silicon in the patterned areas to be changed in subsequent steps. Plasmas can also be used to deposit layers of material on a wafer.

gas chemistry, cell structure and design, and the effects of temperature. Through SETEC, Sandia is attempting to use a supercomputer to develop and verify a basic model of plasma etching, after which it will modify and reduce the code to run on industry-standard mini computers. If successful, the model will reduce from years to months the time it takes equipment makers to bring new designs to market, while improving the uniformity of the etch (or deposition) and machine throughput.

A third SETEC project aims at developing a magnetically levitated stage for a wafer stepper. This technology would allow manufacturers to improve the alignment capability of their lithography equipment. To make complex ICs, patterns must be aligned to within about one-third of the minimum feature size. As linewidths narrow, overlay requirements tighten accordingly. For current ICs with 0.5-micron linewidths, patterns must be aligned to within 150 nanometers (rim); by 2001, the overlay requirement will be 50 to 70 nm.[11] Current technologies may not be able to meet such strict requirements, but proof-of-concept versions of the magnetically levitated stage have demonstrated alignment within 20 nm. Coupled with a new interferometer under development at Sandia, the stage could achieve 0.5-nm stability.

Contamination-Free Manufacturing--Sandia established a Center for Contamination-Free Manufacturing (CFM) through a CRADA with SEMATECH in 1992. The center conducts and coordinates research in cost-effective contamination-free manufacturing technologies involving feature sizes as small as 0.2 microns and removal of defects as small as 0.01 microns (the size of bacteria). The CFM uses Sandia's MDL to conduct experiments that verify advanced semiconductor manufacturing concepts and to develop equipment that reduces the levels of contamination in integrated-circuit manufacturing. Research focuses on the effects of electrostatic fields, chemical particulate, thermal radiation, and electromagnetic radiation (including light) on circuit yield and performance.

Contamination is a primary cause of reduced yields in semiconductor manufacturing. Impurities can arise out of processing chemicals, wafer handling systems, process chambers, and air in the factory. As IC feature sizes become smaller, manufacturers must try to simultaneously reduce the density of defects on a wafer and their size. In 1993, manufacturers could typically tolerate approximately 30 defects on a 6-inch wafer; by 1998, the defect density must be reduced to 20 defects per 8-inch wafer; and by 2004, it must be reduced to Just 5 defects per 16-inch wafer.[12] Whereas in the early 1990s 1-micron contaminants were of little concern, current manufacturing practices cannot tolerate defects larger than 0.1 micron, and defects down to 0.01 micron are quickly becoming a problem. Particles of this size cannot be seen optically and are otherwise difficult to locate on a wafer. New techniques must be invented to detect them.

CMT currently consists of seven projects, which fall into four categories and are included in a 1993 CRADA between Sandia and SEMATECH. In one project, Sandia is developing sensors for detecting contaminants generated during wafer processing. These sensors will enable manufacturers to detect contaminants in real time, allowing for immediate corrective action before fabrication is complete. The sensors will have to be rugged enough to operate in harsh processing environments and be able to monitor gas and chemical purity for unwanted moisture and other particulate at the few parts-per-billion level.

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11 This is roughly the diameter of 150 to 200 atoms. Semiconductor Industry Association, *Semiconductor Technology-Workshop Working Group Reports* (San Jose, CA: Semiconductor Industry Association 1993), p. 37.

12 Semiconductor Industry Association, Semiconductor *Technology—Workshop Working Group Reports*, op. cit., p. 3.

Table 2-3—Los Alamos CRADAs in Microelectronics

Project title	DOE funding ($K)
Supercritical $C0_2$ Cleaning of Particulate	$1,766
Electromagnetic Simulation: High-frequency Computer Circuit Calculations	454
Conductive Oxide Electrodes for Ferroelectric Memory Development	559
Modeling and Simulation of Electronic Devices	2,770
High-temperature Superconductor Devices	3,875
Diamond Technology for Particle and X-ray Detectors	520
Total	$9,944

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

Another type of sensor is being developed for microenvironments. Microenvironment are small plastic containers used to protect and transport wafers between processing steps. Usually the same container is used to transport the same set of 25 wafers from the time they are shipped to the factory until wafer processing is completed. Microenvironment can be a major source of contamination, especially if a film is introduced into the container or if the plastic walls of the container begin to out-gas. The film and/or gas has the potential of ruining all 25 wafers. For wafers containing 100 microprocessors valued at $300 each, the loss of just one container costs $750,000.

Sandia engineers are investigating two ways of monitoring the microenvironment. The first uses the wafers themselves as sensors. Silicon wafers demonstrate a property called total internal reflection. Light directed into a clean crystal will reflect off the inside walls without any loss of intensity. Thus, the microenvironment can be tested by shining light through a window in the wall. The other method of testing the environment uses an electrical vibrating crystal to generate a surface wave across the wafer. Contaminants will retard the wave progress along the wafer.

Other CFM projects include an evaluation of a high-frequency ultrasonic (or megasonic) cleaning mechanism for wafers and several modeling projects that attempt to predict the generation of contaminants during wafer processing and find ways to remove those particles before they reach the wafer.

Los Alamos National Laboratory

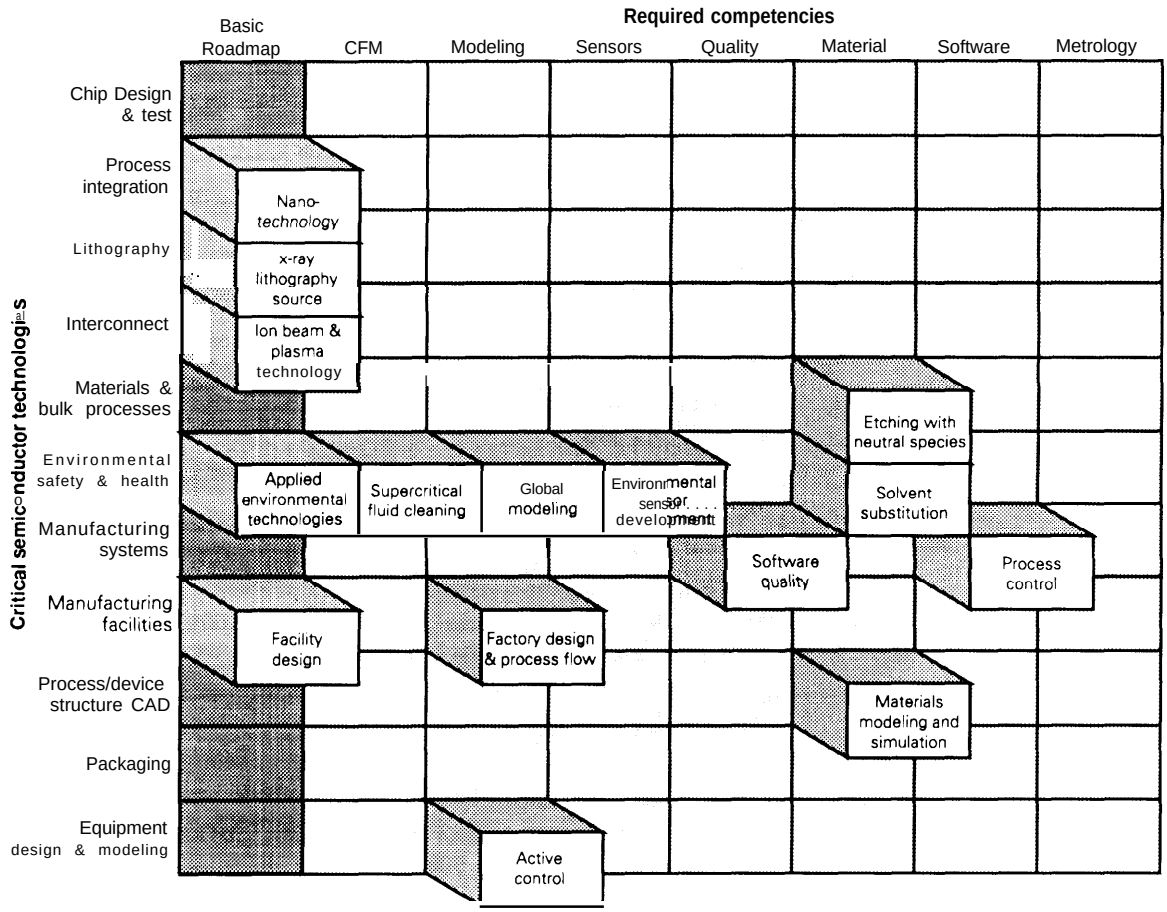
Los Alamos does not have a history of IC fabrication, and its R&D programs in semiconductor technologies are more limited than Sandia's. As a result, Los Alamos has had less interaction with industry in developing semiconductor technologies. In August 1993, Los Alamos had six active CRADAs related to microelectronics, totaling almost $10 million of in-kind laboratory contribution (table 2-3). The number of ongoing programs at Los Alamos that are relevant to the SIA roadmaps is small compared with Sandia (figure 2-4).

Nevertheless, the lab's people and facilities constitute several strong core competencies important to semiconductor manufacturing. Those in which Los Alamos could play a lead role include computer-aided design (CAD) for semiconductor devices and circuits, the materials from which they are made, and the processes used to manufacture them; modeling of semiconductor fabrication facilities; and environmental safety and health (ES&H). Los Alamos' experience with beam technologies could also give it a supporting role in lithography and materials processing.

Modeling and Simulation

Modeling and simulation based on high performance computing is a particular strength of Los Alamos, The lab may be able to play a lead

Figure 2-4-Los Alamos' Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p.37.

role in the development of tools for modeling IC wafer fabrication processes, an area called Technology CAD, or TCAD. Los Alamos is already working with the Semiconductor Research Corporation (SRC) **to** define its role in the development of TCAD technologies.

Los Alamos performs extensive modeling of materials to atomic detail. This work can contribute to both the device and process modeling needs of the semiconductor industry. The lab is developing detailed three-dimensional simulations for devices and circuits to account for the interaction of materials, geometry, and packaging. These computer codes are designed to predict the performance of advanced devices for which conventional simulations are inadequate. The goal of this work is to provide validated design tools for future generations of devices and circuits.

Los Alamos has specialized modeling and simulation capabilities that, when used in conjunction with the capabilities of the other laboratories, can address the needs for process modeling and can contribute to the design of improved process chambers. For example, chemical vapor deposition (CVD) technology is used widely **to** deposit materials such **as** oxides and nitrides of silicon on wafers in the production of ICs. The

design of CVD chambers can be improved substantially by modeling and simulation, thereby improving chip yield and cost.

Los Alamos's modeling capabilities can also be applied to the analysis of complete factories. Such models would allow a full semiconductor manufacturing process to be simulated, including product flows, waste generation, and cost. Such codes may be important in analyzing the cost of future semiconductor fabrication facilities. The cost of building and equipping a new integrated circuit factory today is projected to be over a billion dollars. Even after production starts, it usually takes six months before yields are high enough to make a profit. In order to gain and maintain leadership in semiconductor sales, the industry is striving to offset these costs by improving productivity, increasing quality, and reducing cycle times[13].

Factory modeling has only recently been applied to semiconductor facilities [14]. One reason for this delay is the sheer complexity of the manufacturing process. Random yields, diverse equipment characteristics, unpredictable equipment downtime, material flows, and the problems inherent in using a single facility for both production and research have made modeling difficult. Moreover, most of the more than 300 steps required to produce a single IC require high levels of precision and process control. Between 80 and 100 different machines may be used on a typical production line. Collecting process data at each of these stations requires large computing resources: approximately 240,000 transactions occur each day in a wafer fab.

In support of DOE's efforts to consolidate weapons production facilities, Los Alamos created custom simulations for each DOE manufacturing plant. In addition to performance parameters such as throughput and cycle time, the simulation tracked all material flows, waste streams, and worker exposures. Though not yet tested in the semiconductor industry, these capabilities could help semiconductor manufacturers better plan their production facilities (box 2-C).

Los Alamos' modeling capabilities are made possible by extensive computing facilities. In December 1991, DOE named Los Alamos one of two national High-Performance Computing Research Centers (HPCRC). The HPCRC will attempt to promote technology transfer in advanced computing to industry, academia, and other laboratories through the operation of a computational laboratory, the Advanced Computing Laboratory (ACL). These facilities can make important contributions to the semiconductor industry in TCAD.

Environmental Safety & Health

Los Alamos currently plays a lead role in DOE's program of environmental remediation. In 1993, the lab budgeted almost $200 million for environmental cleanup. While much of this program is tailored to clean-up of nuclear wastes, a number of projects address issues of interest to the semiconductor industry. For example, Los Alamos is working with the Joint Association for the Advancement of Supercritical Fluids to find alternatives to solvents used for precision cleaning in the electronics industry. Through the DOE Industrial Waste Reduction program, Los Alamos is researching ways to recycle metals from waste streams. Los Alamos' Life Cycle Activities project supports work with the Microelectronics and Computer Technology Corporation (MCC) on recyclable workstations and with Motorola on materials return and reuse. The lab is also working with the EPA, the American Electronics Association, and other DOE labs to develop an information retrieval system to access environmental information of relevance to industry. Finally, the lab is working with the American Electronics

13 R. Uzsoy, C. Lee, L. Martin-Vega, "A Review of Production Planning and Scheduling Models in the Semiconductor Industry, Part I: System Characteristics, Performance Evaluation and Production Planning," *IIE Transactions*, vol. 24, no. 4, Sept. 1992, p. 47.

14 Ibid.

Box 2-C-Commercial Application of Los Alamos' Process Modeling Capabilities

Though Los Alamos has not yet applied its factory modeling capabilities to a semiconductor plant, its experience in other portions of the electronics industry demonstrates the efficacy with which codes developed for defense applications can be used to solve commercial problems. One example is Los Alamos's work with Quatro, a small New Mexico business that manufactures printed wiring boards. In the United States alone, the market for printed wiring boards was estimated at $5.5 billion in 1993. Sales by U.S. companies were estimated at $2 billion.

Quatro wanted to build a printed wiring plant that was economically competitive internationality and environmentally benign. The company approached both Sandia and Los Alamos in early 1992 to request help finding a commercially available software package for the factory design. Upon further investigation it was found that any commercially available package would require an extensive effort to modify to include environmental considerations and worker exposure. Thus the company turned to Los Alamos for the simulation.

Applying previously developed code, two engineers--one from Los Alamos and one from Quatro--worked only eight hours to develop a baseline system that accurately portrayed Quatro's existing production facility. With the baseline completed, the engineers used the simulation to optim ize the factory's 120 machine processes. Because of federal and state environmental regulations, pollution prevention was a primary concern. Employing the tool, the engineers were able to completely eliminate many hazardous materials from Quatro's waste stream, including 1,560 pounds of chelated copper, 312 pounds of formaldehyde, and 1,200 pounds of tin and lead per year. Through recycling, the new factory will save on the transportation costs of 63,600 gallons per year of spent etchant, and water use will be reduced to one-third its original level.

The project was completed only 18 months after Quatro decided to undertake the plant study. Without Los Alamos' assistance and code, the baseline system itself could have taken a full man-year of effort to design. As it is, the plant simulation, plant design, detailed costing, and blueprints are finished. The company is currently seeking a combination of private and public funding (about $5 million) to build and initiate operations. Quatro estimates its plant modernization program will substantially increase the number of jobs in the company.

Association to develop alternative manufacturing technologies for manufacturing printed wiring boards.

Applications of Beam Technologies

Another area in which Los Alamos can make a special contribution is in the application of beam technologies (laser beams, electron beams, and ion beams) to semiconductor manufacturing. For example, Los Alamos is developing intense soft x-ray sources based on linear accelerators. These sources can generate light with a wavelength of 13 nm for use in projection lithography systems capable of drawing O. l-micron linewidths. Los Alamos is also working on large-scale ion-beam etching systems that may be of value in the low-cost manufacture of high-density microelectronics packaging (such as multichip modules). These systems potentially offer high levels of throughput at low cost.

Other applications of ion beam technology could allow thin films to be deposited onto silicon or gallium arsenide wafers with greater efficiency than is possible using commercial laser technology. Still other work is pursuing an ion implantation technique based on plasma immersion processes that allows shallow doping of large areas of silicon. Such processes may become important in the development of multiple-layer ICs. Though still in the laboratory stage, Los Alamos hopes to

form an industry partnership to build a prototype system.

Los Alamos has been working with energetic beams of neutral (uncharged) particles for etching and thermal processing. Neutral beams are superior to ion beams for etching feature sizes less than 0.5 micron because they cause less structural damage to the substrate material.[15] Neutral beams can also grow insulating layers while avoiding many of the problems associated with thermal etching processes.[16] Los Alamos would like to team with an industrial partner active in chip processing to create prototype production equipment using hot neutral sources.

Lawrence Livermore National Laboratory (LLNL)

Like Los Alamos, Lawrence Livermore has not manufactured ICs as part of its mission. The lab does, however, run several R&D programs in semiconductor technology that contribute to portions of the SIA roadmap (figure 2-5), Of LLNL's $1 billion operating budget in 1993, approximately $80 million supported R&D in areas related to semiconductor technology. In addition, LLNL, like the other DOE laboratories, has expanded the scope of its cooperative R&D with industry, By the end of 1992, LLNL was contributing $72 million to 84 cooperative agreements with industry; over $30 million was for CRADAs in microelectronics (table 2-4)

The areas in which LLNL is most capable of contributing to the SIA roadmaps are in x-ray lithography, IC packaging, and other applications of laser technology. Lawrence Livermore has developed world-class scientific and technical expertise in high-power lasers and electro-optics. The lab has extensive experience in the technology of laser-generated soft x-rays, soft x-ray optics and diagnostics, and precision metrology. LLNL has also worked on applications of laser technology to doping semiconductors. Most of this work is conducted at the Center for Applications of Laser and Electro-Optic Technologies (CALEOT), which maintains 20,000 square feet of laboratory space for R&D on advanced lithography and on laser material processing

Soft X-ray Projection Lithography

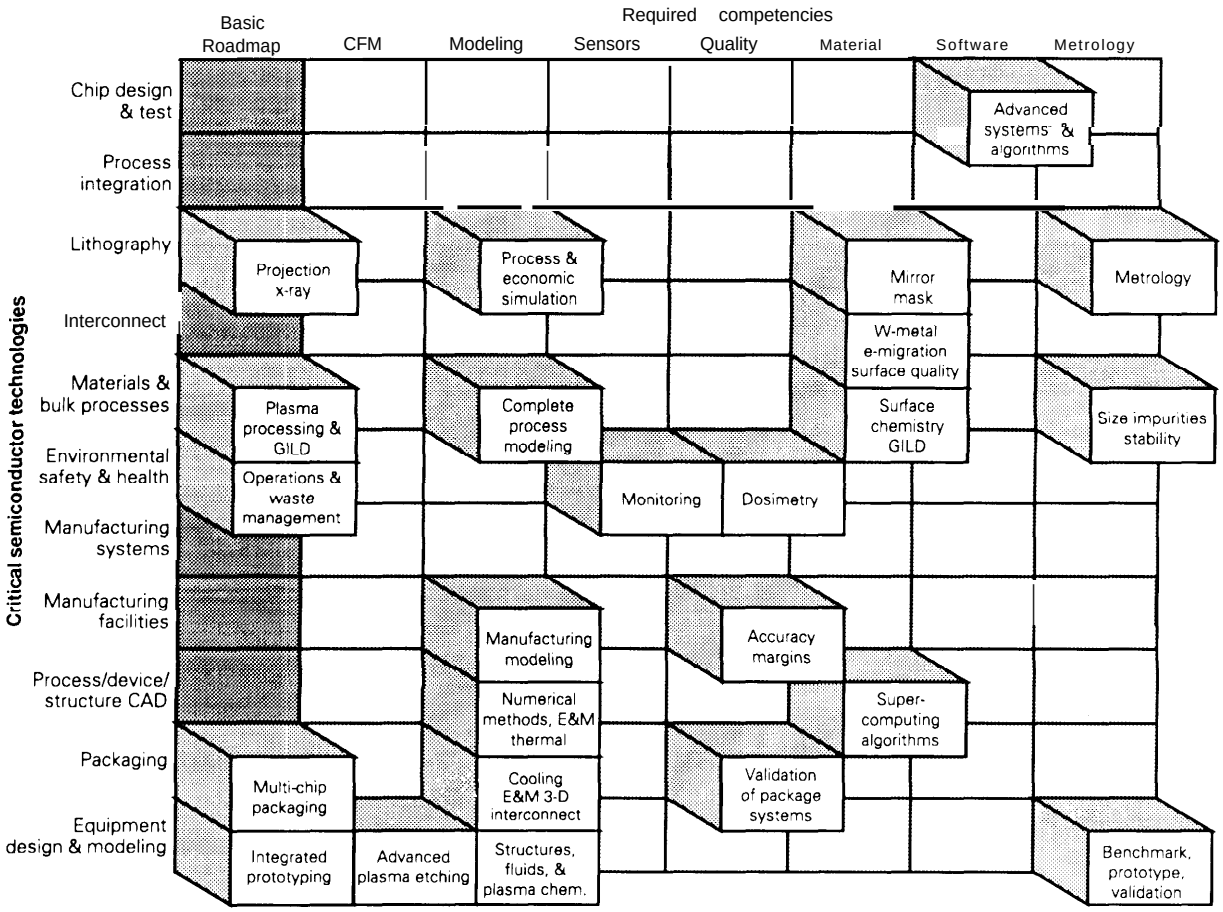
LLNL has a number of programs in soft x-ray projection lithography that could enable it to take a lead role in a larger, national x-ray lithography program, The appeal of soft x-ray projection lithography as a lithographic strategy for U.S. industry derives largely from its potential to project features of 0.1 micron or smaller. This reduction in size could provide a 25-fold improvement in integrated circuit density by the end of this decade.

LLNL, Sandia, Lawrence-Berkeley Lab (LBL, another of DOEs multi-program labs), and industrial organizations are building the prototype systems. AT&T and LLNL devoted about $8 million between 1989 and 1992 to develop and characterize high-performance coatings for the multilayer mirrors that direct the x-rays from their source to the mask. LBL and LLNL have spent $4 million on x-ray interferometry systems to measure the characteristics of x-ray optics. GCA-Tropel has submitted a CRADA proposal to the labs to further pursue this work. LLNL and Micrion Inc. have devoted about $2 million to mask patterning, damage, and repair studies. AMD, DuPont, KLA, and Micrion have submitted a CRADA proposal to LLNL to develop defect-free coating technology and inspection and repair capabilities. Ultratech Stepper and Jamar also have CRADAs with LLNL in soft x-ray projection lithography.

15 Ion beams can break down thin insulating layers of material and build up charge in localized areas, causing deformation of the side walls etched into the substrate,

16 In gallium arsenide devices, for example, thermal processes used to grow a layer of oxide can result in the formation of metallic arsenic and can induce disorder in the lattice structure of the substrate.

Figure 2-5—Lawrence Livermore's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 44.

Additional lithography research is being conducted by LLNL's Center for Applications of Laser and Electro-Optic Technologies (CALEOT). Lasers developed by the lab were to be used by Hampshire Instruments to support work in proximity x-ray lithography and could supplant excimer lasers used for UV lithography systems. The company folded before the project could be completed. The solid state glass laser developed by CALEOT is being inserted into a state-of-the-art commercial lithography system.

Laser Applications: Gas Immersion Laser Doping (GILD)

Lawrence Livermore National Laboratory and Stanford University are working together on an innovative doping process which significantly reduces the number of steps required to make integrated circuits. The process, called Gas Immersion Laser Doping (GILD), replaces currently ion implantation processes and, in practice, can reduce lithographic processing steps (among the most expensive in a fabrication facility) by 46

Table 2-4—Lawrence Livermore CRADAs in Microelectronics

Project title	DOE funding ($K)
Cost-Effective Machining of Ceramics	1,646
Interconnects for Multichip Modules	2,817
Computer-Aided Design of Plasma Etch Reactors	4,800
Compact Soft X-ray Exposure System	10,458
Fabrication of Non-Planar Devices	1,065
Soft X-ray Projection Lithography	9,800
Total	$30,586

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

percent--cutting costs while improving yield and device performance.

GILD uses a relatively simple process to diffuse dopant atoms into a silicon wafer. A silicon wafer is immersed in an atmosphere of dopant gas. An excimer laser beam is then directed through a patterned mask, melting the wafer surface at specific locations and causing the dopant molecules to diffuse into the silicon. The ion implant (conventional) technique directs a high-energy stream of dopant ions into the silicon wafer. But before the ion implantation can be done, the wafer surface must be prepared by applying a special coating, called a resist, to areas that must be shielded from the ion stream. The resist preparation includes a lithographic exposure, etching, and a cleaning operation. After the ion implantation, the resist must be stripped off, requiring plasma processing and several cleaning operations. All told, ion implantation takes 13 steps compared with GILD's one (figure 2-6).

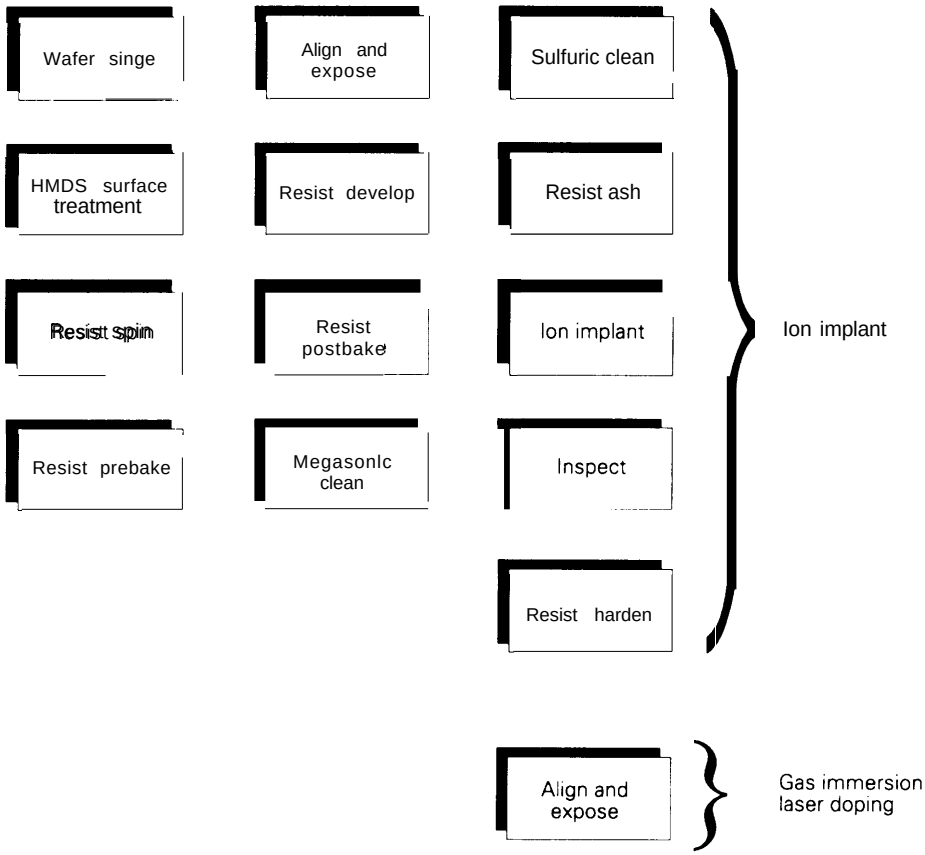
GILD not only reduces the number of steps for doping, it also provides better control over the process. Two critical processing factors for any doping technique are the dopant density at the junction and the junction depth. GILD controls the amount of dopant absorbed by the number of laser pulses at the junction while the junction depth is controlled by adjusting the laser intensity. At this time GILD is the only demonstrated technology that can produce junction depths shallow enough to meet the SIA roadmap junction depth requirements for the year 2001 and beyond. SIA specifies a maximum junction depth of 25 nm for the year 2001. GILD currently produces junction depths as shallow as 10 nm whereas ion implantation is at 40 nm. Other benefits over conventional processing include more uniform dopant distribution, the ability to fabricate narrower base regions, and the elimination of high-temperature anneals (which complicate multilayer processing by allowing dopants to migrate into adjacent layers), and compatibility with 0.2 micron and smaller feature sizes,

LLNL is already one year into a three-year project that is focused on process development and advanced equipment design to demonstrate suitability for manufacturing applications. The projection version of the GILD tool is compatible with the flexible fab or cluster tool concept being pursued by DoD's Advanced Research Projects Agency (ARPA) to help reduce the economies of scale inherent in semiconductor manufacturing. ARPA had provided some early funding to GILD to supplement laboratory funding, but future support is uncertain.

National Institute of Standards and Technology (NIST)

NIST supports semiconductor research through both its intramural and extramural programs. Intramural programs make use of NIST's own staff and facilities and are oriented almost exclusively toward metrology. Extramural programs are conducted by industry partners and can therefore explore technical problems outside

Figure 2-6--Processing Steps Required for GILD Versus Traditional Ion Implantation Techniques



SOURCE: Kurt Weiner, Lawrence Livermore National Laboratory, personal communication, Aug. 27, 1993.

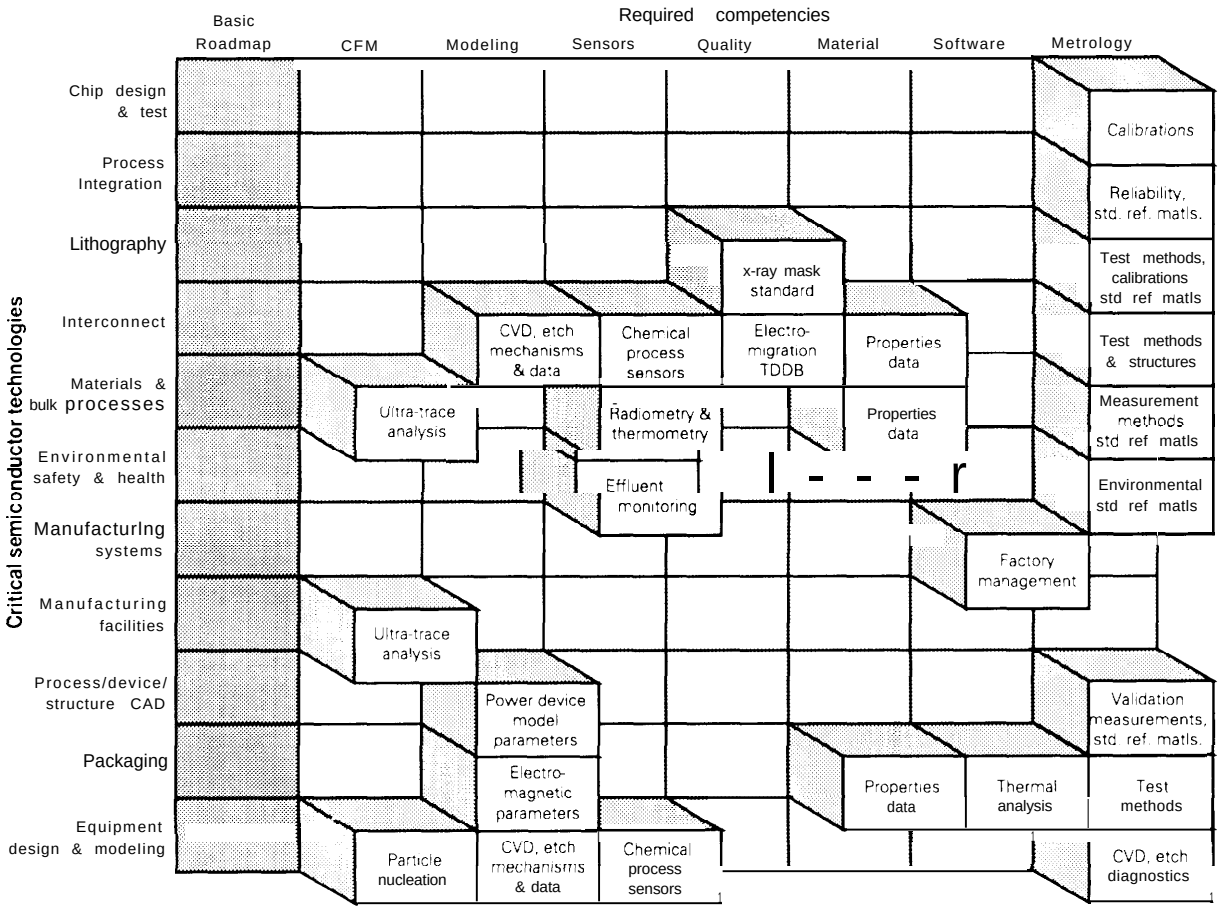
NIST's specific areas of expertise. Together, these programs give NIST the capability to contribute to many areas of semiconductor technology.

Intramural Programs

NIST's intramural programs in semiconductor technology are conducted largely by its Semiconductor Electronics Division, which has an operating budget of about $7 million and a staff of 43, about 35 of whom are full-time researchers. An additional $2.5 million of work is performed by other NIST divisions responsible for chemistry, physics, computer science, and materials science. The programs conducted by these divisions match many of the requirements of the SIA roadmap (figure 2-7). Primary thrusts of the current research program are on semiconductor materials measurements; selected device properties, theory, and models; process control measurements based on test structures and supported by machine learning analytical techniques; and optical and non-optical critical dimension metrology (see box 2-D).

One example of NIST's work is the ellipsometer developed by the Materials Technology group. This device uses polarized light reflected obliquely off a silicon wafer to measure the thickness of deposited films. NIST used this ellipsometer to develop standard reference materials, available in

Figure 2-7—NIST's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, 'The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p.46.

50-, 100-, and 200-nm thicknesses and certified to an accuracy of half a nanometer, so that industry can verify its own measurement systems. NIST's initial offering of sets of the standard reference materials sold out quickly at $1,300 apiece, and the sets are still in demand.

NIST's semiconductor technology program is being expanded by the Office of Microelectronics Programs as new funding can be obtained to draw on the many other technical resources present at NIST. New work has begun on plasma etching processes to develop the data necessary for the creation of physically based process models. Additional research is underway to measure the properties of materials used in semiconductor device packaging, and on extensions to the existing work described above. Both the structure of existing work and plans for new work are being adjusted to address the measurement needs of the national semiconductor roadmap, which specifically identifies NIST roles in the area of metrology and reference data.

NIST has also participated in projects sponsored by SEMATECH. NIST found and corrected a number of sources of errors in the light-intensity measurements in a developmental lithography system. It had appeared that the lithography system was not meeting its light output specifica-

Box 2-D—NISI% Role in Resistivity Measurement

NIST has a long history of helping semiconductor manufacturers and their suppliers measure the resistivity[1] of silicon wafers used to manufacture ICs. Before NIST initiated its program in resistivity measurement in the early 1970s, difficulties in correlating measurements of resistivity between silicon suppliers and IC manufacturers resulted in some 7 percent[2] of all silicon shipments being rejected by manufacturers. Comparable losses in terms of today's silicon market would cost the U.S. semiconductor industry well over $1803 million a year.

Suppliers custom-make silicon to the buyer's specifications, the most important of which is the acceptable resistivity range. Resistivity indicates the silicon's purity, uniformity, and suitability for device purposes. Often, inaccurate measurements either caused buyers to accept orders that were out-of-specification, resulting in low production yields, or caused them to reject orders that could have been acceptable. The lack of measurement agreement was so commonplace that silicon vendors began to keep a log of adjustment factors that helped to compensate for the difference between their measurements and the measurements of their customers.

in 1960, the American Society for Testing and Materials (ASTM) asked NIST (then the National Bureau of Standards) to take the lead in improving measurement techniques of the resistivity of silicon. Most companies, at the time, used the four-probe method for measuring resistivity. The process used one pair of probes to send a known amount of current through the wafer; another pair of probes measured the voltage drop across a section of the wafer. Resistivity was calculated using a simple formula relating the current, the voltage, and the spacing of the probes. The process gained much popularity because it was non-destructive and efficient. NISTspent several years studying the problem with the help of over 22 companies. The effort resulted in the development of correction factors and a standardized procedure for making the measurement. The overall accuracy was improved by an order of magnitude.

The most obvious savings realized from the improvement was a reduction in material rejection or waste caused by a lack of measurement agreement between the buyer and the seller. In addition, buyers were able to reduce the previous levels of testing necessary to achieve measurement agreement with the seller. The most significant benefit, but hardest to quantify, is the gain in manufacturing yields resulting from improved production control.

Upon release in 1967, the NIST correction factors and measurement procedure became a world standard. Shortly thereafter, NIST began selling a silicon wafer standard reference material (SRM) so that suppliers and buyers can check and calibrate their measurement instruments. The SRM, too, has become a de facto standard, used throughout the world.

Today NIST is working on improving the resistivity measurement required to take the industry to 0.2-micron linewidths. Two atomistic methods are being developed. One essentially sandblasts a hole into the material using argon ions,The ratio of silicon atoms to dopant atoms coming out of the hole is subsequently measured, Resistivity is based on the ratio. The other method measures resistivity by mapping atoms on an atomic scale. The goal is to reduce t he measurement uncertain y from the current 1.6 percent to 0.8 percent.[4] The procedures for the new method will be released by 1995.

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1 Resistivity is the resistance that a centimeter cube of a material Offers to the passage of electricity.

2 improvement *in the Precision of Measurement of Electrical Resistivity of Single Crystal Silicon: A Benefit-Cost Analysis,* J. French, National Bureau of Standards, Report Number S07, Sept. 1967.

3 Seven percent of the $s.4 billion market for semiconductor grade silicon in 1993.

4 Personal communication, R. Scace, NIST, April 1993.

tions, but the problem was entirely a matter of measurement error. In another project, NIST is conducting a round-robin calibration experiment on mass flow controllers, used universally for controlling gas flows in semiconductor manufacturing equipment, but often found to be inaccurate. Errors in these controllers arise from calibration uncertainties, incorrect installation practices, and variations in the composition of gas mixtures. The experiment is aimed at the frost of these effects; subsequent work will address the other issues. These projects have resulted in the establishment of new calibration services at NIST for ultraviolet light meters and for mass flow controllers.

NIST supports a wide range of working relationships, from a single phone call or visit to extended residence of industrial, academic, and government researchers at NIST under several forms of agreements that include CRADAs. As of spring 1993, the Semiconductor Electronics Division had signed about 10 CRADAs with industry, each averaging $200,000 of NIST contribution. These figures correlate to one CRADA active or pending for every four full-time technical employees. In addition, the Semiconductor Electronics Division had many guest researchers working in its facilities.

NIST's CRADAs tend to be smaller than those of the DOE labs, reflecting the smaller scale of many metrology projects and the agencys smaller budget. The DOE labs' larger budgets enable them to mobilize many researchers to attack large problems requiring extensive facilities; a typical NIST project may involve only two to three full-time research personnel.

Extramural Programs

In addition to its intramural research program, NIST also manages extramural semiconductor research conducted under the Advanced Technology Program. Through ATP, NIST provides funding to individual companies and consortia to develop precompetitive, generic technologies. ATP is a cost-shared program in which industry typically provides more than half the total project funding and sets research goals and objectives. All projects must pass a technical evaluation and a business plan evaluation to help ensure that the programs are technically feasible and that the participating companies have a viable plan for commercializing the resulting technology. The goal of the program is to help companies apply research results to the rapid commercialization of new scientific discoveries and to the refinement of manufacturing technologies. The program can assist joint R&D ventures with technical advice or it can provide start-up funding or a minority share of the cost, or lend equipment, facilities, and people to the venture.

ATP has supported a number of semiconductor projects. Out of the 60 grants awarded during ATP's first three competitions, 18 are related to semiconductor technology. Participating companies plan to contribute $45 million to these 18 projects and requested just under $50 million in funding from ATP, to be spread out over periods of one to five years. In 1993, ATP provided $7.8 million in matching funds for microelectronics technology projects. These projects span a broad spectrum from manufacturing equipment to semiconductor devices to systems. Under one program, Spire Corp. will develop advanced sensors for a metal-organic chemical vapor deposition chamber used to produce diode (semiconductor) lasers. In another program, Nonvolatile Electronics, Inc. will develop anew type of random access memory (RAM) device that will not lose data when turned off.

COORDINATION OF LAB ACTIVITIES

Together, the semiconductor programs run by the DOE and NIST labs address many of the issues associated with the SIA roadmap, OTA's industry panel, after reviewing the labs' capabilities, identified several areas in which these labs could work effectively (table 2-5). However, each individual cell on the SIA roadmap will require many complementary projects to address near-,

Table 2-5—Possible Semiconductor Focus Areas for Federal Labs

- **Perfect process chambers**
  - Modeling/verification
  - Science knowledge base
  - Environmental safety and health (sensors)
  - Environmentally conscious manufacturing
- **Metrology**
  - Calibration services
  - Standards/reference materials
  - Reference data
  - Measurement methods
  - Diagnostic techniques
- **Wafer handling**
  - Contamination
  - Mechanism design for high reliability
  - Algorithms
  - Software assurance
- **Material systems**
  - Chemistries
  - Contamination-free manufacturing
  - Point-of-use generation/disposal
- **Lithography**
  - invention/commercialization gap
  - Soft x-ray
  - Sources/stages/alignment
  - Electron beam/ion beam technology and prototypes
  - Metrology for mask and water analysis
- **Technology computer aided design (TCAD)**
  - Algorithms for design simulation
  - Algorithms for process synthesis
  - New computing tools
  - TCAD framework
- **Manufacturing systems**
  - Factory design and modeling
  - Flexible scalable factories
  - Sensors
  - Large wafer equipment design/technology
- **Packaging**
  - Cooling
  - Thermal analysis budgets
  - Energy efficiency
  - Array bonding
  - Stress/thermal/electro-magnetic modeling
  - Low stress, encapsulants
  - Multichip packaging technology
- **New materials**
  - Advanced metallization (i.e., copper) dielectric/package materials
  - Thin dielectrics
  - Characterization of materials
- **Device physics**
  - Use of advanced computing techniques from process and device to system analysis and synthesis
  - Nanotechnology
- **Contamlnatlon-free manufacturlng research**
  - Defect and contamination modeling
  - Detection, measurement, and analysis
  - Wafer cleaning and transport
  - Clean gases, liquids, equipment, and processes
- **New chemistries**
  - Neutron beam for low-damage, high-throughput etching and deposition
  - Environmentally sensitive materials
  - Chemical recycling/re-use

SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993, pp. 51-52.

mid-, and long-term issues. Industry, universities, and the labs will each have roles in any program to address these needs. Proper coordination of these organizations will be required to ensure effective use of the labs' capabilities.

Coordination with industry will be required to make sure that laboratory programs meet commercial requirements. To date, the DOE weapons labs have concentrated their technology development programs on issues of importance to the defense community; these labs have only limited experience working on commercial technologies or in a commercial environment in which cost is a primary concern and product generations change rapidly. Making the transition will require time and considerable industry guidance. The SIA roadmaps represent a first step in this direction, in that they express, in a form that is easy to communicate, industry's consensus on its technology needs for the next fifteen years. Continued industry participation will be needed, however, to ensure that laboratory programs to meet these needs are properly implemented and

properly coordinated with industry and university R&D efforts.

Additional coordination will be needed to eliminate or prevent unnecessary redundancy between laboratory programs. At this point, however, the potential for such overlap appears limited. One reason is that the capabilities of the DOE weapons labs and NIST are, in many ways, complementary. DOE labs have the skill set, expertise, and funding to work on large-scale R&D programs, especially those that require multi-disciplinary teams and large, expensive facilities. The DOE labs are set up to work on the higher-risk, longer-duration projects and to deliver operating prototypes, as well as an underlying precommercial knowledge base. NIST is best suited to solving measurement problems and delivering results in a form suitable for use by the industry. Measurement may be a demanding problem requiring significant fundamental research prior to developing a technique suited for practical use, or it may require off-the-shelf NIST technology.

Furthermore, while several labs may claim a competency in a particular technology area, these areas are so broad that planned programs are unlikely to overlap. For example, all three DOE laboratories are strong in numeric simulation and modeling; however, they use this competency to accomplish separate mission responsibilities. Sandia's modeling capabilities are targeted toward plasma modeling and chemical vapor deposition chambers; Los Alamos uses its modeling capabilities to simulate factories and develop active control systems for use with real-time sensors; Lawrence Livermore's modeling capabilities support work in areas such as packaging, structures, and lithography. In addition, both LLNL and NIST have ongoing programs in metrology to support x-ray lithography, but LLNL's capabilities in forming aspheric mirrors are complemented and supported by NIST's capabilities in measuring the precise curvature of the mirror's surface. Similarly, all three DOE laboratories have established major efforts in environmental safety and health for weapons work that may be relevant to semiconductor processing and environmentally conscious manufacturing. Sandia has capabilities in sensors and monitoring for quality; Los Alamos supports work in solvent substitution and clean manufacturing technologies; Lawrence Livermore has research programs in dosimetry and waste management.

In addition, the labs have expressed a commitment to achieve the required coordination and have made several attempts to coordinate their research efforts. Sandia recently signed a Memorandum of Agreement (MOA) with NIST on their activities in metrology. The first industry to be addressed under the Sandia/NIST MOA is the U.S. semiconductor industry. The intent of this program is to maximize cooperation and minimize duplication so that the resources of the two institutions are used most effectively. In addition, the new National Center for Advanced Information Component Manufacturing (NCAICM) established by Congress at Sandia will coordinate research by the three DOE weapons labs and ARPA in the areas of flat panel displays and microelectronics, Projects under this program will be funded through ARPA and performed jointly by industry and the DOE labs. NIST and Sandia have also coordinated their efforts in x-ray lithography through lab visits and transfers of personnel. Such efforts may prove highly effective in enhancing the ability of the laboratories to contribute to commercial semiconductor technology.