

Call for Papers

IEEE Micro Special Issue:

Interconnects for Multicore Chips

September/October 2007

Guest Editors

Partha Kundu, Intel Corporation

Li-Shiuan Peh, Princeton University

Overview

Transistor budgets are making massively parallel processors on a single chip a reality. Such multicore chips have taken many forms, from conventional, coarse-grained symmetric multiprocessing on a single chip to arrays of processing elements connected together to realize program-defined functions. The domains targeted, in addition to general-purpose computing, have also been diverse; multicore chips have been purpose-built to serve specific functions ranging from network processing to security acceleration and multimedia and graphics processing. In all such architectures, the on-chip interconnect has played a significant role—not just in providing a low-power, high-bandwidth, fast communication substrate that enables scaling to large numbers of cores, but also in allowing a rich set of communication modes that offer guarantees of service, reconfigurability, and programmability.

The purpose of this special issue of *IEEE Micro* is to bring readers the latest advances in the field of on-chip interconnects for multicore chips. We seek original papers with a strong focus on actual prototypes, discussing experiences and challenges faced in the design of the prototypes, along with performance evaluation of the chips. We are soliciting contributions in areas including but not limited to the following:

- interconnect architectures for general-purpose chip multiprocessors;
- interconnect architectures for specialized multicore chips used in media, gaming, networking, financial and scientific applications, and other arenas;
- novel interconnect architectures for programmable array processors and reconfigurable processors;
- analysis and characterization of on-chip interconnects in leading-edge multicore chips;
- prototypes of novel router microarchitectures used for on-chip interconnects;
- synthesized network-on-chip prototypes for embedded multiprocessor SoCs;
- prototypes of interconnects used for stacked 3D ICs; and
- prototypes of optical-based interconnects for on-chip communication.

Authors will receive five complimentary copies of the special issue. Authors of selected articles will be further encouraged to submit expanded versions of their articles for possible publication as online IEEE ReadyNotes.

Submission Procedure

Log onto IEEE CS Manuscript Central at <http://cs-ieee.manuscriptcentral.com>, and submit your manuscript. For questions, please contact the *IEEE Micro* magazine assistant at micro-ma@computer.org.

For the manuscript submission, acceptable file formats include Microsoft Word and PDF. Manuscripts should not exceed 5,000 words (with each average-size figure counting as 150 words toward this limit), including references.

Please include all figures and tables, as well as a cover page with author contact information (name, postal address, phone, fax, and e-mail address) and a 200-word

abstract. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere, and all manuscripts must be cleared for publication. Accepted articles will be edited for structure, style, clarity, and readability. For more information, please visit the *IEEE Micro* Author Center, online at <http://www.computer.org/portal/site/micro>.

Key Dates

Papers due: 1 June 2007

Notification date: 6 July 2007

Final version due: 23 July 2007

Publication: September/October 2007