

A Happy Family of Processor and Interconnect Architectures

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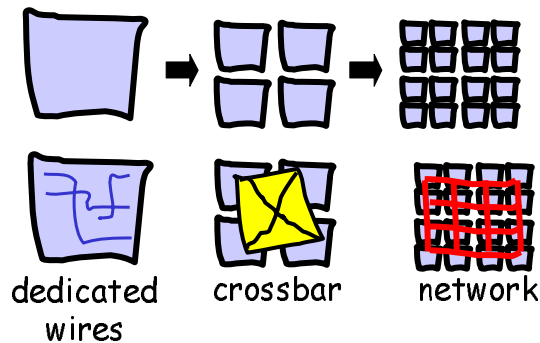
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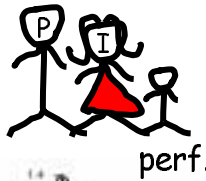
Why proc. and int. need to come together...

- Fine-grain parallelism tightly couples processor and interconnect architectures

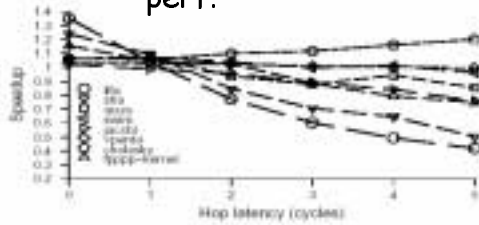


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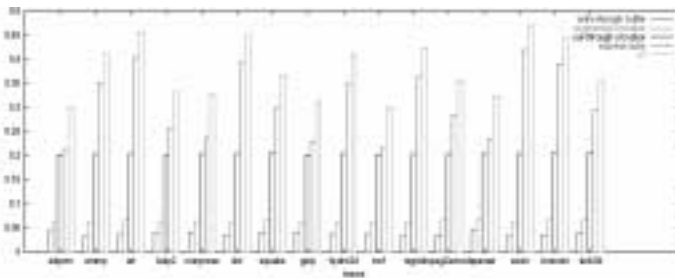


Because processor perf. <-> interconnect perf.



[Raw, HPCA'03]:

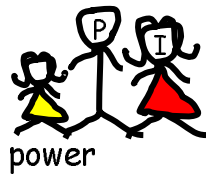
Interconnect delay highly impacts CMP performance



[TRIPS traces on network simulator]:

CMP traces highly impact interconnection network delay

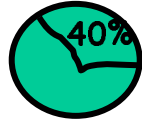
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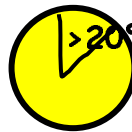
Because processor *power* <-> interconnect *power*

• Can't we ignore interconnect power? No...

MIT Raw CMP



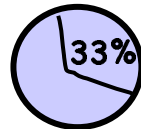
Alpha 21364 Microprocessor



Mellanox server blade

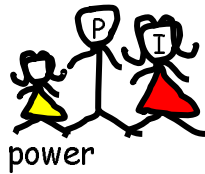


Internet router



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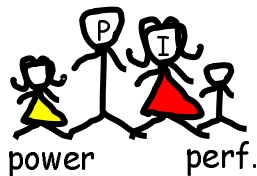


Because processor *power* <-> interconnect *power*

- Processor/interconnect power optimization impacts the other:
 - Impacts other's performance
 - Impacts other's power budget
 - Impacts system temperature

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One big happy family...

- How to realize this in research?
 - *Solo Superman*
 - *Collaboration:*
 - Tools to facilitate marriage
 - Conversations and exchanges between processor and interconnect architects

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What interconnect architects can offer...

- Simulation tools for design space exploration
 - **Orion**: A network power-performance modeling and simulation tool [MICRO'02]
 - Within Liberty Simulation Environment [August] and as a stand-alone C++ network simulator
 - Architectural dynamic and leakage power models for networks
- Consideration of interconnect architectures' impact on processor performance/power

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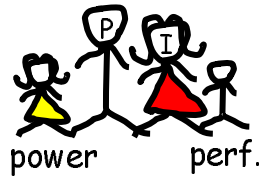


What processor architects can offer...

- Traffic traces
 - Past synthetic network traces unsuitable for power-performance tradeoffs.
 - So far:
 - TRIPs benchmark traces
 - RAW traces soon
- Multiprocessor simulation frameworks
 - So far:
 - Orion -> RSIM

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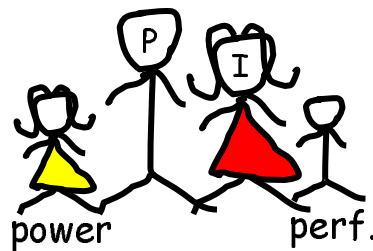


One big happy family...

- How to realize this in education?
 - Don't ignore networks chapter of H&P!
 - Network interface material as a bridge
 - Hope: Students to be as familiar with buses, crossbars, links, and router pipelines as they are currently with caches, registers, adders and processor pipelines.

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Future in computer architecture
-- A happy family of
low-power, high-performance
processors and interconnects.

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