

# Prateek Mishra

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OBJECTIVE	To obtain a job in an area related to my research interests in logic design and associated CAD methodologies	
EDUCATION	<b>Princeton University, USA</b> <ul style="list-style-type: none"><li>• Ph.D., Electrical Engineering, expected Jan 2011</li><li>• M.S., Electrical Engineering, May 2008</li></ul> <b>Indian Institute of Technology (IIT) Kanpur, India</b> <ul style="list-style-type: none"><li>• Bachelor of Technology in Electrical Engineering, May 2006</li></ul>	
RESEARCH INTERESTS	Digital VLSI design and EDA methodologies in the realm of aggressively scaled methodologies	
WORK EXPERIENCE	<b>IBM T. J. Watson Research Center, Yorktown Heights, NY</b> <i>Graduate Research Intern</i> (June - August 2008) <ul style="list-style-type: none"><li>• SRAM design, analysis and layout at the 22nm technology node</li><li>• Evaluated and implemented a 22nm SOI 75Kb SRAM test chip</li><li>• Studied the full macro cross section of the test chip for various performance metrics</li><li>• Analyzed SRAM failure probability</li></ul> <b>Concordia University, Montreal, Canada</b> <i>Undergraduate Technical Intern</i> (May - July 2005) <ul style="list-style-type: none"><li>• Designed a low-power asynchronous wrapper that could communicate between two synchronous systems with independent clocks</li><li>• Results showed better delay, throughput and power characteristics as compared to previous designs in literature</li></ul> <b>IEEE Summer Camp, IIT Kanpur, India</b> <i>Technical Mentor</i> (May - June 2006) <ul style="list-style-type: none"><li>• Timing characterization and power of dual edge-triggered flip-flops</li><li>• Design and layout of a 8b*8b divider</li></ul>	
BOOK	<ul style="list-style-type: none"><li>• <b>P. Mishra</b>, A. Muttreja, and N. K. Jha, "FinFET circuit design," book chapter in <i>Nanoelectronic Circuit Design</i>, Springer 2010</li></ul>	
PUBLICATIONS	A. Muttreja, <b>P. Mishra</b> and N. K. Jha, "Threshold voltage control through multiple supply voltages for power-efficient FinFET interconnects," in <i>Proc. Int. Conf. VLSI Design</i> , pp. 220-227, Jan. 2008 <b>P. Mishra</b> , A. Muttreja and N. K. Jha, "Evaluation of multiple supply and threshold voltages for low-power FinFET circuits," in <i>Proc. IEEE Symp. on Nanoscale Architectures</i> , pp. 77-84, Mar. 2008 <b>P. Mishra</b> and N. K. Jha, "Low-power FinFET circuit synthesis using multiple supply and threshold voltages," <i>ACM J. Emerg. Technol. Comp. Syst.</i> , vol. 5, pp. 1-23, Mar. 2009	

**P. Mishra**, A. Bhoj and N. K. Jha, "Die level leakage power analysis of FinFET circuits considering process variations," in *Proc. Int. Symp. on Quality Electronic Design*, pp. 347-355, Mar. 2010

**P. Mishra** and N. K. Jha, "Low-power FinFET circuit synthesis using surface orientation optimization," in *Proc. Design, Automation and Test in Europe Conference*, pp. 311-314, Mar. 2010

**P. Mishra** and N. K. Jha, "Process variation tolerant design of FinFET standard cells library using response surface methodology under design of experiments," to be submitted in *Proc. IEEE Symp. on Quality Electronic Design*

## PROJECTS

### Graduate Level

#### **Simultaneous driver and wire sizing for performance and power optimization**

- Sized quantized 3T and 4T FinFET buffers for optimized power-performance of global interconnect lines

#### **Evaluation of multiple supply and threshold voltages for low-power FinFET circuits**

- Developed a novel multiple supply voltage scheme to dynamically control the threshold voltage of FinFETs

#### **Improving multiprocessor performance by coarse-grain coherence avoidance**

- Proposed a no-snoop architecture that virtually gets rid of all broadcasts in a multiprocessor system

### Undergraduate Level

#### **Low-power clock distribution - Bachelor of Technology Thesis**

- Analyzed power-dissipation issues in clocked interconnect tree

#### **Design and layout of 8b\*8b multiplier using modified Booth's algorithm**

- Designed a binary multiplier using low-power pass transistor logic

#### **Microprocessor 8085 kit architecture**

- Designed a microprocessor kit architecture with extended functionality of logic controlling, ADC and DAC interfacing and serial port programming with PC

## SKILLS

### Operating Systems

- LINUX, Solaris, MAC, Windows

### Software

- Cadence tool kit, Synopsys tool kit, MATLAB, ModelSIM, MAGIC, IRSIM

### Languages

- Verilog, VHDL, C, C++, Java, Perl, Python, Tcl, BASH, AWK, SED

## COURSES

### Graduate

- Design of Very Large Scale Integrated Circuits
- Computer Architecture
- Low-power IC and System Design
- Probability and Stochastic Systems
- Algorithms and Data Structures
- Switching and Sequential Systems
- Electronic Devices
- Design with Nanotechnologies
- Electronic Design Automation
- Mathematical Statistics
- Advanced Algorithms
- Linear System Theory

### Undergraduate

- Advanced Digital Design
- Digital Electronics and Microprocessors
- Advanced Probability Theory
- Analog VLSI Design
- Solid State Physics
- Convex Optimization

## HONORS

- Awarded fellowship for graduate studies at Princeton University
- Awarded certificate of merit in undergraduate studies for excellent academic performance
- Awarded certificate of merit in Indian school certificate examination for being amongst top 0.01% of all candidates in Mathematics
- Reached the final of ECDC, an all-India circuit design competition

## REFERENCES

Dr. Niraj Jha  
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